# 10.7Gbps 2 × 2 CROSSPOINT SWITCH w/CML OUTPUTS AND INTERNAL TERMINATION

**Precision Edge™**
**SY58023U**

## FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - **> 10.7Gbps data throughput**
  - **< 60ps $t_r/t_f$ times**
  - **< 285ps $t_{pd}$ (IN-to-Q)**
  - **< 20ps max. skew**
- **Low jitter:**
  - **< $10ps_{(pk-pk)}$ total jitter (clock)**
  - **< $1ps_{(rms)}$ random jitter (data)**
  - **< $10ps_{(pk-pk)}$ deterministic jitter (data)**
- **Crosstalk induced jitter: <$1ps_{(rms)}$**
- **Accepts an input signal as low as 100mV**
- **Unique input termination and $V_T$ pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML**
- **50Ω source terminated CML outputs**
- **Fully differential inputs/outputs**
- **Power supply 2.5V ±5% and 3.3V ±10%**
- **Industrial –40°C to +85°C temperature range**
- **Available in 16-pin (3mm × 3mm) MLF™ package**

**Precision Edge™**

## DESCRIPTION

The SY58023U is a 2.5V/3.3V precision, high-speed, fully differential CML 2 × 2 crosspoint switch. The SY58023U is optimized to provide two identical output copies with less than 20ps of skew and ultra-low jitter. It can route clock signals as fast as 6GHz or data up to 10.7Gbps.

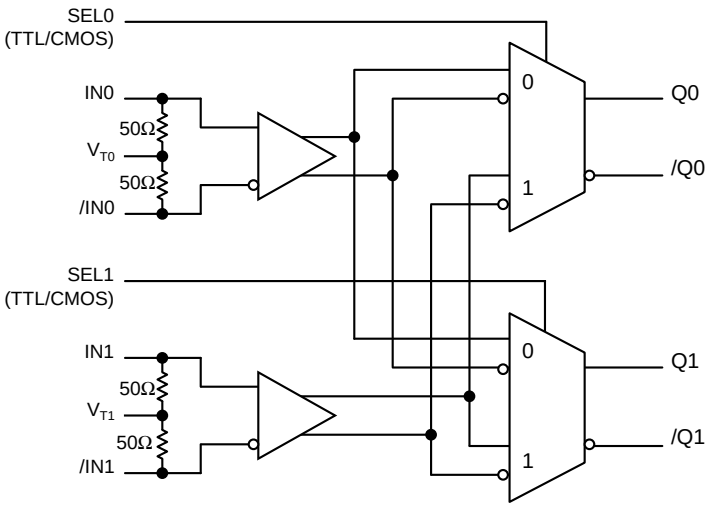
The differential input includes Micrel's unique, 3-pin input termination architecture that allows the SY58023U to directly interface to LVPECL, LVDS, and CML differential signals (AC-coupled or DC-coupled) without any level-shifting or termination resistor networks in the signal path. The CML outputs features 400mV typical swing into 50Ω loads, and provide an extremely fast rise/fall time guaranteed to be less than 60ps.

The SY58023U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require high speed dual CML switches, consider the SY58024U. The SY58023U is part of Micrel's high-speed, Precision Edge™ product line. Data sheets and support documentation can be found on Micrel's website at www.micrel.com.

## APPLICATIONS

- **Gigabit Ethernet data/clock routing**
- **SONET data/clocking routing**
- **Switch fabric clock routing**
- **Redundant switchover**
- **Backplane redundancy**

## FUNCTIONAL BLOCK DIAGRAM

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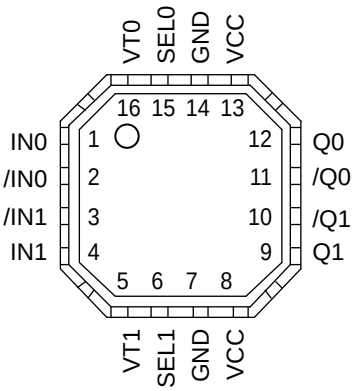
Rev.: A Amendment: /0
Issue Date: June 2003

## PACKAGE/ORDERING INFORMATION




**16-Pin MLF™**

### Ordering Information(Note 1)

| Part Number | Package Type | Operating Range | Package Marking |
|---|---|---|---|
| SY58023UMI | MLF-16 | Industrial | 023U |
| SY58023UMITR(Note 2) | MLF-16 | Industrial | 023U |

**Note 1.** Contact factory for die availability. Die are guaranteed at $T_A = 25°C$, DC electricals only.

**Note 2.** Tape and Reel.

## PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1, 2, 3, 4 | IN0, /IN0, /IN1, IN1 | Differential Signal Input: Each pin of this pair internally terminates with 50Ω to the $V_T$ pin. Note that this input will default to an indeterminate state if left open. See *"Input Interface Applications"* section. |
| 16, 5 | VT0, VT1 | Input Termination Center-Tap: Each input terminates to this pin. The $V_T$ pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See *"Input Interface Applications"* section. |
| 15, 6 | SEL0, SEL1 | Select Input: TTL/CMOS select input control that selects inputs IN0, or IN1. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic High state if left open. |
| 7, 14 | GND, (Exposed Pad) | Ground. Exposed pad must be connected to a ground plane that is the same potential as the device ground pin. |
| 8, 13 | VCC | Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the pins as possible. |
| 12, 11, 10, 9 | Q0, /Q0, /Q1, Q1 | CML Differential Output Pairs: Differential buffered output copy of the selected input signal. The CML single-ended output swing is typically 400mV into 50Ω. Unused output pairs may be left floating with no impact on jitter. See *"CML Output Termination"* section. |

## TRUTH TABLE

| SEL0 | SEL1 | Q0 | Q1 |
|---|---|---|---|
| L | L | IN0 | IN0 |
| L | H | IN0 | IN1 |
| H | L | IN1 | IN0 |
| H | H | IN1 | IN1 |

## Absolute Maximum Ratings(Note 1)

Supply Voltage ($V_{CC}$) ..... –0.5V to +4.0V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{CC}$
CML Output Voltage ($V_{OUT}$) ..... $V_{CC}$ –1.0V to $V_{CC}$ +0.5V
Current ($V_T$)
  Source or Sink Current on $V_T$ pin ..... ±100mA
Input Current ($V_T$)
  Source or Sink Current on IN, /IN ..... ±50mA
Lead Temperature (soldering, 10 sec.) ..... 270°C
Storage Temperature ($T_S$) ..... –65°C +150°C

## Operating Ratings(Note 2)

Supply Voltage ($V_{CC}$) ..... +2.375V to +3.60V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance(**Note 3**)
  MLF™ ($\theta_{JA}$)
    Still-Air ..... 60°C/W
    500lfpm ..... 54°C/W
  MLF™ ($\psi_{JB}$)
    Junction-to-board resistance ..... 33°C/W

## DC ELECTRICAL CHARACTERISTICS(Note 4)

$T_A$ = –40°C to +85°C.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 2.5V nominal<br>3.3V nominal | 2.375<br>3.0 | 2.5<br>3.3 | 2.625<br>3.60 | V<br>V |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = max., current through internal 50Ω source termination resistor included | | 100 | 130 | mA |
| $V_{IH}$ | Input HIGH Voltage | IN, /IN; **Note 5** | $V_{CC}$ –1.6 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | IN, /IN | 0 | | $V_{IH}$ –0.1 | V |
| $V_{IN}$ | Input Voltage Swing | IN, /IN; see Figure 1a | 0.1 | | 1.7 | V |
| $V_{DIFF\_IN}$ | Differential Input Swing | IN, /IN; see Figure 1b | 0.2 | | 3.4 | V |
| $R_{IN}$ | IN-to-$V_T$ Resistance | | 40 | 50 | 60 | Ω |
| IN to $V_T$ | | | | | 1.28 | V |

## CML DC ELECTRICAL CHARACTERISTICS(Note 4)

$V_{CC}$ = 3.3V ±10% or 2.5V ±5%; $R_L$ = 100Ω across each output pair, or equivalent; $T_A$ = –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | Q0, /Q0; Q1, /Q1 | $V_{CC}$–0.020 | | $V_{CC}$ | V |
| $V_{OUT}$ | Output Voltage Swing | Q0, /Q0; Q1, /Q1; see Figure 1a | 325 | 400 | 500 | mV |
| $V_{DIFF\_OUT}$ | Differential Voltage Swing | Q0, /Q0; Q1, /Q1; see Figure 1b | 650 | 800 | 1000 | mV |
| $R_{OUT}$ | Output Source Impedance | Q0, /Q0; Q1, /Q1 | 40 | 50 | 60 | Ω |

## AC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 2.5V ±5% or 3.3V ±10%; $R_L$ = 100Ω across each output pair, or equivalent; $T_A$ = –40°C to +85°C, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Operating Frequency | $V_{IN} \geq 100mV$; $V_{OUT} \geq 200mV$ Clock | 6 | | | GHz |
| | | NRZ Data | 10.7 | | | Gbps |
| $t_{pd}$ | Propagation Delay | IN-to-Q | 135 | | 285 | ps |
| | | SEL-to-Q | 100 | | 400 | ps |
| $t_{CHAN}$ | Channel-to-Channel (Within Bank) | **Note 6** | | | 20 | ps |
| $t_{SKEW}$ | Part-to-Part Skew | **Note 7** | | | 75 | ps |
| $t_{JITTER}$ | Clock Cycle-to-Cycle Jitter | **Note 8** | | | 1 | ps(rms) |
| | Total Jitter | **Note 9** | | | 10 | ps(pk-pk) |
| | Data Random Jitter | **Note 10** | | | 2 | ps(rms) |
| | Deterministic Jitter | **Note 11** | | | 10 | ps(pk-pk) |
| | Crosstalk Induced Jitter | **Note 12** | | <1 | | ps(rms) |
| $t_r$, $t_f$ | Output Rise/Fall Time | 20% to 80%, at full swing | 25 | | 60 | ps |

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

**Note 3.** Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB.

**Note 4.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**Note 5.** $V_{IH}$ (min.) not lower than 1.2V.

**Note 6.** Skew is measured between outputs of the same bank under identical transitions.

**Note 7.** Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

**Note 8.** Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n – T_{n–1}$ where T is the time between rising edges of the output signal.

**Note 9.** Total jitter definition: With an ideal clock input of frequency ≤ $f_{MAX}$, no more than one output edge in $10^{12}$ output edges will deviate by more than the specified peak-to-peak jitter value.

**Note 10.** Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps–3.2Gbps and 10.7Gbps.

**Note 11.** Deterministic jitter is measured at 2.5Gbps–3.2Gbps and 10.7Gbps with both K28.5 and $2^{23}–1$ PRBS pattern.

**Note 12.** Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

## SINGLE-ENDED AND DIFFERENTIAL SWINGS

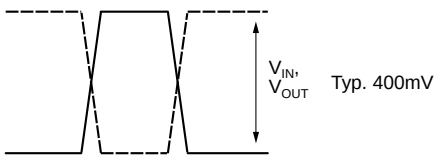



**Figure 1a. Single-Ended Voltage Swing**

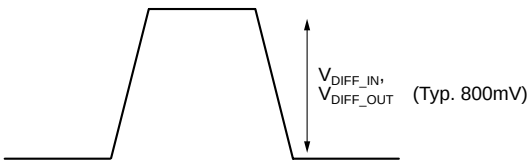



**Figure 1b. Differential Voltage Swing**

## TIMING DIAGRAM

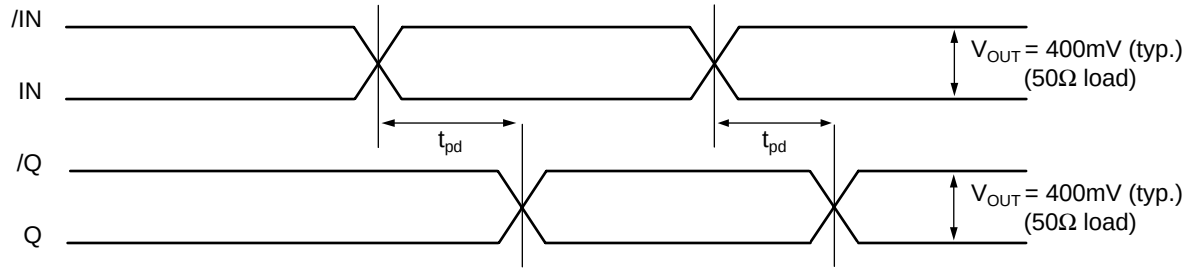
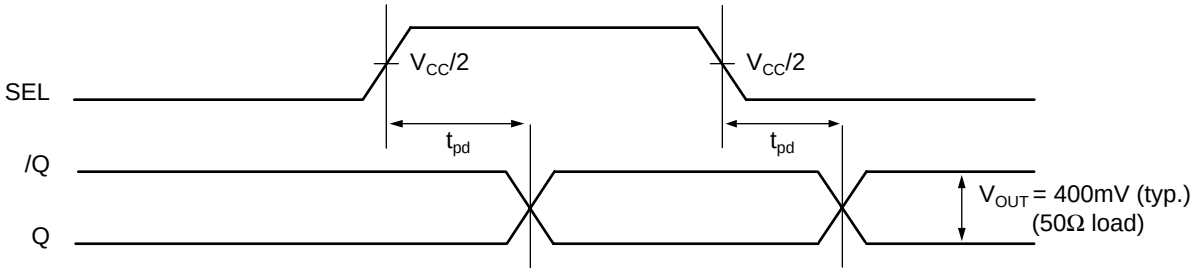



**Figure 2a. AC Timing Diagram IN-to-Q**



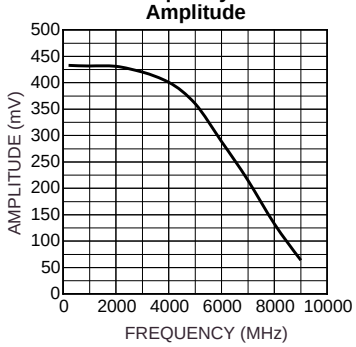

IN0, /IN1 = LOW, /IN0, IN1 = HIGH

**Figure 2b. AC Timing Diagram SEL-to-Q**

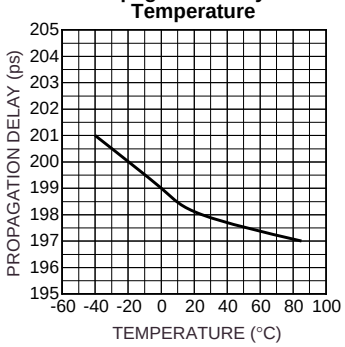
## TYPICAL OPERATING CHARACTERISTICS

$V_{CC}$ = 2.5V, $V_{IN}$ = 100mV, $T_A$ = 25°C, unless otherwise noted.

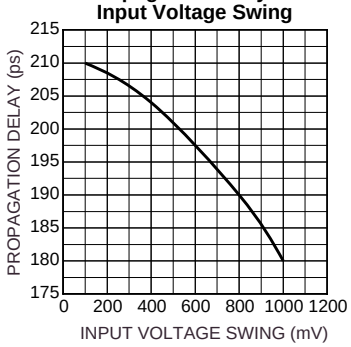
**Frequency vs. Amplitude**



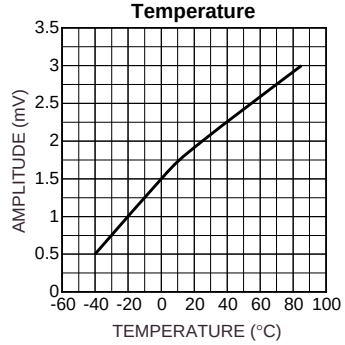

**Propagation Delay vs. Temperature**




**Propagation Delay vs. Input Voltage Swing**



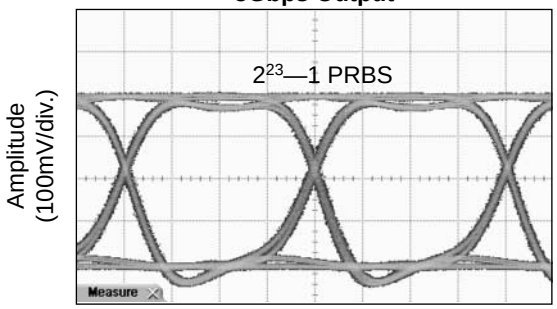

**Within Device Skew vs. Temperature**



## FUNCTIONAL CHARACTERISTICS

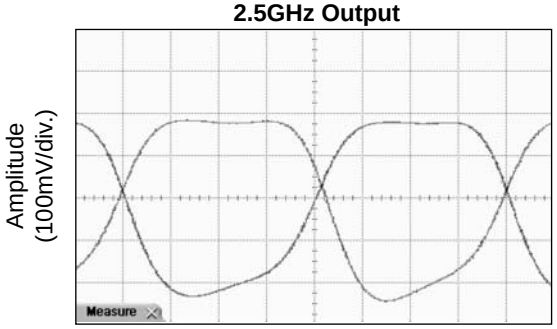
$V_{CC}$ = 2.5V, $V_{IN}$ = 100mV, $T_A$ = 25°C, unless otherwise noted.

**5Gbps Output**



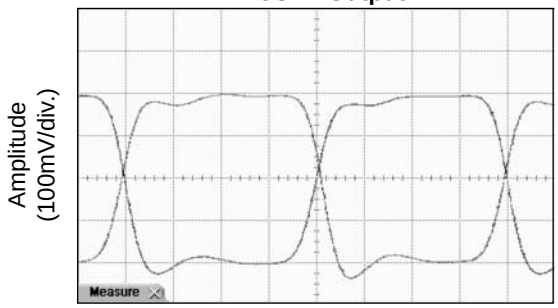

TIME (50ps/div.)

**2.5GHz Output**



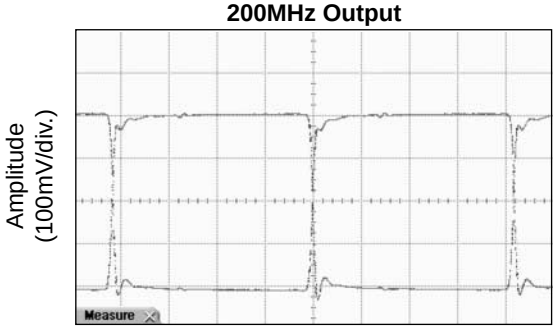

TIME (50ps/div.)

**1.25GHz Output**




TIME (100ps/div.)

**200MHz Output**




TIME (600ps/div.)

## INPUT STAGE

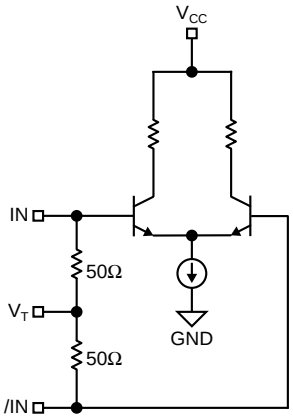



**Figure 3. Simplified Differential Input Buffer**

## INPUT INTERFACE APPLICATIONS

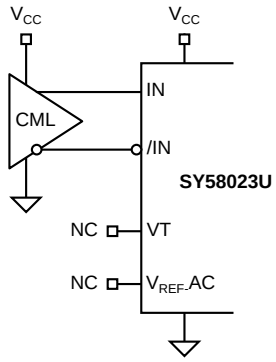



**Figure 4a. DC-Coupled CML Input Interface**
*(Option: may connect $V_T$ to $V_{CC}$)*

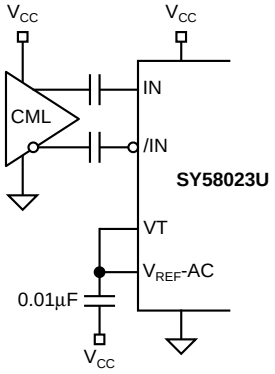
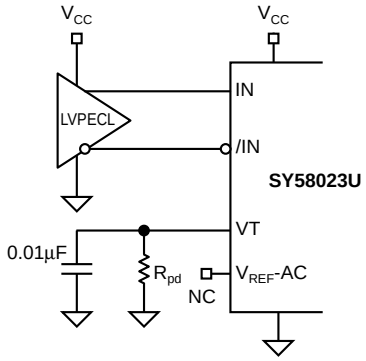
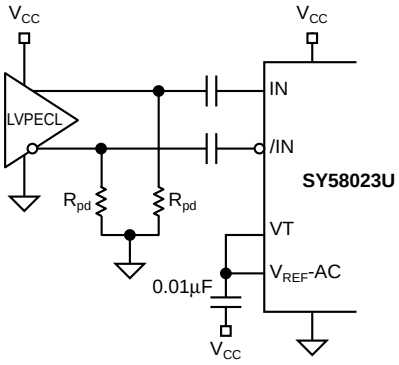



**Figure 4b. AC-Coupled CML Input Interface**




For $V_{CC}$ = 2.5V, $R_{pd}$ = 19Ω
For $V_{CC}$ = 3.3V, $R_{pd}$ = 50Ω

**Figure 4c. DC-Coupled LVPECL Input Interface**




For $V_{CC}$ = 2.5V, $R_{pd}$ = 50Ω
For $V_{CC}$ = 3.3V, $R_{pd}$ = 100Ω

**Figure 4d. AC-Coupled LVPECL Input Interface**

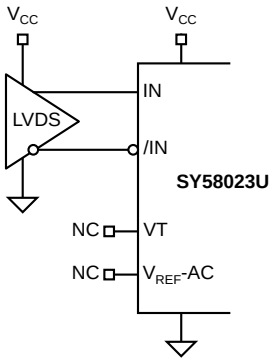



**Figure 4e. LVDS Input Interface**

## CML OUTPUT TERMINATION

Figures 5 and Figure 6 illustrates how to terminate a CML output using both the AC-coupled and DC-coupled configuration. All outputs of the SY58023U are 50Ω with a 16mA current source.

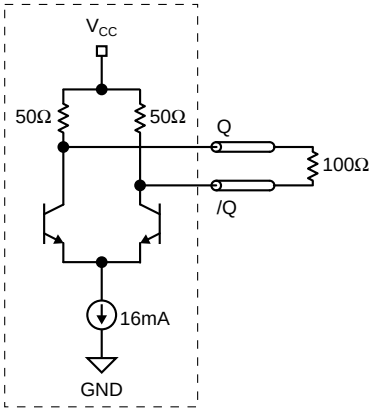



**Figure 5. CML**
**DC-Coupled Termination**

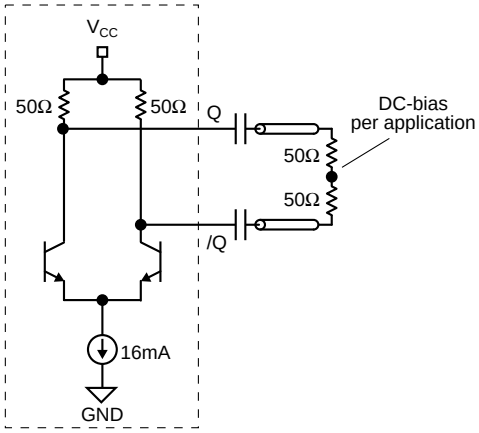
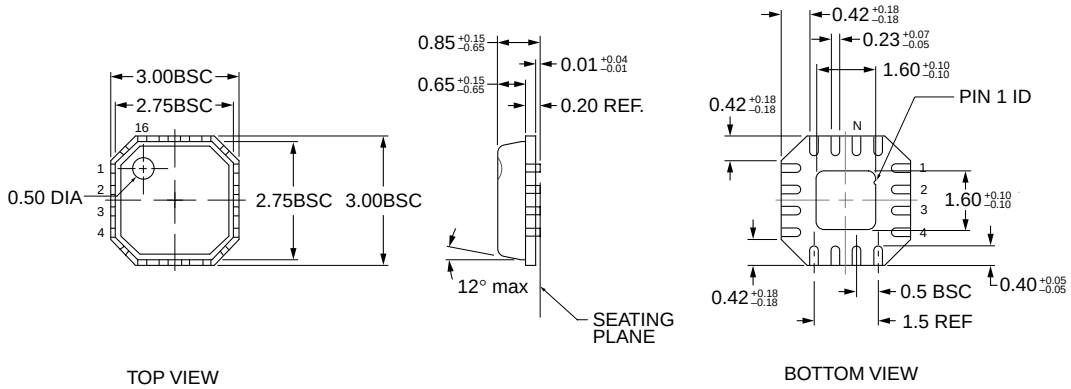



**Figure 6. CML**
**AC-Coupled Termination**

## RELATED PRODUCT AND SUPPORT DOCUMENTATION

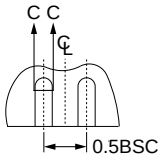
| Part Number | Function | Data Sheet Link |
|---|---|---|
| SY58023U | 6GHz (10.7Gbps) 2×2 Crosspoint Switch w/CML Outputs | http://www.micrel.com/product-info/products/sy58023u.shtml |
| SY58024U | 5.5GHz (10.7Gbps) Dual 2×2 Crosspoint Switch w/CML Outputs | http://www.micrel.com/product-info/products/sy58024u.shtml |
| | 16-MLF™ Manufactering Guidelines Exposed Pad Application Note | www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf |
| | HBW Solutions | http://www.micrel.com/product-info/as/solutions.shtml |

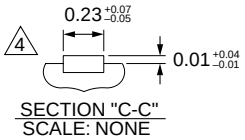
## 16 LEAD *Micro*LeadFrame™ (MLF-16)




TOP VIEW

BOTTOM VIEW

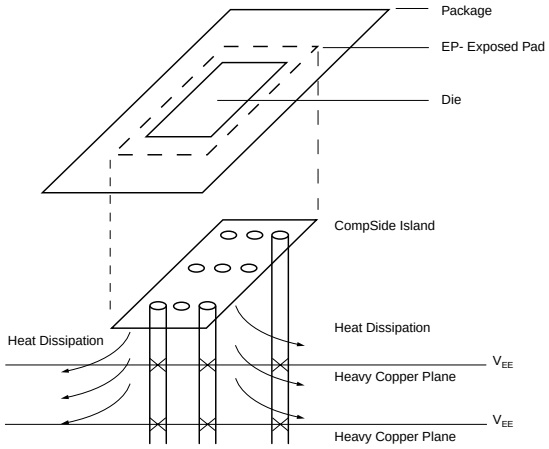



SECTION "C-C"
SCALE: NONE

1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02




**PCB Thermal Consideration for 16-Pin MLF™ Package**
**(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

**Note 1.** Package meets Level 2 qualification.

**Note 2.** All parts are dry-packaged before shipment.

**Note 3.** Exposed pads must be soldered to a ground for proper thermal management.

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