5.5GHz 1:4 FANOUT BUFFER/ TRANSLATOR w/400mV LVPECL OUTPUTS AND INTERNAL INPUT TERMINATION

Precision Edge™
SY58022U

FEATURES

- **Precision 1:4, 400mV LVPECL fanout buffer**
- **Guaranteed AC performance over temperature and voltage:**
  - **> 5.5GHz f_{MAX} clock**
  - **< 80ps t_r/t_f times**
  - **< 250ps ($V_{IN} \geq$ 300mV) t_{pd}**
  - **< 15ps max. skew**
- **Low jitter performance:**
  - **< 10ps$_{(pk-pk)}$ total jitter (clock)**
  - **< 1ps$_{(rms)}$ random jitter (data)**
  - **< 10ps$_{(pk-pk)}$ deterministic jitter (data)**
- **Accepts an input signal as low as 100mV**
- **Unique input termination and V_T pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS and CML**
- **400mV LVPECL compatible outputs**
- **Power supply 2.5V ±5% and 3.3V ±10%**
- **–40°C to +85°C temperature range**
- **Available in 16-pin (3mm × 3mm) MLF™ package**

APPLICATIONS

- **All SONET and All GigE clock distribution**
- **Fibre Channel clock and data distribution**
- **Backplane distribution**
- **Data distribution: OC-48, OC-48+FEC, XAUI**
- **High-end, low-skew, multiprocessor synchronous clock distribution**

Precision Edge™

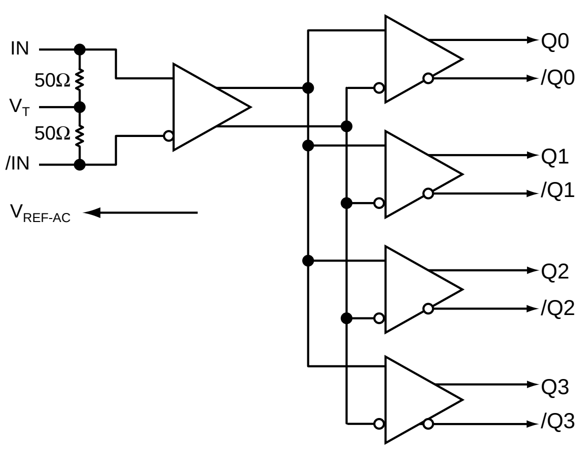
DESCRIPTION

The SY58022U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 LVPECL fanout buffer. Optimized to provide four identical output copies with less than 15ps of skew and less than 10ps$_{(pk-pk)}$ total jitter, the SY58022U can process clock signals as fast as 5.5GHz.

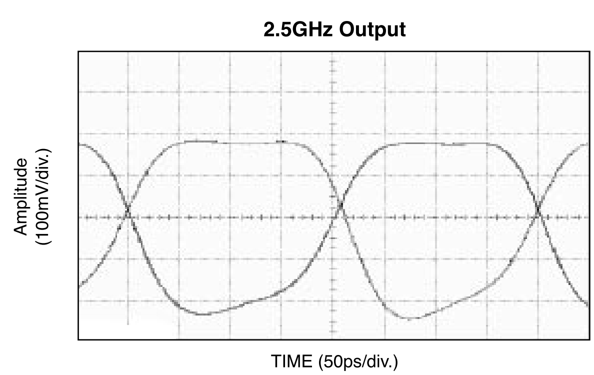
The differential input includes Micrel's unique, 3-pin input termination architecture interfaces to differential LVPECL, CML, and LVDS signals (AC-coupled or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V_{REF-AC}) is provided to bias the V_T pin. The outputs are 400mV LVPECL compatible, with extremely fast rise/fall times guaranteed to be less than 80ps.

The SY58022U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require greater output swing or CML compatible outputs, consider the SY58021U 1:4 fanout buffer with LVPECL outputs, or the SY58020U 1:4 fanout buffer with 400mV CML outputs. The SY58022U is part of Micrel's high-speed, Precision Edge™ product line. Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM

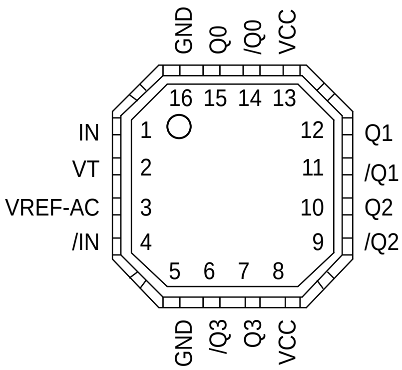


TYPICAL PERFORMANCE



Rev.: A Amendment: /0
Issue Date: July 2003

PACKAGE/ORDERING INFORMATION



16-Pin MLF™

Ordering Information(Note 1)

Part Number	Package Type	Operating Range	Package Marking
SY58022UMI	MLF-16	Industrial	022U
SY58022UMITR(Note 2)	MLF-16	Industrial	022U

Note 1. Contact factory for die availability. Die are guaranteed at T_A = 25°C, DC electricals only.

Note 2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair receives the signal to be buffered. Each pin is internally terminated with 50Ω to the V_T pin. Note that this input will default to an indeterminate state if left open. See *"Input Interface Applications"* section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The V_T pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See *"Input Interface Applications"* section.
3	VREF-AC	Reference Output Voltage: This output biases to V_{CC} –1.2V. It is used when AC-coupling to differentail inputs. Connect V_{REF-AC} directly to the V_T pin. Bypass with 0.01µF low ESR capacitor to V_{CC}. See *"Input Interface Applications"* section.
8, 13	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the pins as possible. A 0.01µF capacitor should be as close to the V_{CC} pin as possible.
5, 16	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14, 15 11, 12 9, 10 6, 7	/Q0, Q0, /Q1, Q1, /Q2, Q2, /Q3, Q3,	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 400mV. Proper termination is 50Ω to V_{CC}–2V at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See *"LVPECL Output Termination"* section.

Absolute Maximum Ratings (Note 1)

Power Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
Output Current (I_{OUT})
Continuous 50mA
Surge 100mA
V_T Current
Source or sink current on V_T pin .... ±100mA
Input Current
Source or sink current on (IN, /IN) .... ±50mA
V_{REF} Current
Source or sink current on V_{REF-AC}, **Note 4** .... ±1.5mA
Soldering, (10 sec.) .... 270°C
Storage Temperature Range (T_{STORE}) .... –65 to +150°C

Operating Ratings (Note 2)

Power Supply Voltage (V_{CC}) .... +2.375V to +3.60V
Operating Temperature Range (T_A) .... –40°C to +85°C
Package Thermal Resistance
MLF™ (θ_{JA})
Still-Air .... 60°C/W
500lpfm .... 54°C/W
MLF™ (ψ_{JB})
(Junction-to-Board Resistance), **Note 3** .... 33°C/W

DC ELECTRICAL CHARACTERISTICS (Note 5)

T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.60	V V
I_{CC}	Power Supply Current	No load, V_{CC} = max		125	160	mA
V_{IH}	Input HIGH Voltage	IN, /IN, **Note 6**	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input LOW Voltage	IN, /IN	0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing	IN, /IN; See Figure 1a	0.1		3.6	V
V_{DIFF_IN}	Differential Input Voltage	IN, /IN; See Figure 1b	0.2		3.4	V
R_{IN}	IN-to-V_T Resistance		40	50	60	Ω
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
$V_{T\ IN}$	IN-to-V_T Voltage				1.28	V

LVPECL DC ELECTRICAL CHARACTERISTICS (Note 5)

V_{CC} = 3.3V ±10% or V_{CC} = 2.5 ±5%; R_L= 50Ω to V_{CC}–2V; T_A= –40°C to 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC}–1.145	V_{CC}–1.020	V_{CC}–0.895	V
V_{OL}	Output LOW Voltage		V_{CC}–1.545	V_{CC}–1.420	V_{CC}–1.295	V
V_{OUT}	Output Differential Swing	see Figure 1a	150	400	650	mV
V_{DIFF_OUT}	Deferential Output Swing	see Figure 1b	300	800	1300	mV

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

Note 4. Due to the limited drive capability, use for input of the same package only.

Note 5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 6. V_{IH} (min.) not lower than 1.2V.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC}–2V; T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ≥ 200mV Clock	5.5			GHz
		NRZ Data		10		Gbps
t_{pd}	Propagation Delay		130	200	280	ps
t_{CHAN}	Channel-to-Channel Skew	**Note 7**		4	15	ps
t_{SKEW}	Part-to-Part Skew	**Note 8**			50	ps
t_{JITTER}	Clock Cycle-to-Cycle Jitter	**Note 9**			1	ps(rms)
	Total Jitter	**Note 10**			10	ps(pk-pk)
	Data Random Jitter	**Note 11** 2.5Gbps – 3.2Gbps			1	ps(rms)
	Deterministic Jitter	**Note 12** 2.5Gbps – 3.2Gbps			10	ps(pk-pk)
t_r, t_f	Output Rise/Fall Time 20% to 80%	At full swing	20	50	80	ps

Note 7. Skew is measured between outputs of the same bank under identical transitions.

Note 8. Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

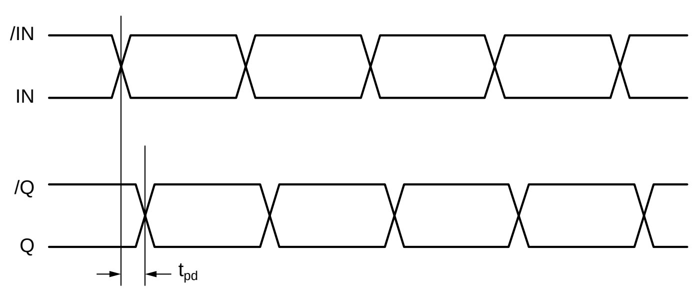
Note 9. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, $T_n–T_{n–1}$ where T is the time between rising edges of the output signal.

Note 10. Total jitter definition: With an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Note 11. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.

Note 12. Deterministic jitter is measured at 2.5Gbps/3.2Gbps with both K28.5 and 2^{23}–1 PRBS pattern.

TIMING DIAGRAM



SINGLE-ENDED AND DIFFERENTIAL SWINGS

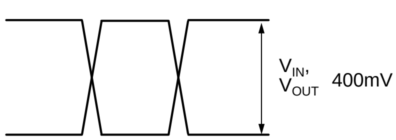


Figure 1a. Single-Ended Swing

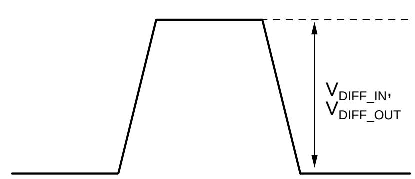
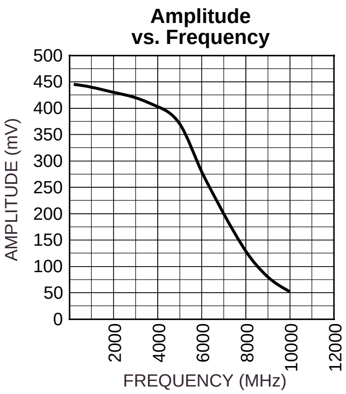
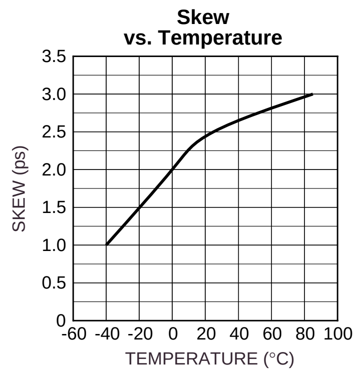


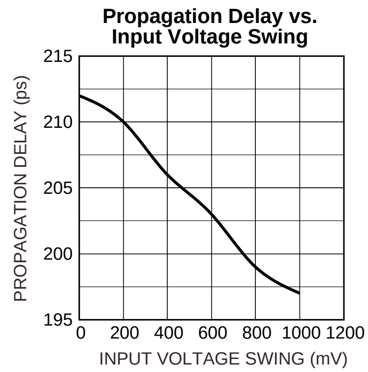
Figure 1b. Differential Swing

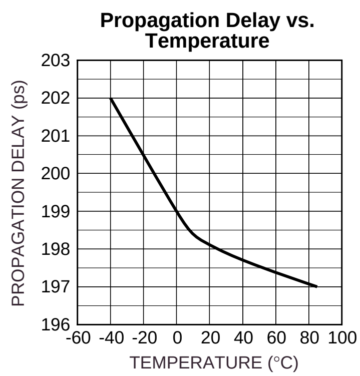
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{EE} = 0V, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.





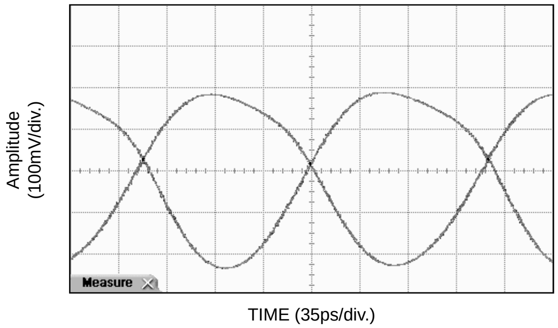




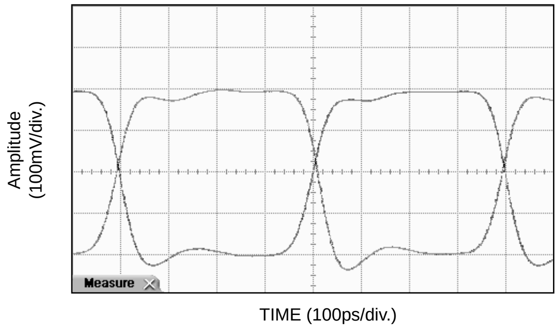
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, V_{EE} = 0V, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

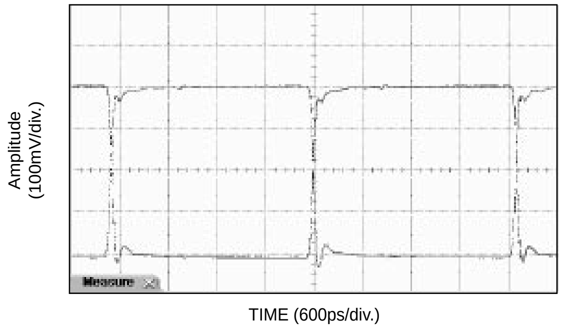
4GHz Output



1.25GHz Output



200MHz Output



INPUT STAGE

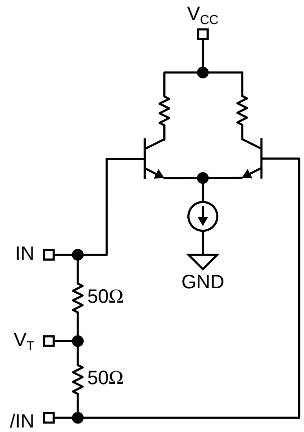
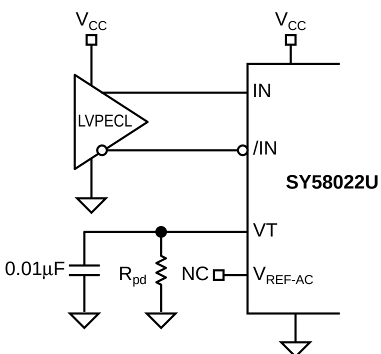


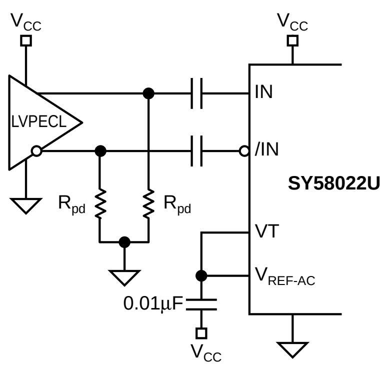
Figure 2. Simplified Differential Input Buffer

INPUT INTERFACE APPLICATIONS



For V_{CC} = 2.5V, R_{pd} = 19Ω
For V_{CC} = 3.3V, R_{pd} = 50Ω

Figure 3a. DC-Coupled LVPECL Input Interface



R_{pd} = 100Ω for a 3.3V system
R_{pd} = 50Ω for a 2.5V system

Figure 3b. AC-Coupled LVPECL Input Interface

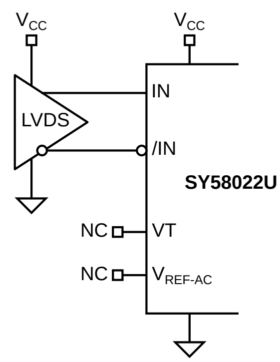
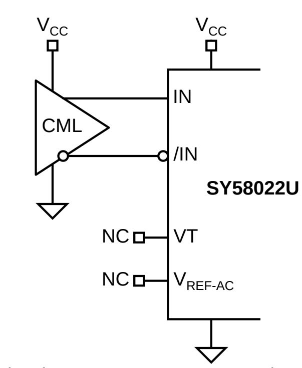


Figure 3c. LVDS Input Interface



(Option: May connect V_T to V_{CC})

Figure 3d. AC-Coupled CML Input Interface

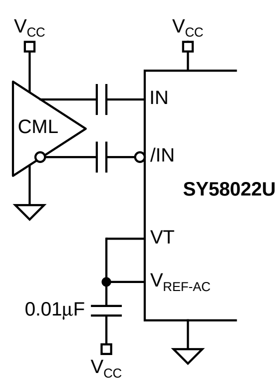


Figure 3e. CML Input Interface

OUTPUT TERMINATION RECOMMENDATIONS

LVPECL outputs have very low output impedance (open emitter), and small signal swing which results in low EMI (electro-magnetic interference). The LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. In addition, LVPECL is compatible for driving standard PECL inputs since PECL inputs require only 100mV input swing. Further, there are several techniques in terminating the LVPECL outputs, as shown in Figure 4 through 6.

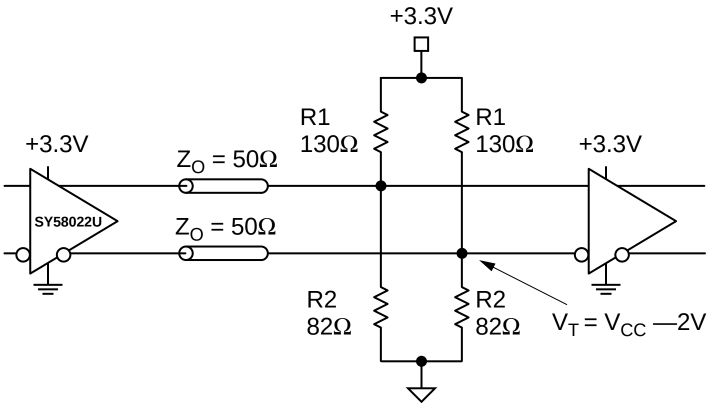


Figure 4. Parallel Termination–Thevenin Equivalent

Note 1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω

Note 2. For +3.3V systems: R1 = 130Ω, R2 = 83Ω

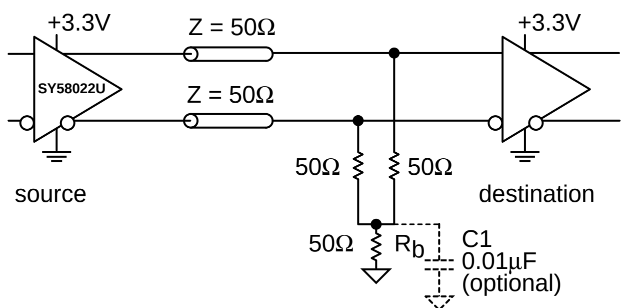


Figure 5. Three-Resistor "Y–Termination"

Note 1. Power-saving alternative to Thevenin termination.

Note 2. Place termination resistors as close to destination inputs as possible.

Note 3. R_b resistor sets the DC bias voltage, equal to V_T.
For +2.5V systems R_b = 19Ω.
For +3.3V systems R_b = 46Ω to 50Ω.

Note 4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

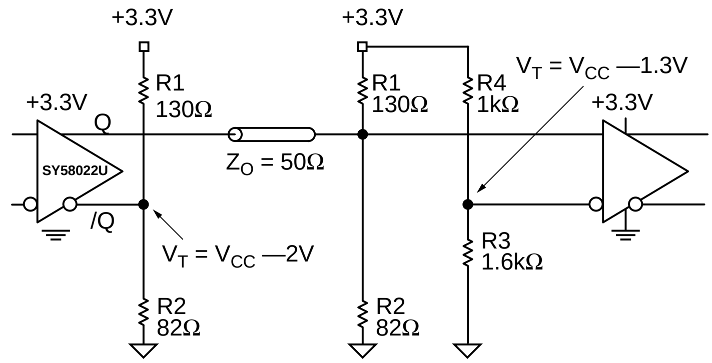


Figure 6. Terminating Unused I/O

Note 1. Unused output (/Q) must be terminated to balance the output.

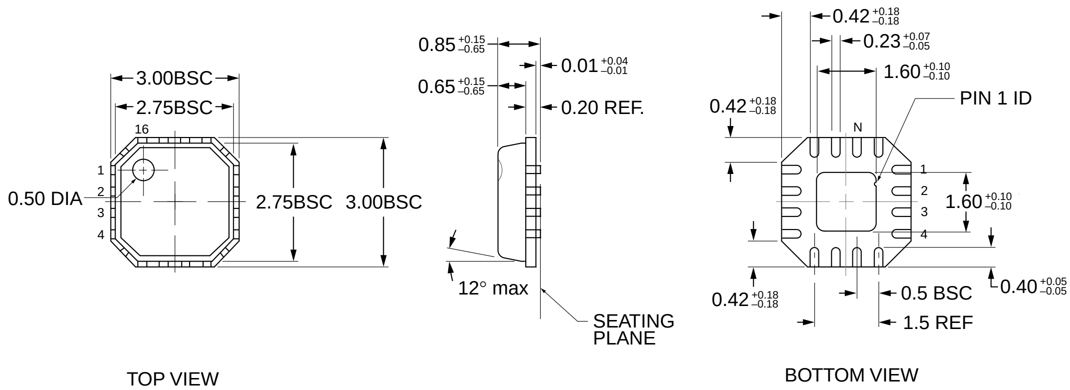
Note 2. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.
For +3.3V systems: R1 = 130Ω, R2 = 82Ω, R3 = 1kΩ, R4 = 1.6kΩ.

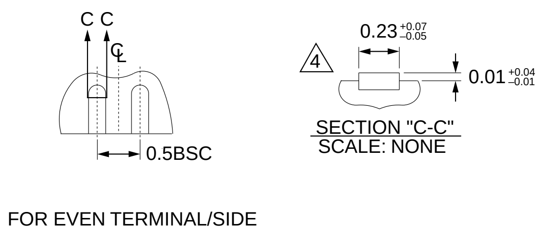
Note 3. Unused output pairs (Q and /Q) may be left floating.

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58020U	6GHz, 1:4 CML Fanout Buffer/Translator Internal I/O Termination	http://www.micrel.com/product-info/prod/ucts/sy58020u.shtml
SY58021U	4GHz, 1:4 LVPECL Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/product-info/products/sy58021u.shtml
SY58022U	5.5GHz, 1:4 Fanout Buffer/Translator w/400mV LVPECL Outputs and Internal Input Termination	http://www.micrel.com/product-info/products/sy58022u.shtml
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
M-0317	HBW Solutions	http://www.micrel.com/product-info/as/solutions.shtml

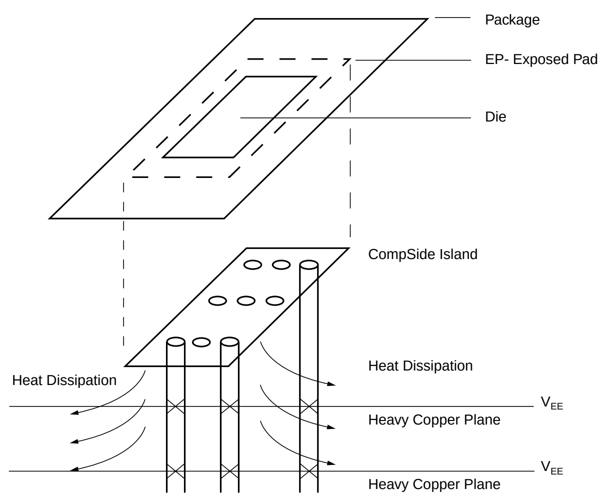
16 LEAD *Micro*LeadFrame™ (MLF-16)





1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com