10.7Gbps DIFFERENTIAL 400mV LVPECL 2:1 MUX WITH INTERNAL TERMINATION

Precision Edge™
SY58019U

FEATURES

- **Guaranteed AC performance over temperature and voltage:**
  - **> 10.7Gbps data throughput**
  - **> 7GHz f_{MAX} (clock)**
  - **< 240ps propagation delay**
  - **< 70ps t_r / t_f times**
- **Ultra-low crosstalk induced jitter: 1ps$_{(rms)}$**
- **Ultra-low jitter design:**
  - **< 1ps$_{(rms)}$ random jitter**
  - **< 10ps$_{(pk-pk)}$ deterministic jitter**
  - **< 10ps$_{(pk-pk)}$ total jitter (clock)**
- **Unique input termination and V_T pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)**
- **400mV (100k) LVPECL output swing**
- **Power supply 2.5V ±5% or 3.3V ±10%**
- **–40°C to +85°C temperature range**
- **Available in 16-pin (3mm × 3mm) MLF™ package**

APPLICATIONS

- **Redundant clock distribution**
- **OC-3 to OC-192 SONET/SDH clock/data distribution**
- **Loopback**
- **Fibre Channel distribution**

Precision Edge™

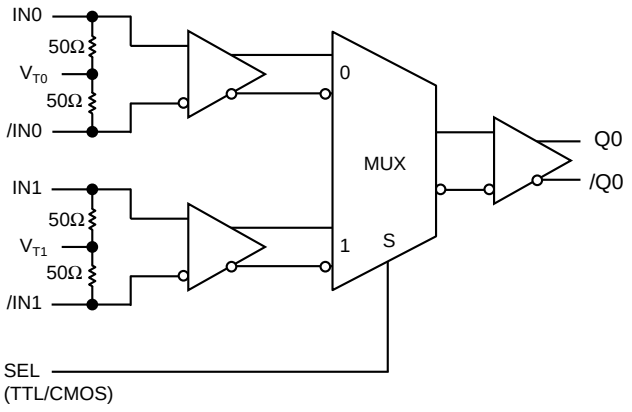
DESCRIPTION

The SY58019U is a 2.5V/3.3V precision, high-speed, 2:1 differential MUX capable of handling clocks up to 7GHz and data up to 10.7Gbps.

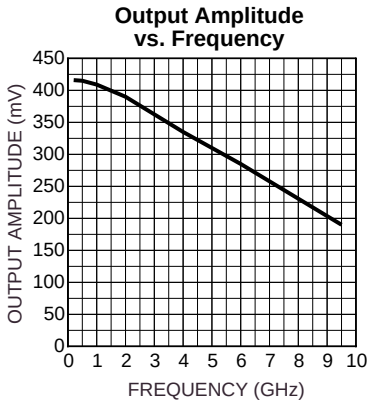
The differential input includes Micrel's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 400mV, 100k compatible, LVPECL, with extremely fast rise/fall times guaranteed to be less than 70ps.

The SY58019U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require CML outputs, consider the SY58017U or for 800mV LVPECL outputs the SY58018U. The SY58019U is part of Micrel's high-speed, Precision Edge™ product line. Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

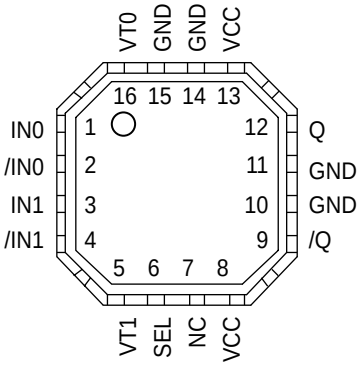
FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE



PACKAGE/ORDERING INFORMATION



16-Pin MLF™

Ordering Information(Note 1)

Part Number	Package Type	Operating Range	Package Marking
SY58019UMI	MLF-16	Industrial	019U
SY58019UMITR(Note 2)	MLF-16	Industrial	019U

Note 1. Contact factory for die availability. Die is guaranteed at T_A = 25°C, DC electricals only.

Note 2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 2 3, 4	IN0, /IN0 IN1, /IN1	Differential Input: These input pairs are the differential signal inputs to the device. They accept differential AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a V_T pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the *"Input Interface Applications"* section for more details.
16, 5	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a V_T pin. The V_{T0} and V_{T1} pins provide a center-tap to a termination network for maximum interface flexibility. See *"Input Interface Applications"* section for more details.
6	SEL	This single-ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
7	NC	No connect.
8, 13	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors. 0.01µF capacitor should be as close to V_{CC} pin as possible.
12, 9	Q, /Q	Differential Outputs: This 100k compatible LVPECL output pair is the output of the device. Terminate through 50Ω to V_{CC}–2V. See *"Output Interface Applications"* section. It is a logic function of the IN0, IN1, and SEL inputs. Please refer to the *"Truth Table"* for details.
10, 11, 14, 15	GND, Exposed Pad	Ground. Ground pins and exposed pad must be connected to the same ground plane.

TRUTH TABLE

INPUTS					OUTPUTS	
IN0	/IN0	IN1	/IN1	SEL	Q	/Q
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

Absolute Maximum Ratings(Note 1)

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Termination Current, **Note 3**
  Source or sink current on V_T pin ..... ±100mA
Input Current
  Source or sink current on IN, /IN pin ..... ±50mA
Lead Temperature (soldering, 10 sec.) ..... 220°C
Storage Temperature Range (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Power Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance, **Note 4**
  MLF™ (θ_{JA})
    Still-Air ..... 60°C/W
    500lpfm ..... 54°C/W
  MLF™ (ψ_{JB})
    Junction-to-Board ..... 33°C/W

DC ELECTRICAL CHARACTERISTICS(Note 5)

T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}		55	70	mA
R_{DIFF_IN}	Differential Input Resistance (IN0-to-/IN0, IN1-to-/IN1)		80	100	120	Ω
R_{IN}	Input Resistance (IN0-to-V_{T0}, /IN0-to-V_{T0}, IN1-to-V_{T1}, /IN1-to-V_{T1})		40	50	60	Ω
V_{IH}	Input HIGH Voltage (IN0, /IN0, IN1, /IN1)	**Note 6**	1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN0, /IN0, IN1, /IN1)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN0, /IN0, IN1, /IN1)	See Figure 1a	100			mV
V_{DIFF_IN}	Differential Input Voltage Swing |IN0, /IN0|, |IN1, /IN1|	See Figure 1b	200			mV
$V_{T\ IN}$	IN to V_T (IN0, /IN0, IN1, /IN1)				1.28	V

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Due to the limited drive capability, use for input of the same package only.

Note 4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB.

Note 5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 6. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS(Note 7)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C; R_L = 50Ω to V_{CC}—2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}–1.545		V_{CC}–1.295	V
V_{OUT}	Output Differential Swing Q, /Q	See Figure 1a	200	400		mV
V_{DIFF_OUT}	Differiential Output Voltage Swing Q, /Q	See Figure 1b	400	800		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS(Note 7)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current				300	µA

Note 7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[Note 8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C, R_L = 50Ω to V_{CC}—2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	10.7			Gbps
		$V_{OUT} \geq$ 200mV Clock		7		GHz
t_{pd}	Differential Propagation Delay	IN-to-Q	90	160	240	ps
		SEL-to-Q	50	160	350	ps
t_{SKEW}	Input-to-Input Skew	**Note 9**		3	15	ps
	Part-to-Part Skew	**Note 10**			100	ps
t_{JITTER}	Data Random Jitter	**Note 11**			1	$ps_{(rms)}$
	Deterministic Jitter	**Note 12**			5	$ps_{(pk-pk)}$
	Clock Cycle-to-Cycle Jitter	**Note 13**			1	$ps_{(rms)}$
	Total Jitter	**Note 14**			10	$ps_{(pk-pk)}$
	Crosstalk-induced Jitter (Clock/Data) Channel-to-Channel	**Note 15**		1		$ps_{(rms)}$
t_r, t_f	Output Rise/Fall Time	20% to 80%, at full swing	20	40	70	ps

Note 8. High-frequency AC parameters are guaranteed by design and characterization.

Note 9. Input-to-input skew is the difference in time from an input to output in comparison to any other input-to-output. In addition, the input-to-input skew does not include the output skew.

Note 10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

Note 11. RJ is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps/3.2Gbps.

Note 12. DJ is measured at 10.7Gbps and 2.5Gbps/3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern

Note 13. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.

Note 14. Total jitter definition: With an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Note 15. Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

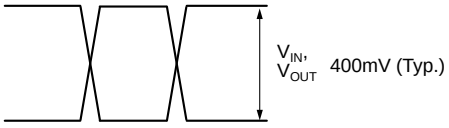


Figure 1a. Single-Ended Voltage Swing

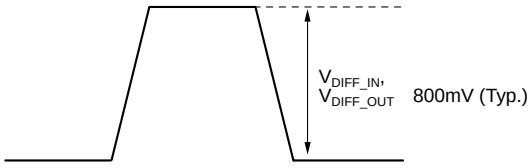
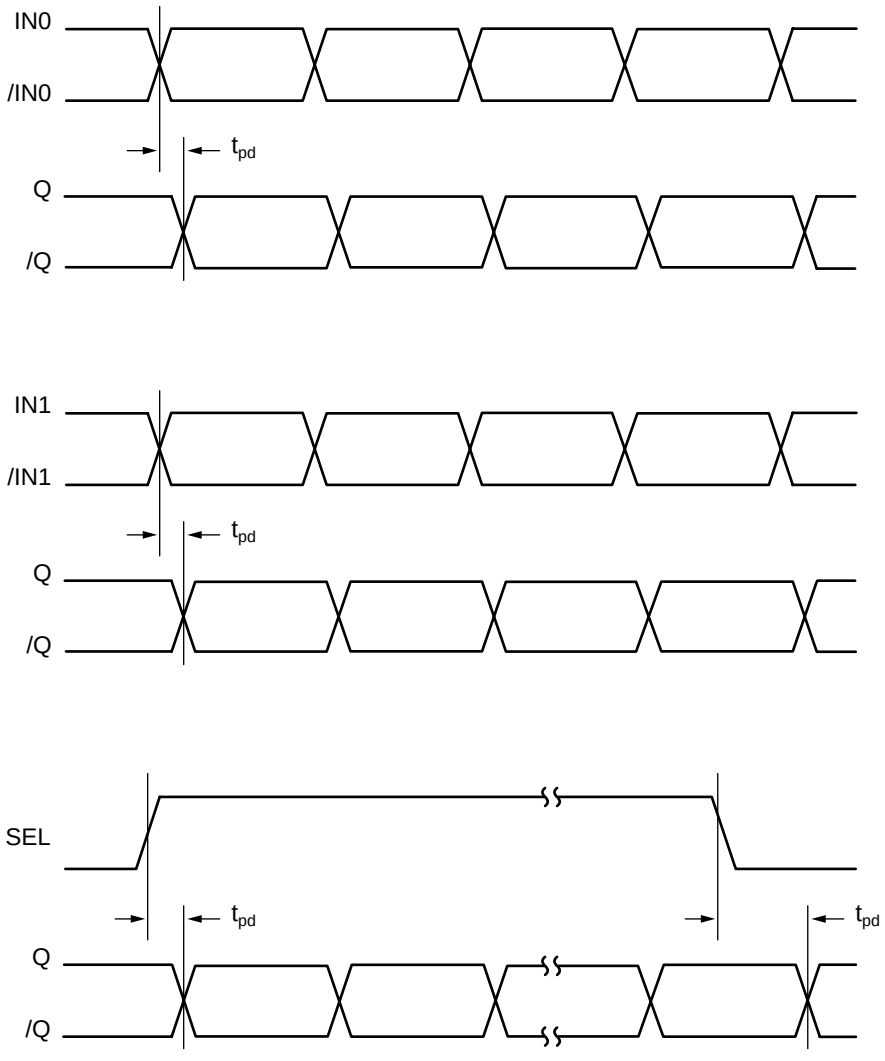


Figure 1b. Differential Voltage Swing

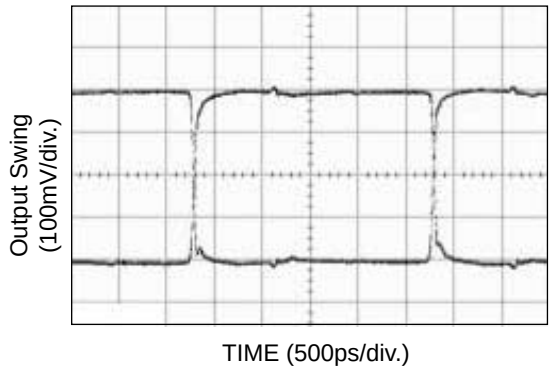
TIMING DIAGRAMS



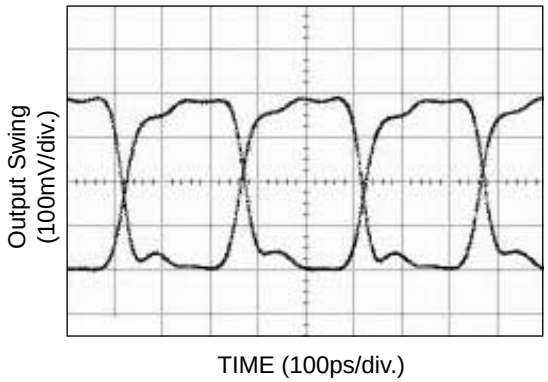
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

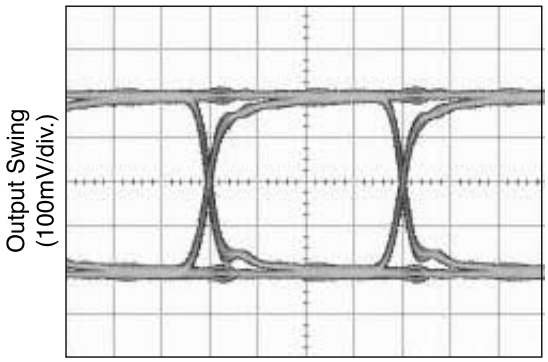
200MHz Output



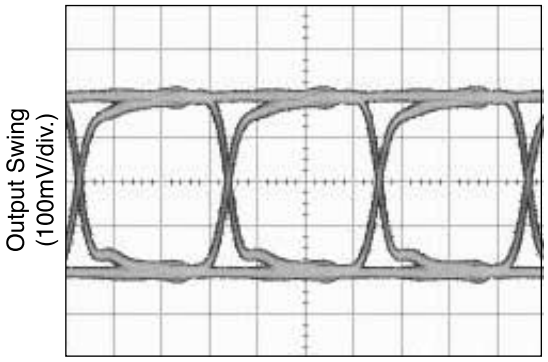
2GHz Output



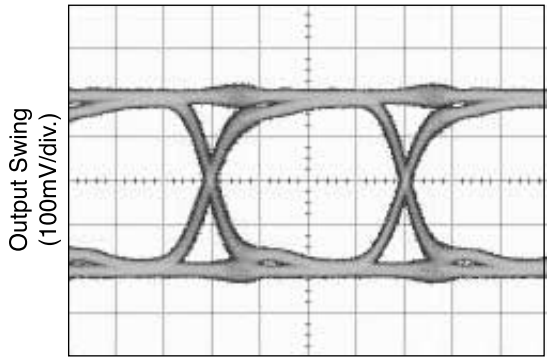
2.5Gbps Output



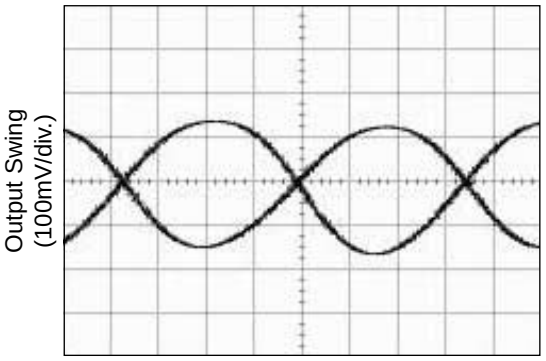
3.2Gbps Output



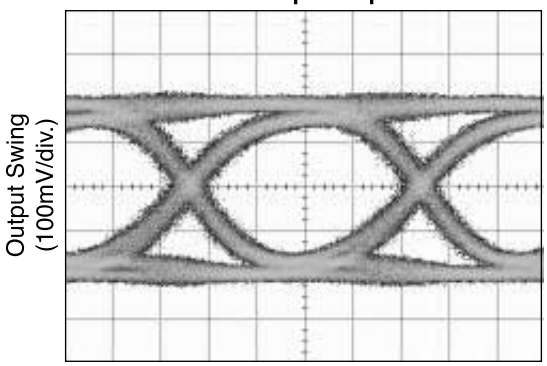
5Gbps Output



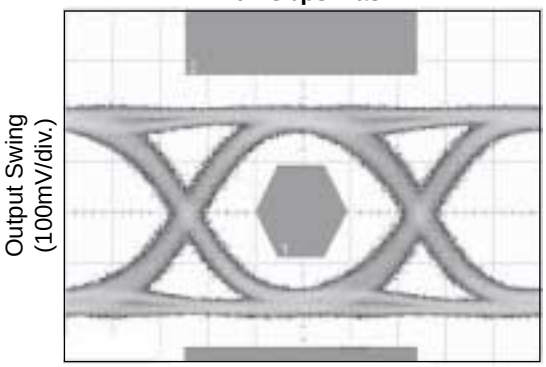
7GHz Output



10.7Gbps Output



10.7Gbps Mask



INPUT AND OUTPUT STAGES

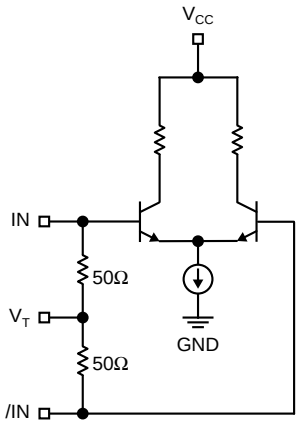


Figure 2a. Simplified Differential Input Stage

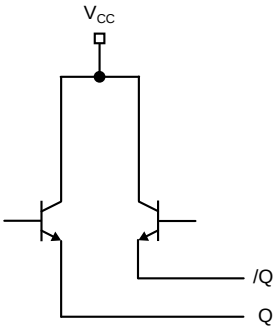


Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS

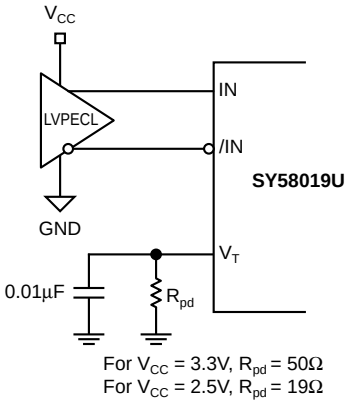


Figure 3a. LVPECL Interface (DC-coupled)

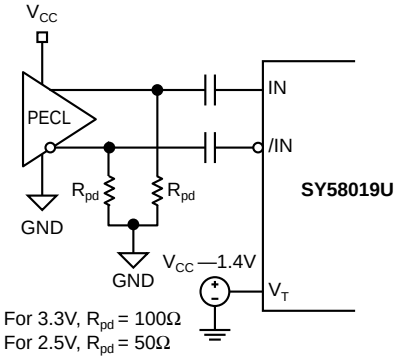


Figure 3b. LVPECL Interface (AC-coupled)

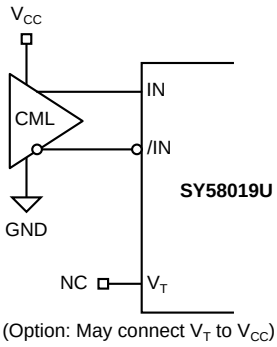


Figure 3c. CML Interface (DC-coupled)

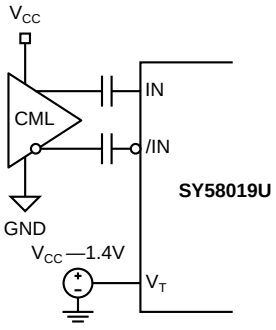


Figure 3d. CML Interface (AC-coupled)

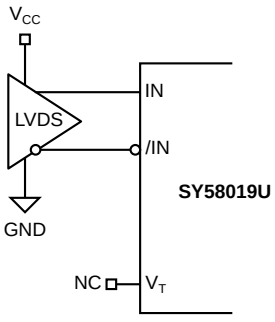


Figure 3e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

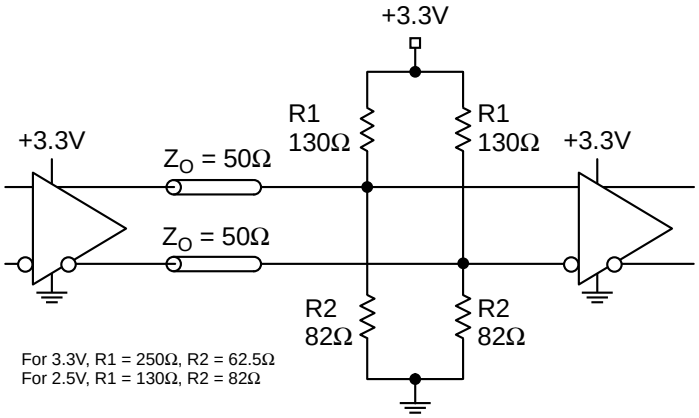


Figure 4a. Parallel Thevenin-Equivalent Termination

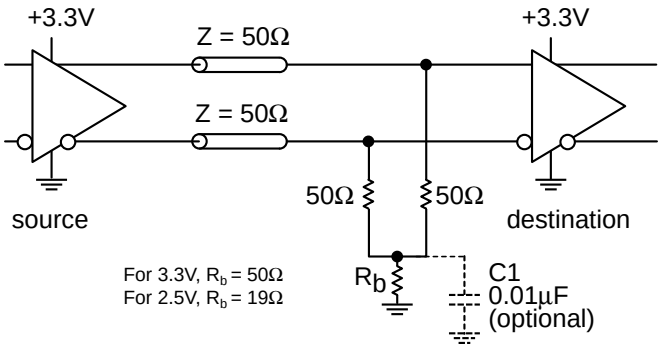


Figure 4b. Three-Resistor "Y" Termination

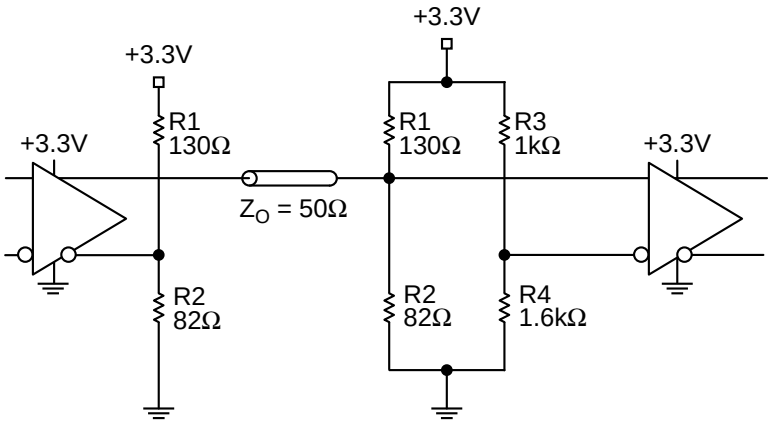
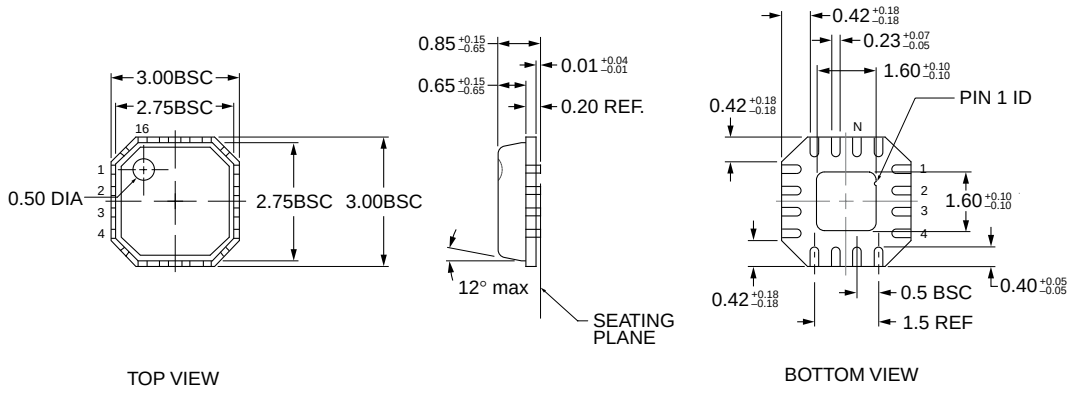


Figure 4c. Terminating Unused I/O

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

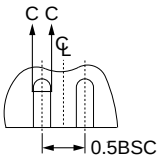
Part Number	Function	Data Sheet Link
SY58016L	3.3V 10Gbps Differential CML Line Driver/Receiver with Internal Termination	http://www.micrel.com/product-info/products/sy58016l.shtml
SY58017U	10.7Gbps Differential CML 2:1 Mux with Internal Termination	http://www.micrel.com/product-info/products/sy58017u.shtml
SY58018U	5Gbps Differential LVPECL 2:1 Mux with Internal Termination	http://www.micrel.com/product-info/products/sy58018u.shtml
SY58025U	10.7Gbps Dual 2:1 CML Mux with Internal I/O Termination	http://www.micrel.com/product-info/products/sy58025u.shtml
SY58026U	5Gbps Dual 2:1 Mux with Internal Termination	http://www.micrel.com/product-info/products/sy58026u.shtml
SY58027U	10.7Gbps Dual 2:1 400mV LVPECL Mux with Internal Termination	http://www.micrel.com/product-info/products/sy58027u.shtml
SY58051U	10.7Gbps AnyGate® with Internal Input and Output Termnation	http://www.micrel.com/product-info/products/sy58051u.shtml
SY58052U	10Gbps Clock/Data Retimer with 50Ω Input Termination	http://www.micrel.com/product-info/products/sy58052u.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

16 LEAD *Micro*LeadFrame™ (MLF-16)

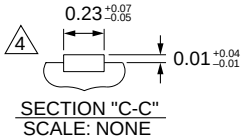


TOP VIEW

BOTTOM VIEW

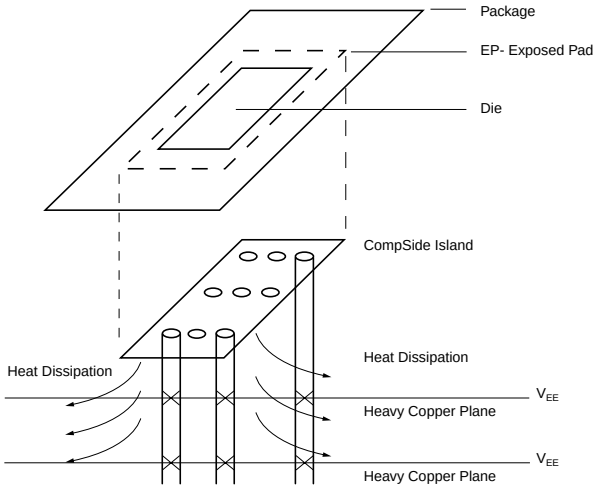


FOR EVEN TERMINAL/SIDE



1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

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