

FEATURES

- Accepts up to 10.7Gbps data
- < 45ps edge rate
- Gain $\geq 4V/V$
- CML/PECL differential inputs
- CML outputs
- Internal 50 Ω input termination
- Internal 50 Ω output load resistors
- Available in die or 16-pin (3mm \times 3mm) MLF package

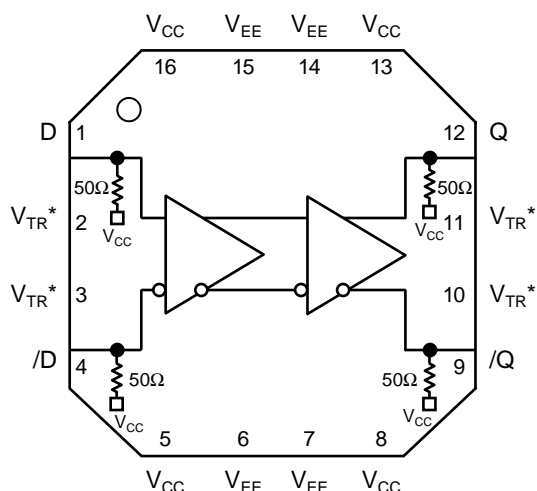
DESCRIPTION

The SY58016L is a high-speed, current mode logic (CML) differential receiver. It is ideal for interfacing with high frequency sources. It can be used as Line Receiver, Line Driver and Limiting Amplifier. The device can be operated from DC to 10Gbps. The input incorporates internal termination resistors, and directly interfaces to a CML logic signal. The output is CML compatible, and includes 50 Ω load resistors.

APPLICATIONS

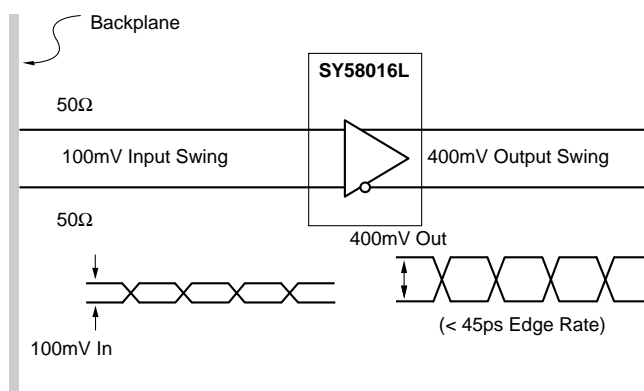
- Backplane buffering
- OC-3/OC-192 SONET clock or data distribution/driver
- All GigE clock or data distribution/driver
- Fibre Channel distribution/driver

FUNCTIONAL BLOCK DIAGRAM

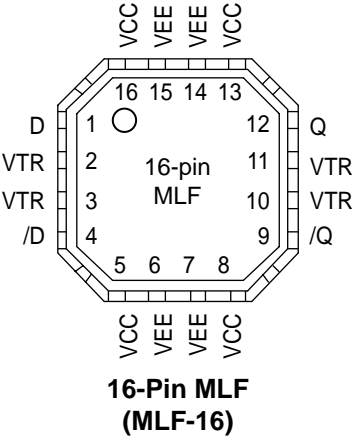


*V_{TR} is not connected to the DIE.

TYPICAL PERFORMANCE



PACKAGE/ORDERING INFORMATION



Ordering Information

| Part Number | Package Type | Operating Range | Package Marking |
|---------------|--------------|-----------------|-----------------|
| SY58016LXC | DIE | 25°C | — |
| SY58016LMI | MLF-16 | Industrial | 016L |
| SY58016LMITR* | MLF-16 | Industrial | 016L |

*Tape and Reel

PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|-----------------------------|----------|---|
| 1, 4 | D, /D | CML, PECL Differential Inputs with internal 50Ω pull-up resistors. |
| 2, 3, 10, 11 | VTR | Transmission Line Return: Normally connected to the most positive supply. |
| 6, 7, 14, 15 Exposed pad | VEE | Most Negative Supply. Exposed pad to be at the same electrical potential as VEE pins. |
| 12, 9 | Q, /Q | CML Differential Outputs with internal 50Ω pull-up resistors. |
| 5, 8, 13, 16 | VCC | Positive Power Supply: +3.3V nominal. |

Absolute Maximum Ratings(Note 1)

| | |
|---|----------------------|
| Supply Voltage $ V_{CC} - V_{EE} $ | +4.0V |
| Output Voltage (V_{OUT}) | Max. $V_{CC} + 0.5V$ |
| | Min. $V_{CC} - 1.0V$ |
| Maximum Input Current (I_{IN}) | $\pm 25mA$ |
| Maximum Output Current (I_{OUT}) | $\pm 25mA$ |
| Lead Temperature (Soldering, 10 sec.) | 220°C |

Operating Ratings(Note 2)

| | |
|---------------------------------------|------------------------------------|
| Supply Voltage (V_{IN}) | |
| Input Voltage ($V_{CC} = 0V$) | -1.0V to +0.5V |
| Input Voltage ($V_{EE} = 0V$) | $V_{CC} - 1.0V$ to $V_{CC} + 0.5V$ |
| Ambient Temperature (T_A) | -40°C to +85°C |
| Storage Temperature (T_S) | -65°C to +150°C |
| Package Thermal Resistance | |
| MLF (θ_{JA}) | |
| Still Air | 60°C/W |
| 500lfpm | 54°C/W |
| MLF (Ψ_{JB})(Note 4) | 32°C/W |

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. The device is guaranteed to meet the DC specifications, shown in the table above, after thermal equilibrium has been established. The device is tested in a socket such that transverse airflow of ≥ 500 lfpm is maintained.

Note 4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = GND$, $V_{CC} = +3.3V \pm 10\%$

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------|-------------------------|---------------|------------------|------------------|------------------|----------|
| I_{EE} | Power Supply Current | | — | 50 | 75 | mA |
| R_{IN} | Input Resistance | | 40 | 50 | 60 | Ω |
| R_{OUT} | Output Source Impedance | | 40 | 50 | 60 | Ω |
| V_{IH} | Input HIGH Voltage | | $V_{CC} - 0.9$ | — | V_{CC} | V |
| V_{IL} | Input LOW Voltage | | $V_{CC} - 1.0$ | — | $V_{CC} - 0.1$ | V |
| V_{OH} | Output HIGH Voltage | Note 1 | $V_{CC} - 0.040$ | $V_{CC} - 0.010$ | V_{CC} | V |
| V_{OL} | Output LOW Voltage | Note 1 | — | $V_{CC} - 0.400$ | $V_{CC} - 0.325$ | V |
| $V_{OUT(swing)}$ | Output Voltage Swing | Note 1 | 325 | 400 | — | mVp-p |

Note 1. 50 Ω output load and input swing is more than 100mVp-p. See Figure 1 for Output Swing definition.

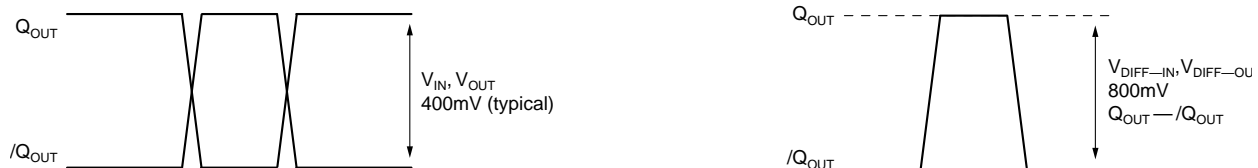


Figure 1. Input/Output Swing

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = \text{GND}$, $V_{CC} = +3.3\text{V} \pm 10\%$

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------------------------------|--|---------------|------|-----|-----|-----------|
| f_{MAX} | Maximum Data Rate | | 10.7 | — | — | Gbps |
| t_{PLH} t_{PHL} | Propagation Delay | | — | 100 | 150 | ps |
| t_{JITTER} | Random Jitter | Note 1 | — | — | 1.5 | ps(rms) |
| | Deterministic Jitter | Note 2 | — | — | 15 | ps(pk-pk) |
| V_{IN} | Minimum Input Swing | Note 3 | 100 | — | — | mVp-p |
| t_r , t_f | Output Rise/Fall Times (20% to 80%) | Note 4 | — | 30 | 45 | ps |

Note 1. Measured with a K28.7 comma detect character pattern, measured at 10Gbps. See "Figure 2. Eye Diagram."

Note 2. Measured with a K28.5 pattern $2^{23}-1$ PRBS pattern at 10Gbps.

Note 3. Minimum input swing for which AC parameters are guaranteed. See Figure 1. Reduced input swing will impact maximum data rate and the resulting eye pattern.

Note 4. 50Ω load and input swing is more than 100mVp-p.

EYE DIAGRAM

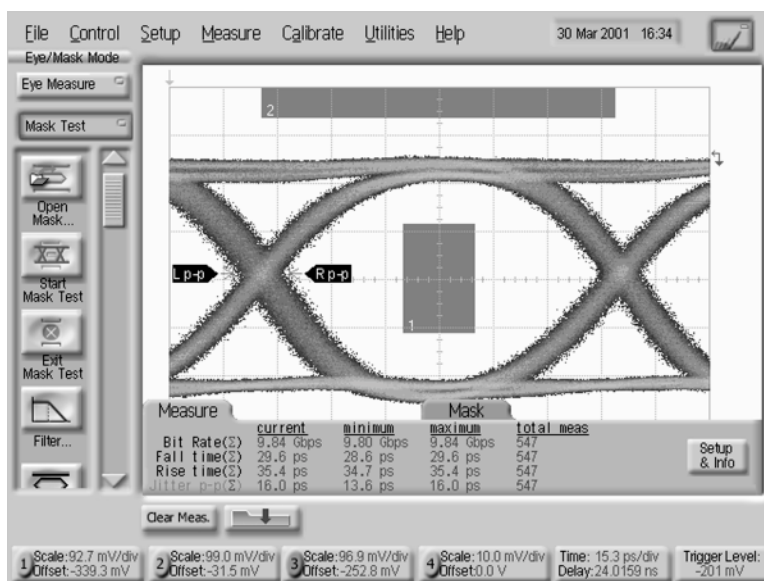
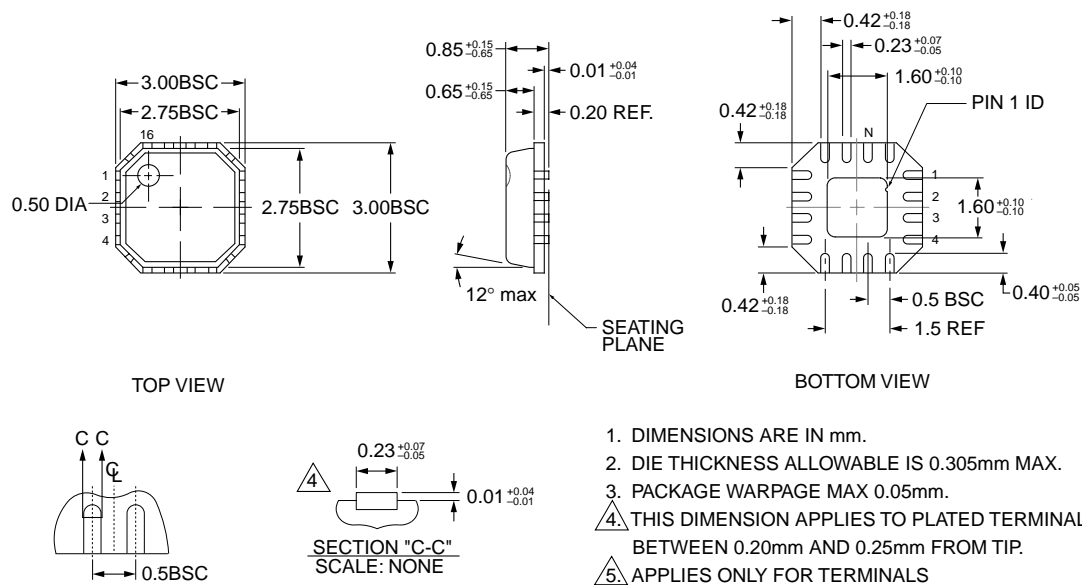


Figure 2. Eye Diagram

16 LEAD *MicroLeadFrame*[™] (MLF-16)



1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification and is shipped in Dry-pack form.
2. Expose pad must be soldered to a ground for proper thermal management.

Rev. 02

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