3.3V, 2.5Gbps ANY INPUT-to-LVPECL DUAL TRANSLATOR

SuperLite™ SY55857L

FEATURES

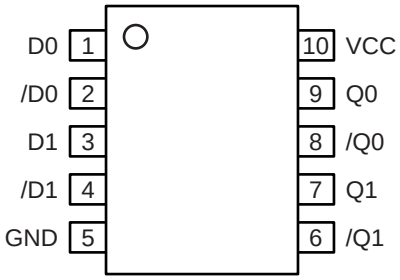
- **Input accepts virtually all logic standards**
  - **Single-ended: SSTL, TTL, CMOS**
  - **Differential: LVDS, HSTL, CML**
- **Guaranteed AC parameters over temperature:**
  - **f_{MAX} > 2.5Gbps (2.5GHz toggle)**
  - **t_r / t_f < 200ps**
  - **Within-device skew < 50ps**
  - **Propagation delay < 400ps**
- **Low power: 46mW/channel (typ)**
- **3.0V to 3.6V power supply**
- **100K LVPECL outputs**
- **Flow-through pinout and fully differential design**
- **Two channels in a 10-pin (3mm × 3mm) MSOP package**

SuperLite™

DESCRIPTION

The SY55857L is a fully differential, high-speed dual translator optimized to accept any logic standard from single-ended TTL/CMOS to differential LVDS, HSTL, or CML and translate it to LVPECL. Translation is guaranteed for speeds up to 2.5Gbps (2.5GHz toggle frequency). The SY55857L does not internally terminate its inputs, as different interfacing standards have different termination requirements. Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

PIN CONFIGURATION

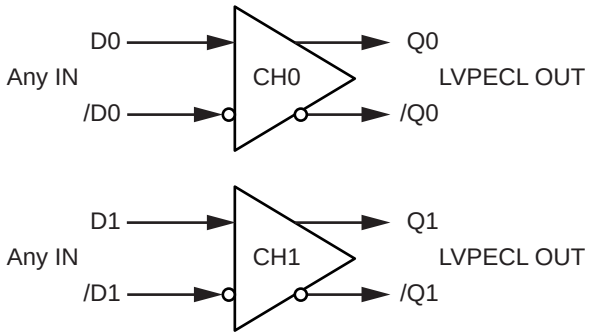


10-Pin MSOP (K10-1)

APPLICATIONS

- **High-speed logic**
- **Data communications systems**
- **Wireless communications systems**
- **Telecom systems**

FUNCTIONAL BLOCK DIAGRAM



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Rev.: B Amendment: /0
Issue Date: Sept. 2003

PIN DESCRIPTIONS

Pin Number	Pin Name	Description
D0, /D0	1, 2	Channel 0 differential inputs (clock or data). See Figure 1 for input structure. See *"Input Interface"* section for typical interface recommendations.
D1, /D1	3, 4	Channel 1 differential inputs (clock or data). See Figure 1 for input structure. See *"Input Interface"* section for typical interface recommendations.
Q0, /Q0	9, 8	Channel 0 differential 100k compatible LVPECL outputs. Terminate to V_{CC} – 2V. See *"LVPECL Output Termination"* section. Outputs are low impedance, emitter-followers. For AC-coupled applications, a pull-down resistor is required on Q and /Q to ensure a DC current path to GND.
Q1, /Q1	7, 6	Channel 1 differential 100k compatible LVPECL outputs. Terminate to V_{CC} – 2V. See *"LVPECL Output Termination"* section. Outputs are low impedance, emitter-followers. For AC-coupled applications, a pull-down resistor is required on Q and /Q to ensure a DC current path to GND.
GND	5	Device ground. Typically connected to Logic ground.
V_{CC}	10	Supply Voltage. Typically connect to +3.3V ± 10% supply. Bypass with 0.01μF//0.1μF low ESR capacitors.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

Do not leave unused inputs floating. Tie either the true or complement inputs to ground, but not both. A logic zero is achieved by connecting the complement input to ground with the true input floating. For a TTL input, tie a 2.5kΩ resistor between the complement input and ground. See *"Input Interface"* section.

Input Levels

LVDS, CML and HSTL differential signals may be connected directly to the D inputs. Depending on the actual worst case voltage seen, performance of SY55857L varies as per the following table:

Input Voltage Range	Minimum Voltage Swing	Maximum Translation Speed
0 to 2.4V	100mV	2.5Gbps
0 to V_{CC} +0.3	200mV	1.25Gbps

For LVDS applications, only point-to-point interfaces are supported. Due to the current required by the input structure shown in Figure 1, mutlidrop and multipoint architectures are not supported.

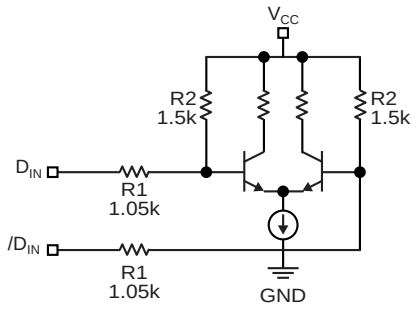


Figure 1. Simplified Input Structure

Absolute Maximum Ratings(Note 1)

Power Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.5V
Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Lead Temperature (soldering, 10 sec.) ..... +220°C
Storage Temperature Range (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Power Supply Voltage (V_{CC}) ..... 3.0V to 3.6V
Ambient Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance
  MSOP (θ_{JA})
    Still-Air ..... 113°C/W
    500lpfm ..... 96°C/W
  MSOP (θ_{JC})
    Junction-to-Case ..... 42°C/W

DC ELECTRICAL CHARACTERISTICS(Note 3)

T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	
I_{CC}	Power Supply Current	—	28	45	mA	Inputs/Outputs Open

INPUT ELECTRICAL CHARACTERISTICS(Note 3)

V_{CC} = 3.0V to 3.6V; GND = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{ID}	Input Voltage Swing	100	—	—	mV	See Figure 2a, $V_{IN} < 2.4V$
		200	—	—	mV	$V_{IN} < V_{CC}$+0.3V
V_{IH}	Input HIGH Voltage	—	—	V_{CC}+0.3V	V	
V_{IL}	Input LOW Voltage	–0.3	—	—	V	

(100k) LVPECL OUTPUT CHARACTERISTICS(Note 4)

V_{CC} = 3.0V to 3.6V; GND = 0V; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{OL}	Output LOW Voltage	1355	1480	1605	mV	
V_{OH}	Output HIGH Voltage	2155	2280	2405	mV	
V_{DIFF_OUT}	Differential Output Voltage Swing	600	700	—	mV_{p-p}	See Figure 2b

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. The specifications shown are valid after thermal equilibrium has been established.

Note 4. 100k circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters are at V_{CC} = 3.3V. They vary 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10%; T_A= –40°C to +85°C; R_L = 50Ω to V_{CC} –2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency **Note 5**	V_{IN} < 2.4V NRZ Data	2.5			Gbps
		V_{IN} < 2.4V Clock	2.5			GHz
		V_{IN} < V_{CC} +0.3V NRZ Data	1.25			Gbps
		V_{IN} < V_{CC} +0.3V Clock	1.25			GHz
t_{pd}	Propagation Delay D-to-Q				400	ps
t_{SKEW}	Within-Device-Skew (Differential)	**Note 6**			50	ps
	Part-to-Part Skew (Differential)	**Note 7**			200	ps
t_{JITTER}	Random Jitter (RJ)	**Note 8**			1	ps(rms)
	Deterministic Jitter (DJ)	**Note 9**			10	ps(pk-pk)
	Total Jitter (TJ)	**Note 10**		1	10	ps(pk-pk)
t_r, t_f	Output Rise/Fall Time 20% to 80%	At full output swing			200	ps

Note 5. Clock frequency is defined as the maximum toggle frequency, and guaranteed for functionality only. Measured with a 750mV signal, 50% duty cycle. High -frequency AC-parameters are guaranteed by design and characterization.

Note 6. Within-device skew is measured between two different outputs under identical transitions.

Note 7. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

Note 8. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps.

Note 9. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}–1 PRBS pattern.

Note 10. Total jitter definition: With an ideal differential clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

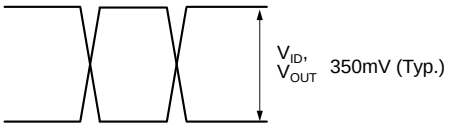


Figure 2a. Single-Ended Voltage Swing

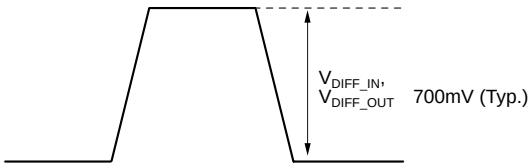


Figure 2b. Differential Voltage Swing

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Package Marking
SY55857LKI	K10-1	Industrial	857L
SY55857LKITR(Note 1)	K10-1	Industrial	857L

Note 1. Tape and Reel.

INPUT INTERFACE

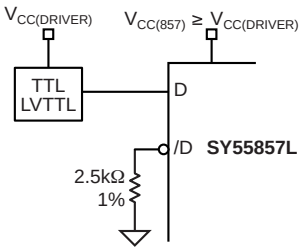


Figure 3. 5V, 3.3V "TTL"

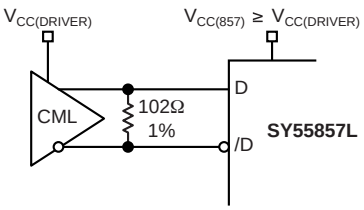


Figure 4. CML-DC Coupled

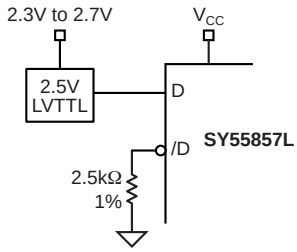


Figure 5. 2.5V "TTL"

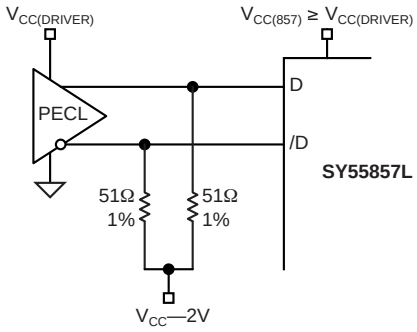


Figure 6. PECL-DC Coupled

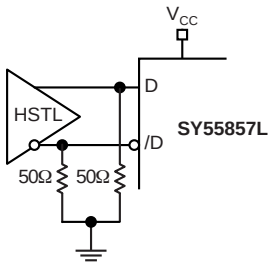


Figure 7. HSTL

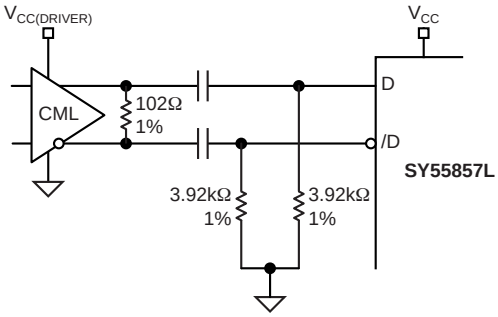


Figure 8. CML-AC Coupled Short Lines

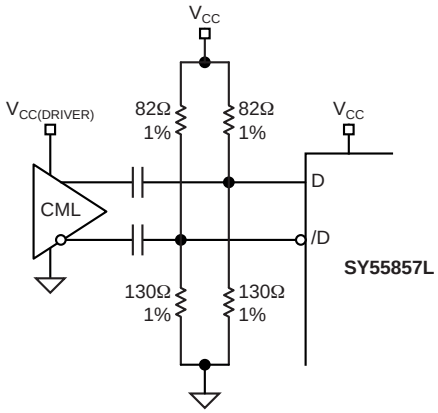


Figure 9. CML-AC Coupled Long Lines

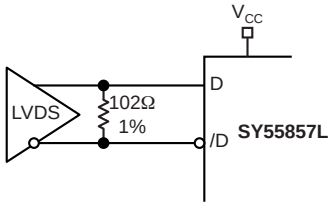


Figure 10. LVDS

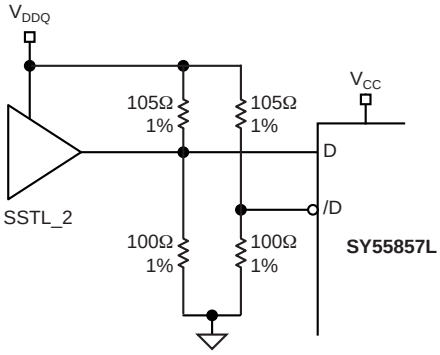


Figure 11. SSTL_2

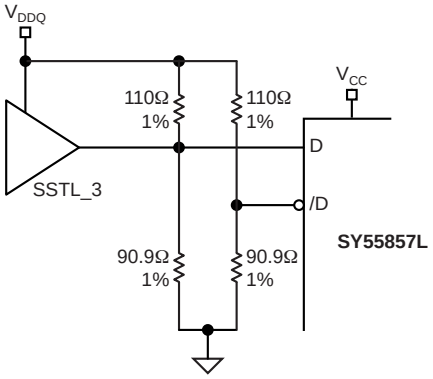
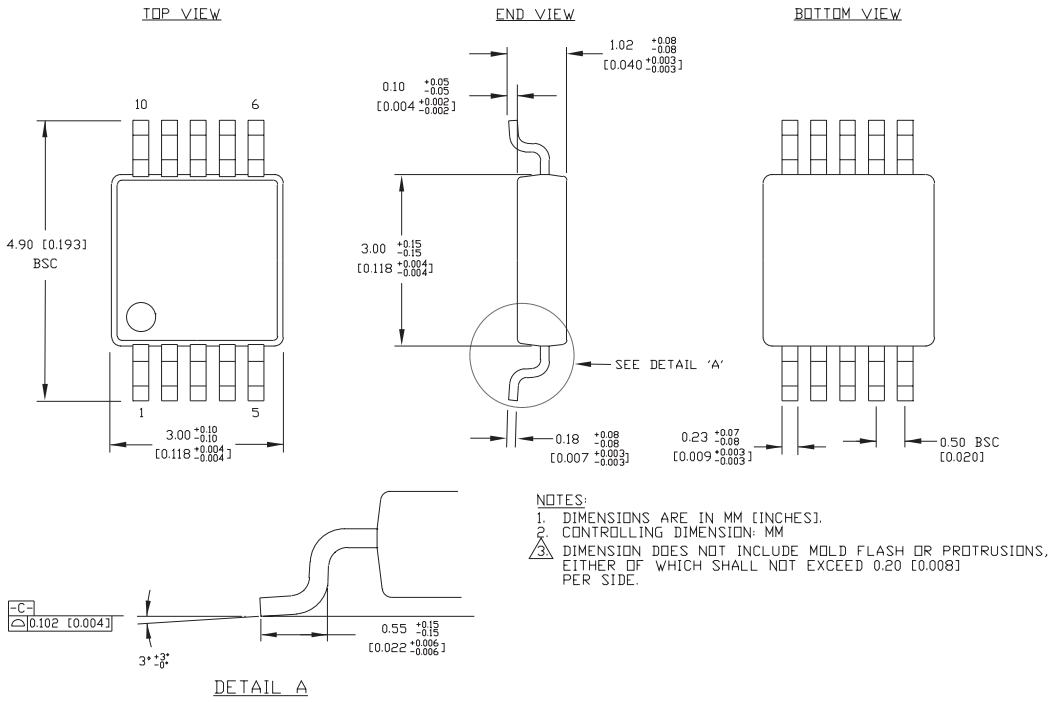


Figure 12. SSTL_3

10 LEAD MSOP (K10-1)



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