

## FEATURES

- Guaranteed  $f_{MAX} > 2.5\text{GHz}$  over temperature
- 2.3V to 5.7V power supply
- Non-blocking “switch architecture”
- Guaranteed  $<15\text{ps}$  channel-to-channel skew
- Guaranteed  $<480\text{ps}$  propagation delay over temperature
- Configurable as 2:1 mux, 1:2 fan-out buffer, dual buffer, or 2 x 2 switch
- Accepts CML, PECL, LVPECL inputs
- Fully differential inputs/outputs
- Source terminated CML outputs for fast edge rates
- Wide operating temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Available in a tiny 16-pin EPAD-QSOP package



SuperLite™

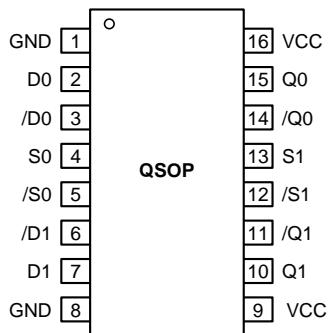
## DESCRIPTION

The SY55854U is a fully differential, CML, 2 x 2-crosspoint switch. The non-blocking design allows any input to be connected to any output. Varying the state of the select inputs allows SY55854U to be used in backup, fault tolerant, protection, and backplane distribution applications.

SY55854U inputs can be terminated with a single resistor between the true and the complement pins of a given input.

The SY55854U is a member of Micrel's new SuperLite™ family of high-speed logic devices. This family features very small packaging, high signal integrity, and flexible supply voltage operation.

## PIN CONFIGURATION

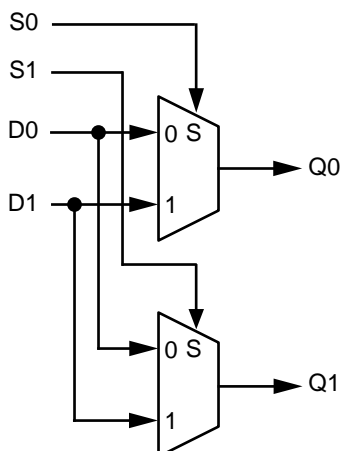


16-Pin QSOP

## APPLICATIONS

- High-speed logic
- Data communications systems
- Wireless communications systems
- Telecom systems
- Backplane redundancy

## FUNCTIONAL BLOCK DIAGRAM



## PIN NAMES

Pin	Function
D0, /D0	CML/PECL/LVPECL Input Data
D1, /D1	CML/PECL/LVPECL Input Data
Q0, /Q0	CML Output Data
Q1, /Q1	CML Output Data
S0, /S0	CML/PECL/LVPECL Select Input
S1, /S1	CML/PECL/LVPECL Select Input
GND	Ground
V <sub>CC</sub>	V <sub>CC</sub>

## PIN DESCRIPTIONS

### D0, /D0 – CML/PECL/LVPECL Input (Differential)

This is one of the data inputs to the crosspoint. It will be switched either to the Q0 output, the Q1 output, both outputs, or neither output, depending on the state of the S0 and S1 inputs.

### D1, /D1 – CML/PECL/LVPECL Input (Differential)

This is the other data input to the crosspoint. It will be switched either to the Q0 output, the Q1 output, both outputs, or neither output, depending on the state of the S0 and S1 inputs.

### Q0, /Q0 – CML Output (Differential)

This is one output from the crosspoint. Input S0 selects either the D0 or the D1 input to be switched to this output.

### Q1, /Q1 – CML Output (Differential)

This is the other output from the crosspoint. Input S1 selects either the D0 or D1 input to be switched to this output.

### S0, /S0 – CML/PECL/LVPECL Input (Differential)

This select input chooses which data input switches to the Q0 output. S0 logic low selects the D0 input, while S0 logic high selects the D1 input.

### S1, /S1 – CML/PECL/LVPECL Input (Differential)

This select input chooses which data input switches to the Q1 output. S1 logic low selects the D0 input, while S1 logic high selects the D1 input.

## FUNCTIONAL DESCRIPTION

### Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased halfway between  $V_{CC}$  and ground by a voltage divider consisting of two 75kΩ resistors. In this way, unconnected inputs appear as logic zeros. To keep an

input at static logic zero at  $V_{CC} > 3.0V$ , leave both inputs unconnected. For  $V_{CC} \leq 3.0V$ , connect the complement input to  $V_{CC}$  and leave the true input unconnected. To make an input static logic one, connect the true input to  $V_{CC}$ , leave the complement input unconnected. These are the only two safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (no connect) pins should be unconnected.

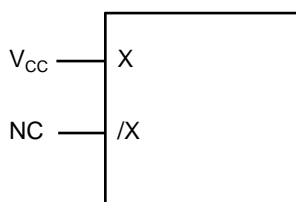


Figure 1. Hard Wiring a Logic “1” (1)

**Note 1.** X is either D0, D1, S0, or S1 input. /X is either /D0, /D1, /S0, or /S1 input.

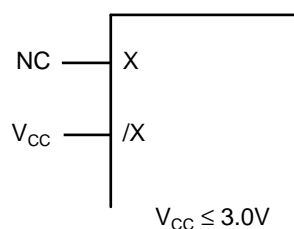
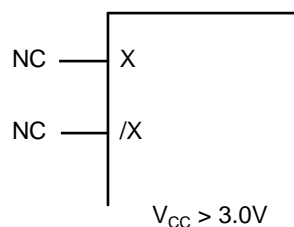


Figure 2. Hard Wiring a Logic “0” (1)

### Usage

SY55854U is very versatile. Tying its select inputs in various ways varies its functionality. For example, tying the select inputs together turns SY55854U into a redundant distributor. Either input will be switched to both outputs simultaneously. This is very useful in redundant backplane applications. By cross-tying the select inputs, SY55854U becomes a true crosspoint, selecting between “straight

through” and “cross connected” operation. Also, using the select inputs independently, SY55854U functions as two multiplexers. Setting the select inputs to static values turns SY55854U into a dual buffer, or a fan-out buffer.

To make larger crosspoints, cascade SY55854U devices, either in a tree or in a Banyan structure, as appropriate for your application.

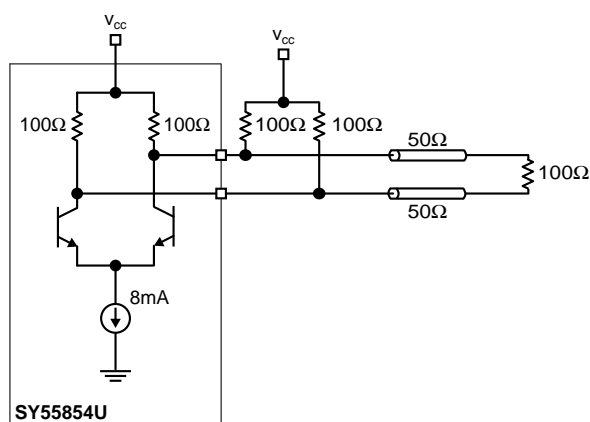
## TRUTH TABLE

S0	S1	Q0	Q1	Function
0	0	D0	D0	Fan-Out Buffer
0	1	D0	D1	Dual Buffer
1	0	D1	D0	Dual Buffer
1	1	D1	D1	Fan-Out Buffer
CTL	CTL	Same	Same	Redundant Distribution
CTL	/CTL	Opposite	Opposite	Crosspoint

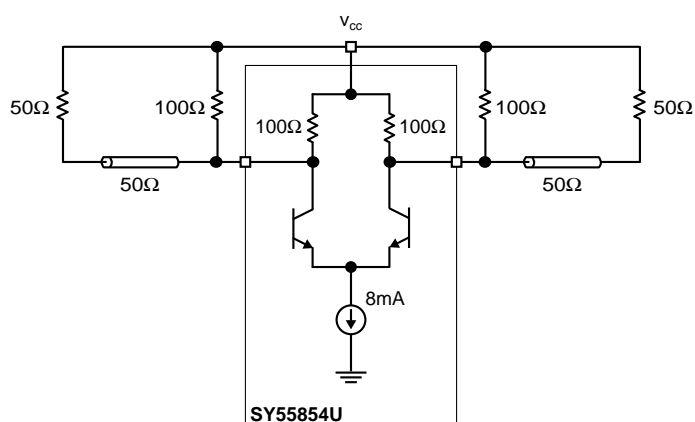
## CML TERMINATION

All inputs accept the output from any other member of this family. All outputs are source terminated 100Ω CML differential drivers as shown in Figures 3 and 4. SY55854U expects the inputs to be terminated, and that good high

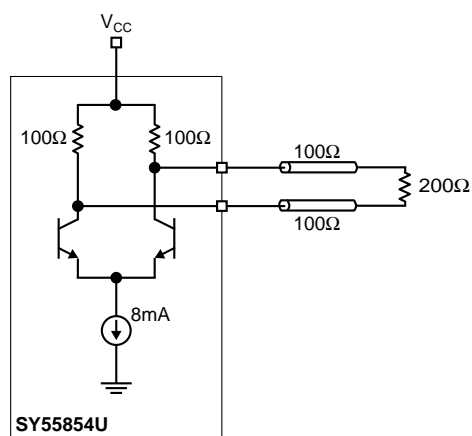
speed design practices be adhered to. SY55854U inputs are designed to accept a termination resistor between the true and complement inputs of a differential pair. 0402 form factor chip resistors will fit with some trace fanout.



**Figure 3a. Differentially Terminated  
(50Ω Load CML Output)**



**Figure 3b. Individually Terminated  
(50Ω Load CML Output)**



**Figure 4. 100Ω Load CML Output**

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Value	Unit
$V_{CC}$	Power Supply Voltage	-0.5 to +6.0	V
$V_I$	Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	CML Output Voltage	$V_{CC} - 1.0$ to $V_{CC} + 0.5$	V
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{store}$	Storage Temperature Range	-65 to +150	°C

**Note 1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

$V_{CC} = 2.3V$  to  $5.7V$ ;  $GND = 0V$

Symbol	Parameter	$T_A = -40^\circ C$		$T_A = 0^\circ C$		$T_A = +25^\circ C$		$T_A = +85^\circ C$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{CC}$	Power Supply Voltage	2.3	5.7	2.3	5.7	2.3	5.7	2.3	5.7	V
$I_{CC}$	Power Supply Current	—	60	—	60	—	60	—	60	mA

**Note 1.** Specification for packaged product only.

**CML DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

$V_{CC} = 2.3V$  to  $5.7V$ ;  $GND = 0V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ <sup>(2)</sup>

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$V_{ID}$	Differential Input Voltage	100	—	—	mV	
$V_{IH}$	Input HIGH Voltage	1.6	—	$V_{CC}$	V	
$V_{IL}$	Input LOW Voltage	1.5	—	$V_{CC} - 0.1$	V	
$V_{OH}$	Output HIGH Voltage	$V_{CC} - 0.020$	$V_{CC} - 0.010$	$V_{CC}$	V	No Load
$V_{OL}$	Output LOW Voltage	$V_{CC} - 0.97$	$V_{CC} - 0.825$	$V_{CC} - 0.660$	V	No Load
$V_{OS}$	Output Voltage Swing <sup>(3)</sup>	0.700	0.800 0.400 0.200	0.950	V	No Load 100Ω Environment <sup>(5)</sup> 50Ω Environment <sup>(4)</sup>
$R_{DRIVE}$	Output Source Impedance	80	100	120	Ω	

**Note 1.** Specification for packaged product only.

**Note 2.** Equilibrium temperature.

**Note 3.** Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in the 100Ω environment and a 200mV swing in the 50Ω environment. Refer to the "CML Termination" diagram for more details.

**Note 4.** See Figure 3a and 3b.

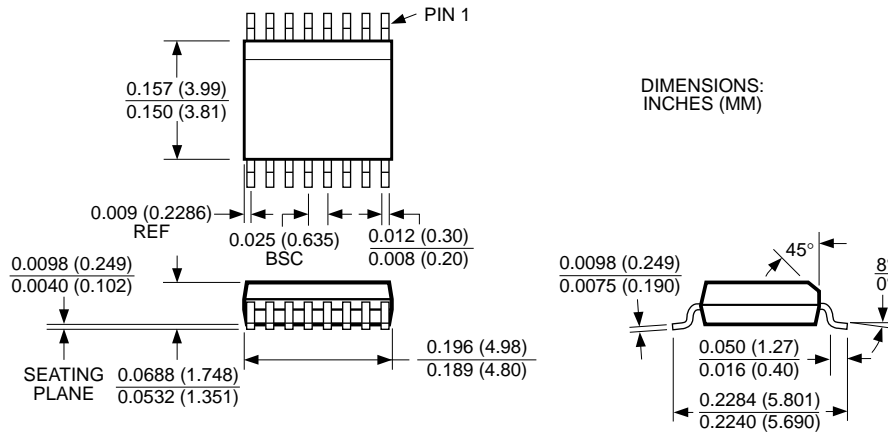
**Note 5.** See Figure 4.

**AC ELECTRICAL CHARACTERISTICS<sup>(1, 2)</sup>** $V_{CC} = 2.3V$  to  $5.7V$ ;  $GND = 0V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ 

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
$f_{MAX}$	Max. Operating Frequency	2.5	—	—	GHz	
$t_{PLH}$ $t_{PHL}$	Propagation Delay, S0, S1, D0, D1 to Q0, Q1	—	—	400	ps	
$t_{SKEW}$	Within-Device Skew <sup>(3)</sup> Part-to-Part Skew (Diff.)	— —	— —	15 100	ps	
$t_r$ $t_f$	CML Output Rise/Fall Times (20% to 80%)	—	—	150	ps	

**Note 1.** Specification for packaged product only.**Note 2.** Tested using environment of Figure 3b, 50Ω load CML output.**Note 3.** Worst case difference between Q0 and Q1 from either A or B, when both outputs come from the same input**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range	Package Marking
SY55854UYI	Y16-1	Industrial	854U
SY55854UYITR	Y16-1	Industrial	854U

**16 LEAD EPAD-QSOP (Y16-1)****MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA**TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB <http://www.micrel.com>

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