MICREL

The Infinite Bandwidth Company™

D LATCH

SuperLite™
SY55853U
FINAL

FEATURES

- ■ **2.5GHz min f$_{max}$**
- ■ **2.3V to 5.7V power supply**
- ■ **Single bit latch**
- ■ **Stores or flows through 1 bit of data**
- ■ **Optimized to work with SuperLite™ family**
- ■ **Fully differential**
- ■ **Source terminated CML outputs for fast edge rates**
- ■ **Accepts CML, PECL, LVPECL input logic levels**
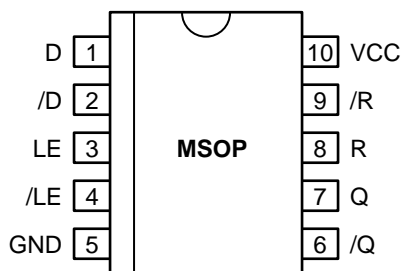- ■ **Available in a tiny 10-pin MSOP**

SuperLite™

DESCRIPTION

The SY55853U is a latch. Its differential output will flow through the input while it's enable is high. The output will remain static while the enable is low. In addition, an asynchronous, level sensitive reset is provided.

SY55853U inputs can be terminated with a single resistor between the true and the complement pins of a given input.

The SY55853U is a member of Micrel's SuperLite™ family of high-speed CML logic. This family features very small packaging and 2.3V to 5.7V operation.
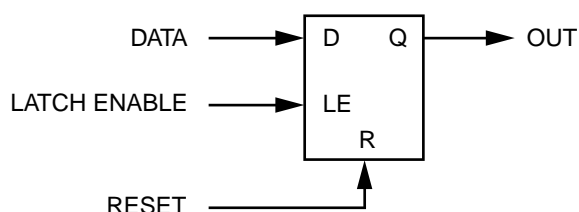
PIN CONFIGURATION

```
        ┌───────┐
 D    1 │       │ 10  VCC
/D    2 │       │  9  /R
LE    3 │ MSOP  │  8  R
/LE   4 │       │  7  Q
GND   5 │       │  6  /Q
        └───────┘
```

APPLICATIONS

- ■ **High-speed logic**
- ■ **OC-48 communication systems**

FUNCTIONAL BLOCK DIAGRAM

```
DATA ──────────▶│ D    Q │──────▶ OUT

LATCH ENABLE ──▶│ LE     │
                │     R  │
RESET ─────────▶│   ▲    │
```

PIN NAMES

Pin	Function
D, /D	CML/PECL/LVPECL Data Input
LE, /LE	CML/PECL/LVPECL Latch Enable Input
R, /R	CML/PECL/LVPECL Reset Input
Q, /Q	Data Output
GND	Ground
V$_{CC}$	V$_{CC}$

SuperLite is a trademark of Micrel, Inc.

PIN DESCRIPTIONS

D, /D – CML/PECL/LVPECL Input (Differential)

This is the single bit of data that gets latched.

LE, /LE – CML/PECL/LVPECL Input (Differential)

A high on this input causes the D, /D input to flow through to the Q, /Q output. A low on the input causes the Q, /Q output to remain static, except for a possible reset.

R, /R – CML/PECL/LVPECL Input (Differential)

This is an asynchronous active high level reset, that forces the latch into a known state, namely zero. It has priority over the LE, /LE input.

Q, /Q – CML Output (Differential)

This is the output of the latch.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased halfway between V_{CC} and ground by a voltage divider consisting of two 75kΩ resistors. To keep an input at static logic zero at $V_{CC} > 3.0V$, leave both inputs unconnected. For $V_{CC} \leq 3.0V$, connect the complement input to V_{CC} and leave the true input unconnected. To make an input static logic one, connect the true input to V_{CC}, leave the complement input unconnected. These are the only ;safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (no connect) pins should be unconnected.
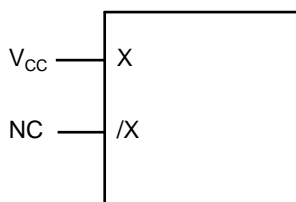

Figure 1. Hard Wiring A Logic "1" [1]

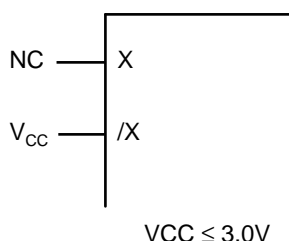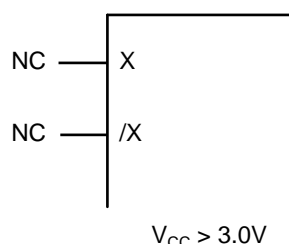**Note 1.** X is either D, LE, R input. /X is either /D, /LE, /R input.

$V_{CC} > 3.0V$

VCC ≤ 3.0V

Figure 2. Hard Wiring A Logic "0" [1]

TRUTH TABLE

D	LE	R	Q	/Q
X	0	0	Latched[1]	Latched[1]
0	1	0	0	1
1	1	0	1	0
X	X	1	0	1

Note 1. Retains data before LE falling transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	−0.5 to +6.0	V
V_{IN}	Input Voltage	−0.5 to V_{CC} +0.5	V
V_{OUT}	CML Output Voltage	V_{CC} −1.0 to V_{CC} +0.5	V
T_A	Operating Temperature Range	−40 to +85	°C
T_{store}	Storage Temperature Range	−65 to +150	°C

Note 1.   Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation
is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM
RATING conditions for extended periods may affect device reliability.

CML TERMINATION

All inputs accept the output from any other member of this family. All outputs are source terminated 100Ω CML differential drivers as shown in Figures 3 and 4. SY55853U expects the inputs to be terminated, and that good high speed design practices be adhered to. SY55853U inputs are designed to accept a termination resistor between the true and complement inputs of a differential pair. 0402 form factor chip resistors will fit with some trace fanout.
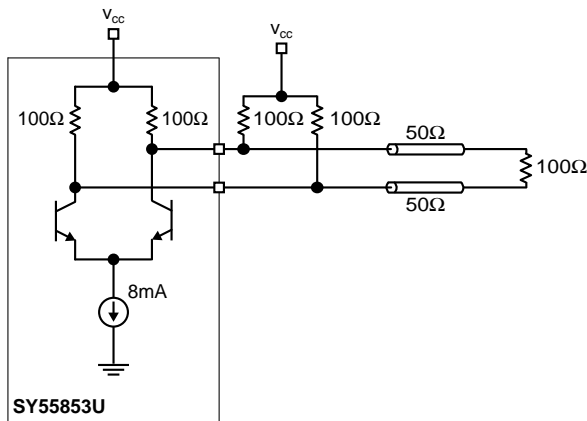
Figure 3a.   Differentially Terminated
(50Ω Load CML Output)
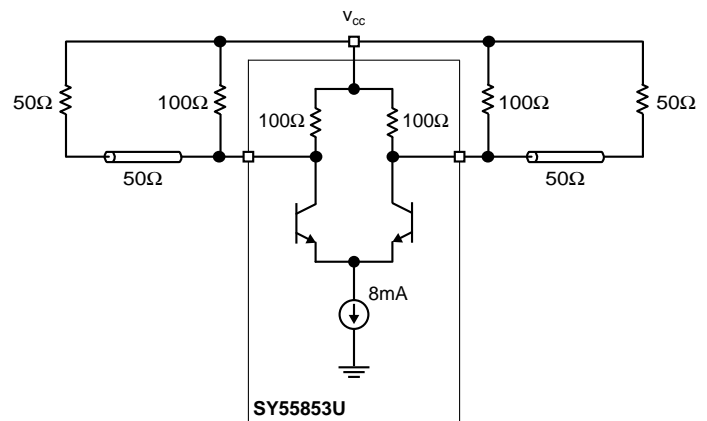
Figure 3b.   Individually Terminated
(50Ω Load CML Output)
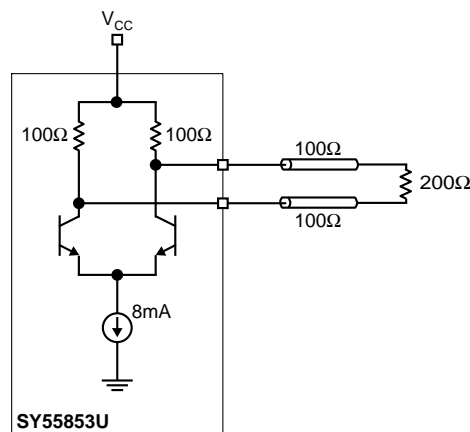
Figure 4.   100Ω Load CML Output

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 2.3V to 5.7V; GND = 0V

Symbol	Parameter	T_A = −40°C		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{CC}	Power Supply Voltage	2.3	5.7	2.3	5.7	2.3	5.7	2.3	5.7	V
I_{CC}	Power Supply Current	—	37	—	37	—	37	—	37	mA

Note 1. Specification for packaged product only.

CML DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = −40°C to +85°C[2]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{ID}	Differential Input Voltage	100	—	—	mV	
V_{IH}	Input HIGH Voltage[3]	1.6	—	V_{CC}	V	
V_{IL}	Input LOW Voltage[3]	1.5	—	$V_{CC} - 0.1$	V	
V_{OH}	Output HIGH Voltage	$V_{CC} - 0.020$	$V_{CC} - 0.010$	V_{CC}	V	No Load
V_{OL}	Output LOW Voltage	$V_{CC} - 0.97$	$V_{CC} - 0.825$	$V_{CC} - 0.660$	V	No Load
V_{OS}	Output Voltage Swing[4]	0.660	0.800 0.400 0.200	0.950	V	No Load 100Ω Environment[5] 50Ω Environment[6]
R_{DRIVE}	Output Source Impedance	80	100	120	Ω	

Note 1. Specification for packaged product only.

Note 2. Equilibrium temperature.

Note 3. Inputs Must be biased to logic LOW or HIGH when V_{CC} is less than 3.0V.

Note 4. Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in the 100Ω environment and a 200mV swing in the 50Ω environment. Refer to the "CML Termination" diagram for more details.

Note 5. See Figure 4.

Note 6. See Figure 3a and 3b.

AC ELECTRICAL CHARACTERISTICS[1, 2]

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = −40°C to +85°C

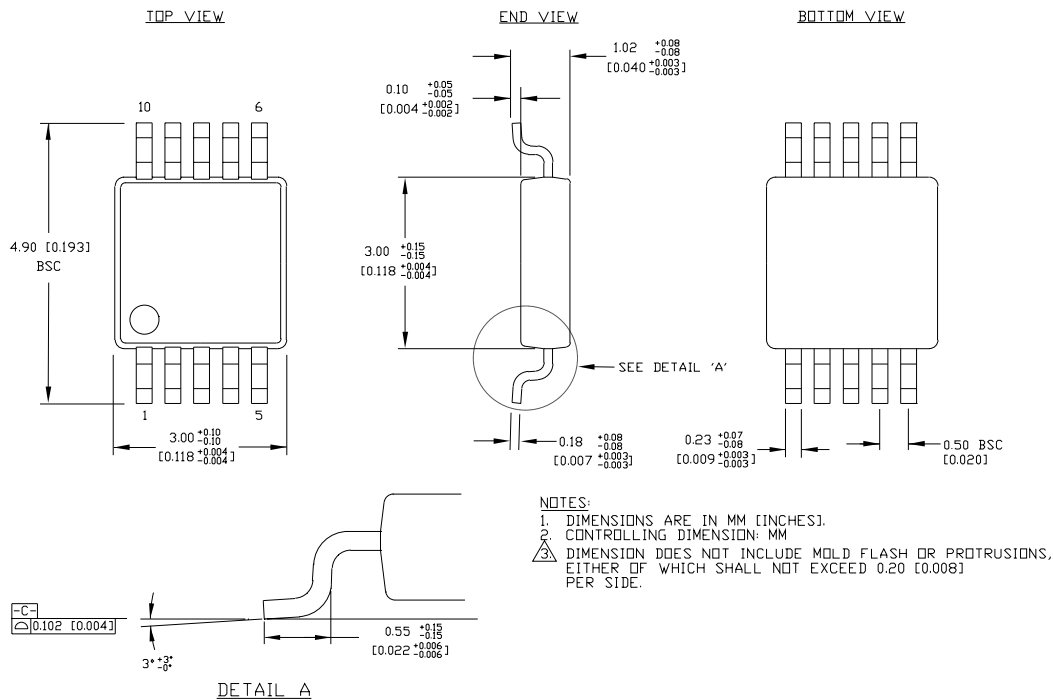| Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
f_{MAX}	Max. Operating Frequency		2.5	—	—	GHz	
t_{PLH} t_{PHL}	Propagation Delay	D to Q LE to Q R to Q	— — —	— — —	400 400 500	ps	
t_S	Set-Up Time	D to LE D to R	70 —	— —	— —	ps	
t_H	Hold Time	LE to D	40	—	—	ps	
t_{RR}	Reset Recovery		400	—	—	ps	
t_{PW}	Minimum Pulse Width	LE High R High	160 250	— —	— —	ps	
t_r t_f	CML Output Rise/Fall Times (20% to 80%)	−40°C to 0°C 0°C to 85°C	— 35	— —	175 160	ps	

Note 1. Specification for packaged product only.

Note 2. Tested using environment of Figure 3b, 50Ω load CML output.

TIMING DIAGRAMS
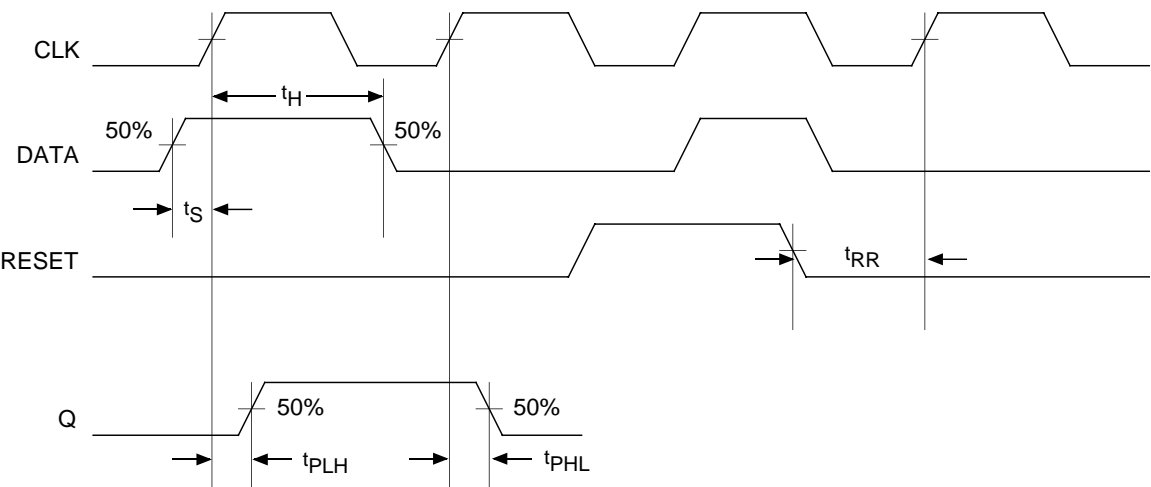
PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY55853UKC	K10-1	Commercial

10 LEAD MSOP (K10-1)

TOP VIEW

END VIEW

BOTTOM VIEW

10   6

4.90 [0.193]
BSC

1   5

3.00 $^{+0.10}_{-0.10}$
[0.118 $^{+0.004}_{-0.004}$]

1.02 $^{+0.08}_{-0.08}$
[0.040 $^{+0.003}_{-0.003}$]

0.10 $^{+0.05}_{-0.05}$
[0.004 $^{+0.002}_{-0.002}$]

3.00 $^{+0.15}_{-0.15}$
[0.118 $^{+0.004}_{-0.004}$]

SEE DETAIL 'A'

0.18 $^{+0.08}_{-0.08}$
[0.007 $^{+0.003}_{-0.003}$]

0.23 $^{+0.07}_{-0.08}$
[0.009 $^{+0.003}_{-0.003}$]

0.50 BSC
[0.020]

NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

-C-
0.102 [0.004]

3° $^{+3°}_{-0°}$

0.55 $^{+0.15}_{-0.15}$
[0.022 $^{+0.006}_{-0.006}$]

DETAIL A

Rev. 00