FEATURES

- 2.5GHz min. f_{MAX}
- 2.3V to 5.7V power supply
- Single bit register memory
- Synchronizes 1 bit of data to a clock
- Optimized to work with SuperLite™ family
- Fully differential
- Accepts CML, PECL, LVPECL input logic levels
- Source terminated CML outputs for fast edge rates
- Available in a tiny 10-pin MSOP

SuperLite™

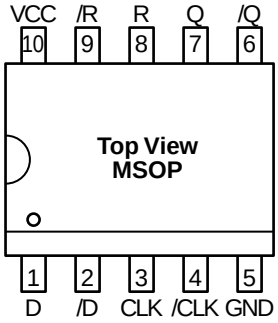
DESCRIPTION

The SY55852U is a flip-flop used to synchronize data to a clock. Its differential output will reproduce and remember the value on its input at the rising edge of the clock. In addition, an asynchronous, level sensitive reset is provided. For a synchonous reset, the SY55851U AnyGate™ can be used.

SY55852U inputs can be terminated with a single resistor between the true and complement pins of a given input.

The SY55852U is a member of Micrel's SuperLite™ family of high-speed CML logic. This family features very small packaging and 2.3V to 5.7V operation.

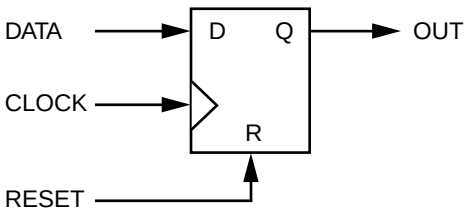
PIN CONFIGURATION



APPLICATIONS

- High-speed logic
- OC-48 communication systems

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

Pin	Function
D, /D	CML/PECL/LVPECL Data Input
CLK, /CLK	CML/PECL/LVPECL Clock Input
R, /R	CML/PECL/LVPECL Reset Input
Q, /Q	CML Data Output
GND	Ground
V_{CC}	V_{CC}

SuperLite is a trademark of Micrel, Inc.

PIN DESCRIPTIONS

D, /D – CML/PECL/LVPECL Input (Differential)

This is the single bit of data that gets clocked in and remembered.

CLK, /CLK – CML/PECL/LVPECL Input (Differential)

The rising edge of this signal is the clock signal that determines when the Boolean value at the data input gets stored.

R, /R – CML/PECL/LVPECL Input (Differential)

This is an asynchronous active high level reset, that forces the flip-flop into a known state, namely zero.

Q, /Q – CML Output (Differential)

This is the output of the flip-flop.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased halfway between V_{CC} and ground by a voltage divider consisting of two 75kΩ resistors. To keep an input at static logic zero at V_{CC} > 3.0V, leave both inputs unconnected. For $V_{CC} \leq 3.0V$, connect the complement inputs to V_{CC} and leave the true inputs unconnected. To make an input static logic one, connect the true input to V_{CC}, leave the complement input unconnected. These are the only safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (no connect) pins should be unconnected.

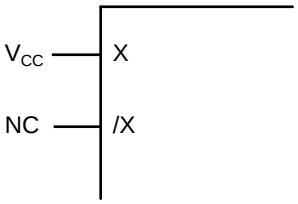
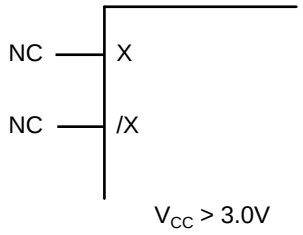


Figure 1. Hard Wiring a Logic "1" (1)

Note 1. X is either D, CLK, R input. /X is either /D, /CLK, /R input.



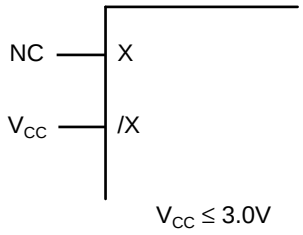


Figure 2. Hard Wiring a Logic "0" (1)

TRUTH TABLE

D	CLK	R	Q	/Q
X	X	1	0	1
X	0	0	Q_{N-1}	$/Q_{N-1}$
X	1	0	Q_{N-1}	$/Q_{N-1}$
0	↑	0	0	1
1	↑	0	1	0

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +6.0	V
V_{IN}	Input Voltage	–0.5 to V_{CC} +0.5	V
V_{OUT}	CML Output Voltage	V_{CC} –1.0 to V_{CC} +0.5	V
T_A	Operating Temperature Range	–40 to +85	°C
T_{store}	Storage Temperature Range	–65 to +150	°C

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

CML TERMINATION

All inputs accept the output from any other member of this family. All outputs are source terminated 100Ω CML differential drivers as shown in Figures 3 and 4. SY55852U expects the inputs to be terminated, and that good high speed design practices be adhered to. SY55852U inputs are designed to accept a termination resistor between the true and complement inputs of a differential pair. 0402 form factor chip resistors will fit with some trace fanout.

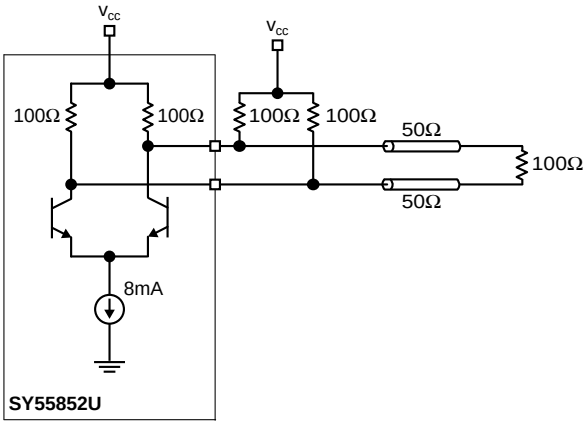


Figure 3a. Differentially Terminated (50Ω Load CML Output)

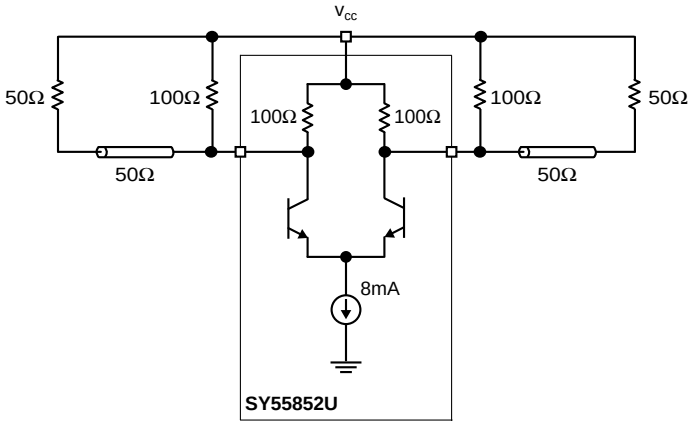


Figure 3b. Individually Terminated (50Ω Load CML Output)

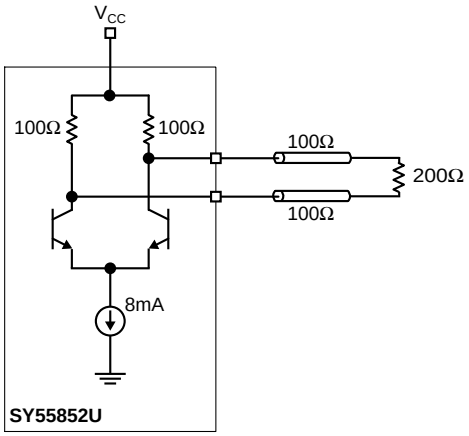


Figure 4. 100Ω Load CML Output

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 2.3V to 5.7V; GND = 0V

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{CC}	Power Supply Voltage	2.3	5.7	2.3	5.7	2.3	5.7	2.3	5.7	V
I_{CC}	Power Supply Current	—	36	—	36	—	36	—	36	mA

Note 1. Specification for packaged product only.

CML DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = –40°C to +85°C[2]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{ID}	Differential Input Voltage	100	—	—	mV	
V_{IH}	Input HIGH Voltage[6]	1.6	—	V_{CC}	V	
V_{IL}	Input LOW Voltage[6]	1.5	—	V_{CC} – 0.1	V	
V_{OH}	Output HIGH Voltage	V_{CC} – 0.020	V_{CC} – 0.010	V_{CC}	V	No Load
V_{OL}	Output LOW Voltage	V_{CC} – 0.97	V_{CC} – 0.825	V_{CC} – 0.660	V	No Load
V_{OS}	Output Voltage Swing[3]	0.660	0.800 0.400 0.200	0.950	V	No Load 100Ω Environment[5] 50Ω Environment[4]
R_{DRIVE}	Output Source Impedance	80	100	120	Ω	

Note 1. Specification for packaged product only.

Note 2. Equilibrium temperature.

Note 3. Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in the 100Ω environment and a 200mV swing in the 50Ω environment. Refer to the “CML Termination” diagram for more details.

Note 4. See Figure 3a and 3b.

Note 5. See Figure 4.

Note 6. Inputs must be biased to logic LOW or HIGH when V_{CC} is less than 3.0V.

AC ELECTRICAL CHARACTERISTICS[1]

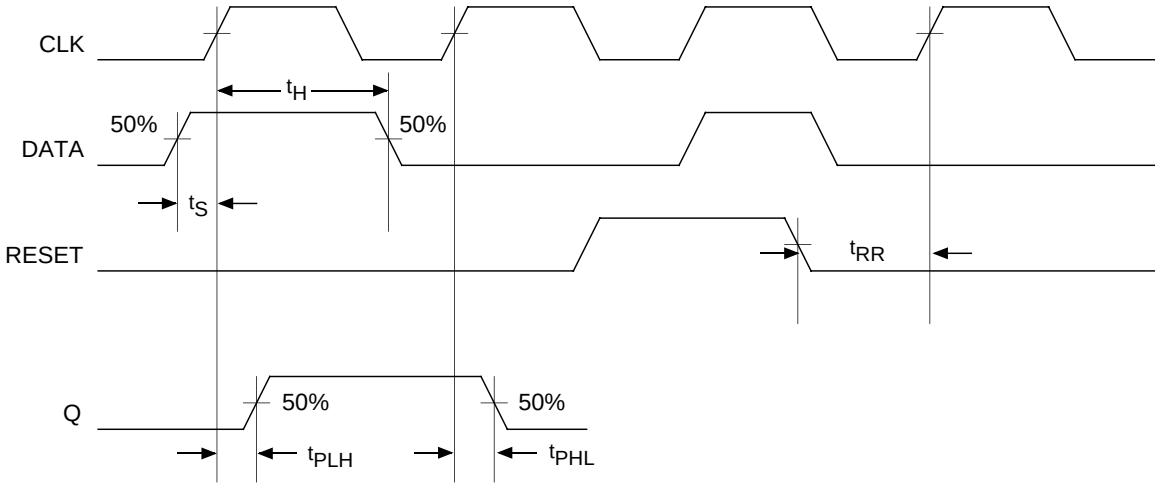
V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = –40°C to +85°C

Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition[2]
f_{MAX}	Max. Operating Frequency		2.5	—	—	GHz	
t_{PLH} t_{PHL}	Propagation Delay,	CLK to Q R to Q	— —	— —	400 500	ps	
t_S	Set-Up Time		40	—	—	ps	
t_H	Hold Time		40	—	—	ps	
t_{RR}	Reset Recovery		400	—	—	ps	
t_{PW}	Minimum Pulse Width CLK to Q R to Q	V_{CC} < 3V V_{CC} ≥ 3V	160 140 250	— — —	— — —	ps	
t_r t_f	CML Output Rise/Fall Times (20% to 80%)		35	—	150	ps	

Note 1. Specification for packaged product only.

Note 2. Tested using environment of Figure 3b, 50Ω load CML output.

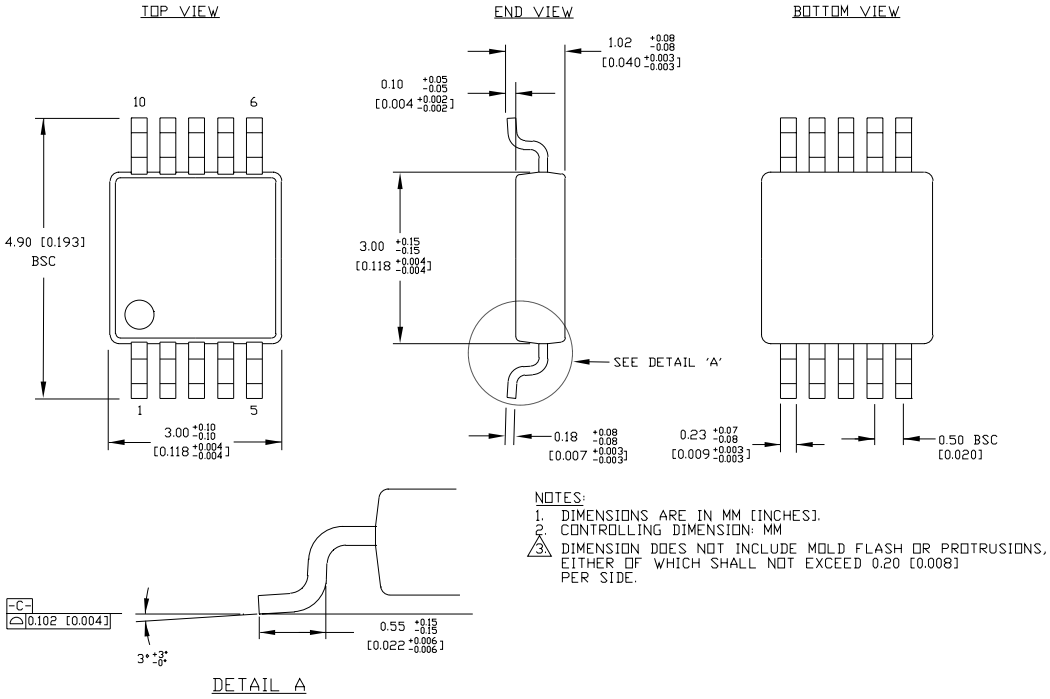
TIMING DIAGRAMS



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY55852UKC	K10-1	Commercial

10 LEAD MSOP (K10-1)



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