FEATURES

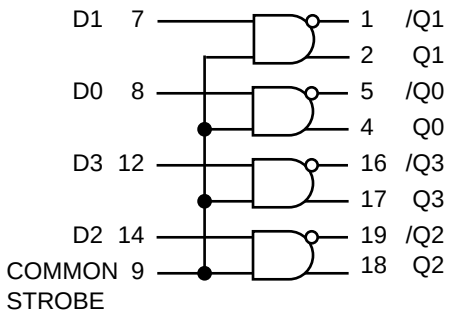
- **Single 5V power supply**
- **All V_{CC} pins isolated on chip**
- **Differentially drive balanced lines**
- **t_{pd} 1.3ns typical**
- **Fully compatible with ON Semiconductor MC10H352**
- **Available in 20-pin PLCC package**

DESCRIPTION

The SY10H352 is a quad translator for interfacing data between a CMOS logic section and the PECL section of digital systems when only a +5.0V VDC power supply is available. The SY10H352 has CMOS compatible inputs and PECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state (≈ +3.2V) and all inverting outputs to the PECL high logic state (≈ +4.1V).

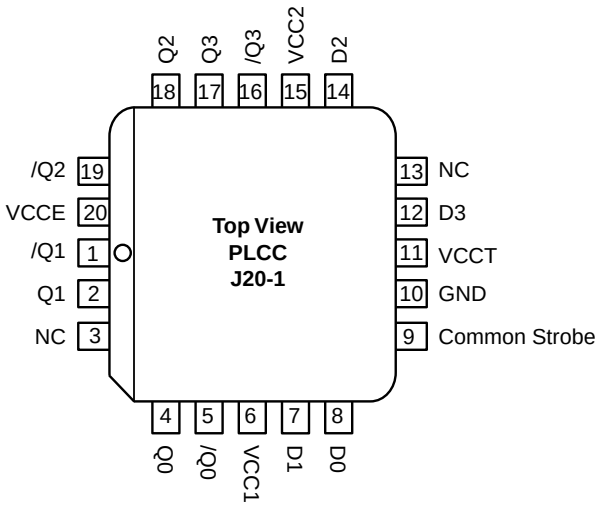
The SY10H352 can also be used with the SY10H350 to transmit and receive CMOS information differentially via balanced twisted pair lines.

BLOCK DIAGRAM



V_{CC} (+5 V_{DC}) = Pins 6, 11, 15, 20;
GND = Pin 10

PIN CONFIGURATION



PIN NAMES

Pin	Function
D0 – D3	Inputs
Q0 – Q3	Outputs
/Q0 – /Q3	Inverted outputs
VCC1	PECL V_{CC} (5.0V)
VCCE	PECL V_{CC} (5.0V)
VCCT	CMOS V_{CC} (5.0V)
VCC2	PECL V_{CC} (5.0V)
Common Strobe	Common Strobe
GND	Ground

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
I_O	Output Current –Continuous –Surge	 50 100	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

CS	D	Q	/Q
H	L	L	H
H	H	H	L
H	Open	H	L
L	X	L	H
Open	L	L	H
Open	H	H	L
Open	Open	H	L

DC ELECTRICAL CHARACTERISTICS

VCC1 = VCC2 = VCCE = VCCT = 4.75V to 5.25V

Symbol	Parameter	T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
I_{CC}	Power Supply Current ECL[1] TTL[2]	— —	45 15	— —	— —	45 15	— —	45 15	mA	No output loads
I_R	Reverse Current (Pins 7, 8, 12, 14)	—	20	—	—	20	—	20	µA	
I_{INH}	Reverse Current, (Pin 9)	—	80	—	—	80	—	80	µA	
I_F	Forward Current (Pins 7, 8, 12, 14)	—	–0.6	—	—	–0.6	—	–0.6	mA	
I_{INL}	Forward Current, (Pin 9)	—	–2.4	—	—	–2.4	—	–2.4	mA	
$V_{BR(in)}$	Input Breakdown Voltage	5.5	—	5.5	—	—	5.5	—	V	
V_I	Input Clamp Voltage	—	–1.5	—	—	–1.5	—	–1.5	V	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage[3]	3.98	4.16	4.02	—	4.19	4.09	4.28	V	
V_{OL}	Output LOW Voltage[3]	3.05	3.37	3.05	—	3.37	3.05	3.37	V	
V_{IH}	Input HIGH Voltage	3.15	—	3.15	—	—	3.15	—	V	
V_{IL}	Input LOW Voltage	—	1.5	—	—	1.5	—	1.5	V	

NOTES:

1. Total ICC at VCC1, VCC2 and VCCE.
2. ICC at ICCT.
3. These values are for VCC = 5.0V. Level Specifications will vary 1:1 VCC.

AC ELECTRICAL CHARACTERISTICS

VCC1 = VCC2 = VCCE = VCCT = 4.75V to 5.25V

Symbol	Parameter	T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay(1)	0.4	1.9	0.4	—	2.0	0.4	2.1	ns	50Ω to VCC–2V
t_r t_f	Output Rise/Fall Time (20% to 80%)	0.4	1.9	0.4	—	2.0	0.4	2.1	ns	50Ω to VCC–2V
f_{MAX}	Maximum Input Frequency(2)	150	—	150	—	—	150	—	MHz	50Ω to VCC–2V

NOTES:

1. Propagation delay is measured on this circuit from V_{CC2} on the input waveform to the 50% point on the output waveform.
2. These parameters are guaranteed but not tested.

SWITCHING WAVEFORM

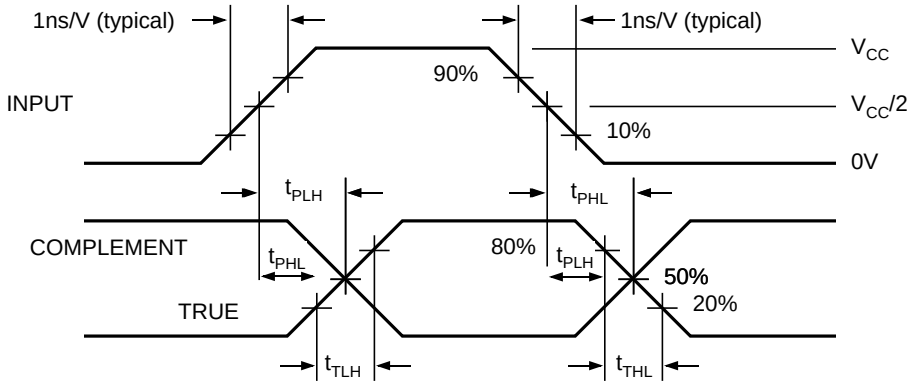
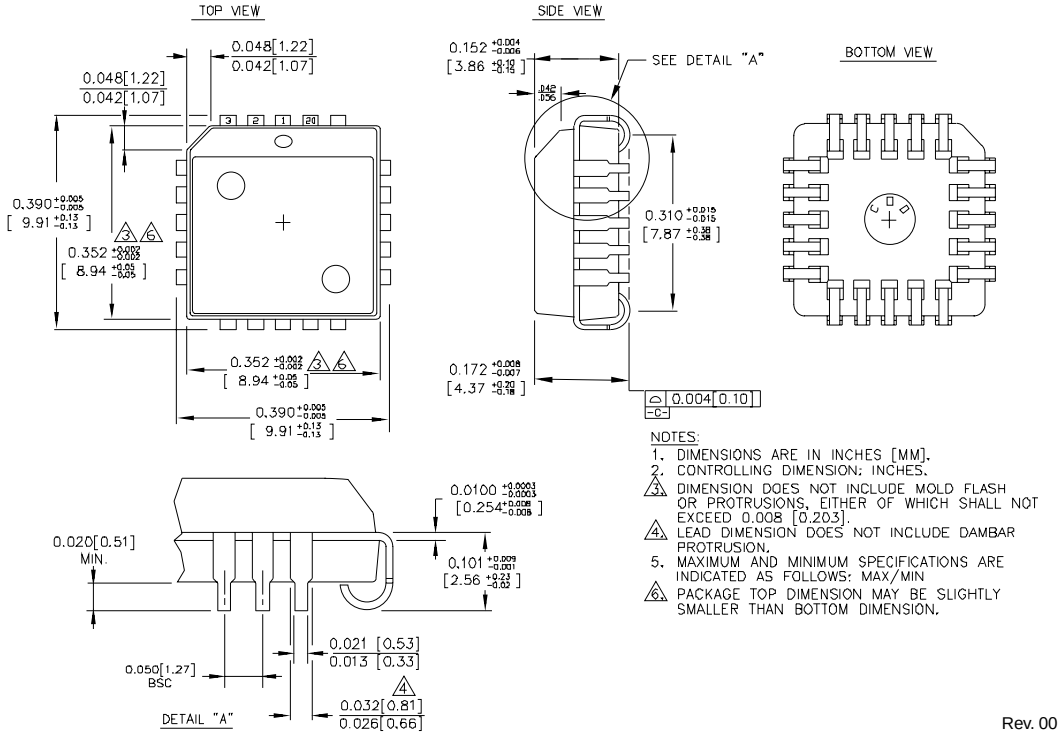


Figure 1. Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Vcc Range (V)
SY10H352JC	J20-1	Commercial	+4.75 to +5.25
SY10H352JCTR	J20-1	Commercial	+4.75 to +5.25

20 LEAD PLASTIC LEADED CHIP CARRIER (J20-1)



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