

FEATURES

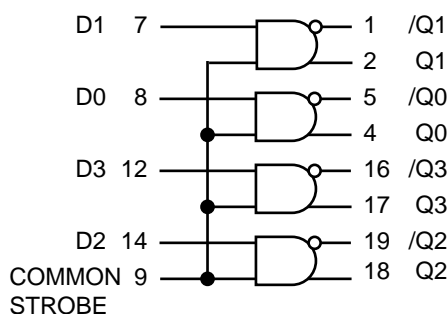
- Single 5V power supply
- All V_{CC} pins isolated on chip
- Differentially drive balanced lines
- t_{pd} 1.3ns typical
- Fully compatible with ON Semiconductor MC10H351
- Available in 20-pin PLCC package

DESCRIPTION

The SY10H351 is a quad translator for interfacing data between a saturated logic selection and the PECL section of digital systems when only a +5.0V V_{DC} power supply is available. The SY10H351 has TTL/NMOS compatible inputs and PECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at a low logic level, it forces all true outputs to the PECL low logic state ($\approx +3.2V$) and all inverting outputs to the PECL high logic state ($\approx 4.1V$).

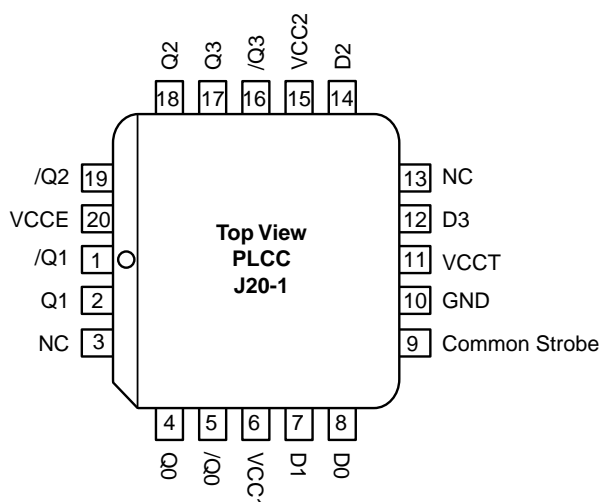
The SY10H351 can also be used with the SY10H350 to transmit and receive TTL/NMOS information differentially via balanced twisted pair lines.

BLOCK DIAGRAM



V_{CC} (+5 V_{DC}) = Pins 6, 11, 15, 20;
GND = Pin 10

PIN CONFIGURATION



PIN NAMES

Pin	Function
D0 – D3	Inputs
Q0 – Q3	Outputs
/Q0 – /Q3	Inverted outputs
VCC1	PECL V_{CC} (5.0V)
VCCE	PECL V_{CC} (5.0V)
VCCT	TTL V_{CC} (5.0V)
VCC2	PECL V_{CC} (5.0V)
Common Strobe	Common Strobe
GND	Ground

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{CC}	Power Supply Voltage	−0.5 to +7.0	V
I _O	Output Current −Continuous −Surge	50 100	mA
T _{store}	Storage Temperature	−65 to +150	°C
T _A	Operating Temperature	0 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

CS	D	Q	/Q
H	L	L	H
H	H	H	L
H	Open	H	L
L	X	L	H
Open	L	L	H
Open	H	H	L
Open	Open	H	L

DC ELECTRICAL CHARACTERISTICS

V_{CC1} = V_{CC2} = V_{CC} = V_{CE} = V_{CT} = 4.75V to 5.25V

Symbol	Parameter	T _A = 0°C		T _A = +25°C			T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
I _{CC}	Power Supply Current ECL ⁽¹⁾ TTL ⁽²⁾	—	45 15	—	—	45 15	—	45 15	mA	No output loads
I _R	Reverse Current (Pins 7, 8, 12, 14)	—	20	—	—	20	—	20	μA	
I _{INH}	Reverse Current, (Pin 9)	—	80	—	—	80	—	80	μA	
I _F	Forward Current (Pins 7, 8, 12, 14)	—	−0.6	—	—	−0.6	—	−0.6	mA	
I _{INL}	Forward Current, (Pin 9)	—	−2.4	—	—	−2.4	—	−2.4	mA	
V _{BR(in)}	Input Breakdown Voltage	5.5	—	5.5	—	—	5.5	—	V	
V _I	Input Clamp Voltage	—	−1.5	—	—	−1.5	—	−1.5	V	I _{IN} = −18mA
V _{OH}	Output HIGH Voltage ⁽³⁾	3.98	4.16	4.02	—	4.19	4.08	4.27	V	
V _{OL}	Output LOW Voltage ⁽³⁾	3.05	3.37	3.05	—	3.37	3.05	3.37	V	
V _{IH}	Input HIGH Voltage	2.0	—	2.0	—	—	2.0	—	V	
V _{IL}	Input LOW Voltage	—	0.8	—	—	0.8	—	0.8	V	

NOTES:

1. Total I_{CC} at V_{CC1}, V_{CC2} and V_{CE}.
2. I_{CC} at I_{CT}.
3. These values are for V_{CC} = 5.0V. Level Specifications will vary 1:1 V_{CC}.

AC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2} = V_{CE} = V_{CT} = 4.75V$ to $5.25V$

Symbol	Parameter	$T_A = 0^\circ C$		$T_A = +25^\circ C$			$T_A = +85^\circ C$		Unit	Condition
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay ⁽¹⁾	0.4	2.2	0.4	—	2.2	0.4	2.1	ns	50Ω to $V_{CC}-2V$
t_r t_f	Output Rise/Fall Time (20% to 80%)	0.4	1.9	0.4	—	2.0	0.4	2.1	ns	50Ω to $V_{CC}-2V$
f_{MAX}	Maximum Input Frequency ⁽²⁾	150	—	150	—	—	150	—	MHz	50Ω to $V_{CC}-2V$

NOTES:

1. Propagation delay is measured on this circuit from +1.5V on the input waveform to the 50% point on the output waveform.
2. These parameters are guaranteed but not tested.

SWITCHING WAVEFORM

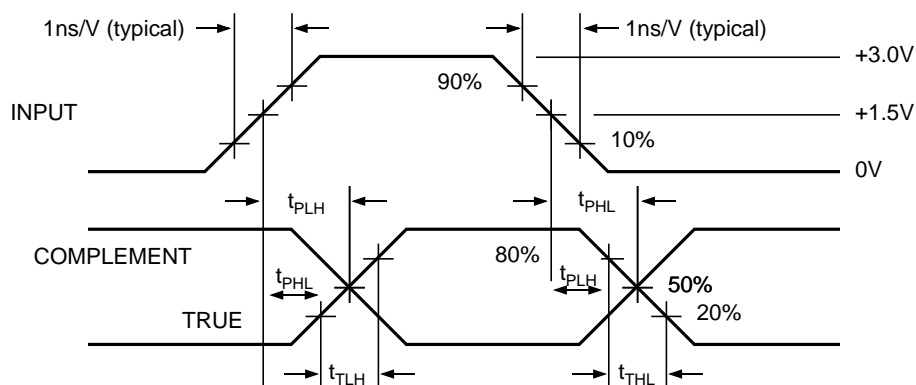
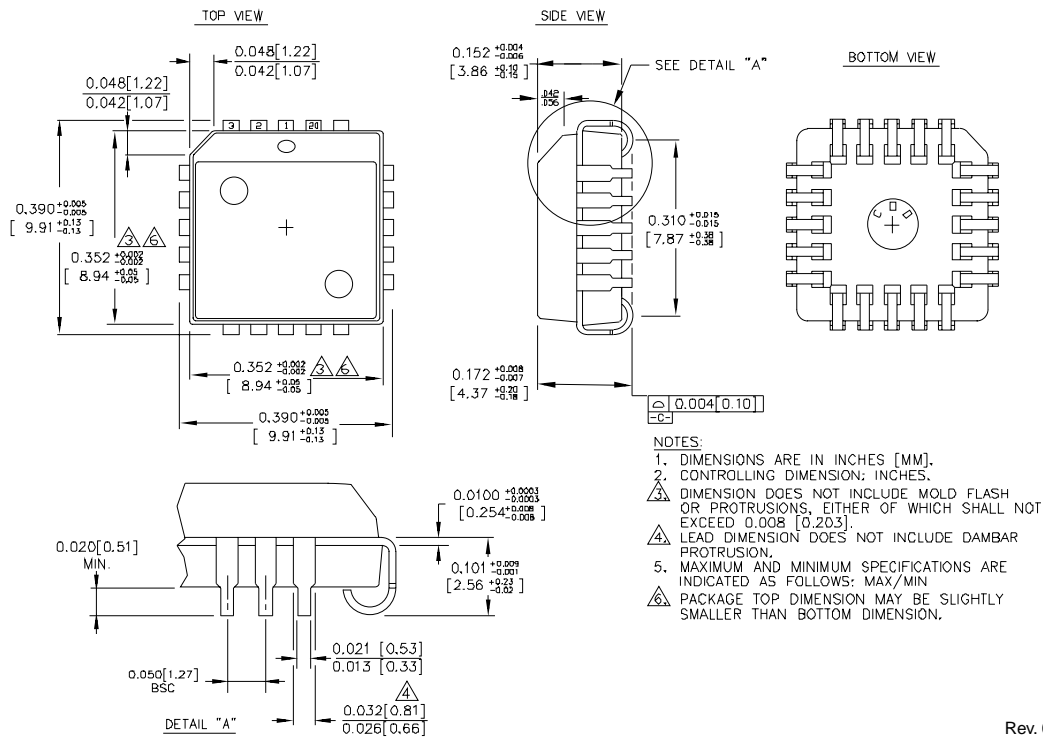


Figure 1. Propagation Delay and Transition Times

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Vcc Range (V)
SY10H351JC	J20-1	Commercial	+4.75 to +5.25
SY10H351JCTR	J20-1	Commercial	+4.75 to +5.25

20 LEAD PLASTIC LEADED CHIP CARRIER (J20-1)



Rev. 00

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