

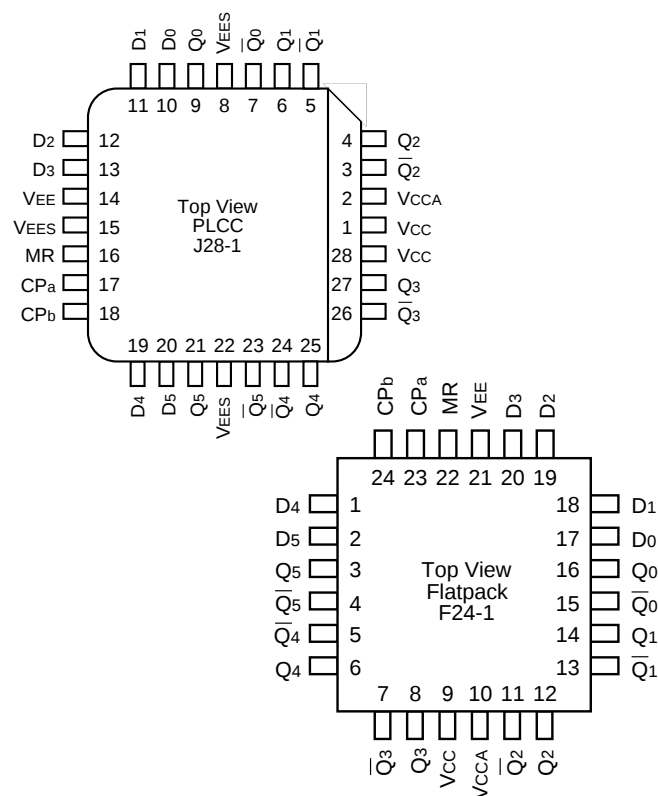
FEATURES

- Max. toggle frequency of 700MHz
- Clock to Q max. of 1200ps
- IEE min. of -98mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 50% faster than Fairchild 300K
- Better than 20% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

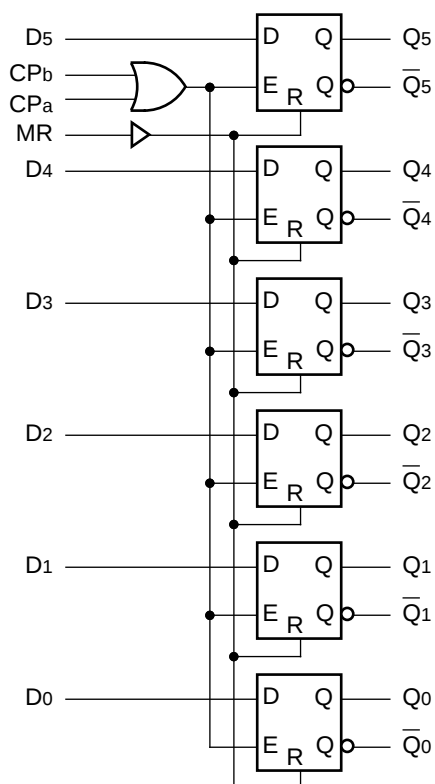
DESCRIPTION

The SY100S351 offers six D-type, edge-triggered, master/slave flip-flops with differential outputs, and is designed for use in high-performance ECL systems. The flip-flops are controlled by the signal from the logical OR operation on a pair of common clock signals (CPa, CPb). Data enters the master when both CPa and CPb are LOW and transfers to the slave when either CPa or CPb (or both) go to a logic HIGH. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN NAMES

Pin	Function
D ₀ — D ₅	Data Inputs
CP _a , CP _b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q ₀ — Q ₅	Data Outputs
$\overline{Q}_0$ — $\overline{Q}_5$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLES

Asynchronous Operation ⁽¹⁾				
Inputs				Outputs
D _n	CP _a	CP _b	MR	Q _n (t+1)
X	X	X	H	L

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
t = Time before CP Positive Transition
t+1 = Time after CP Positive Transition
u = LOW-to-HIGH Transition

Synchronous Operation ⁽¹⁾				
Inputs				Outputs
D _n	CP _a	CP _b	MR	Q _n (t+1)
L	u	L	L	L
H	u	L	L	H
L	L	u	L	L
H	L	u	L	H
X	H	u	L	Q _n (t)
X	u	H	L	Q _n (t)
X	L	L	L	Q _n (t)

DC ELECTRICAL CHARACTERISTICS

VEE = −4.2V to −5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current MR D ₀ – D ₅ CP _a , CP _b	— — —	— — —	270 200 300	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	−98	−71	−49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

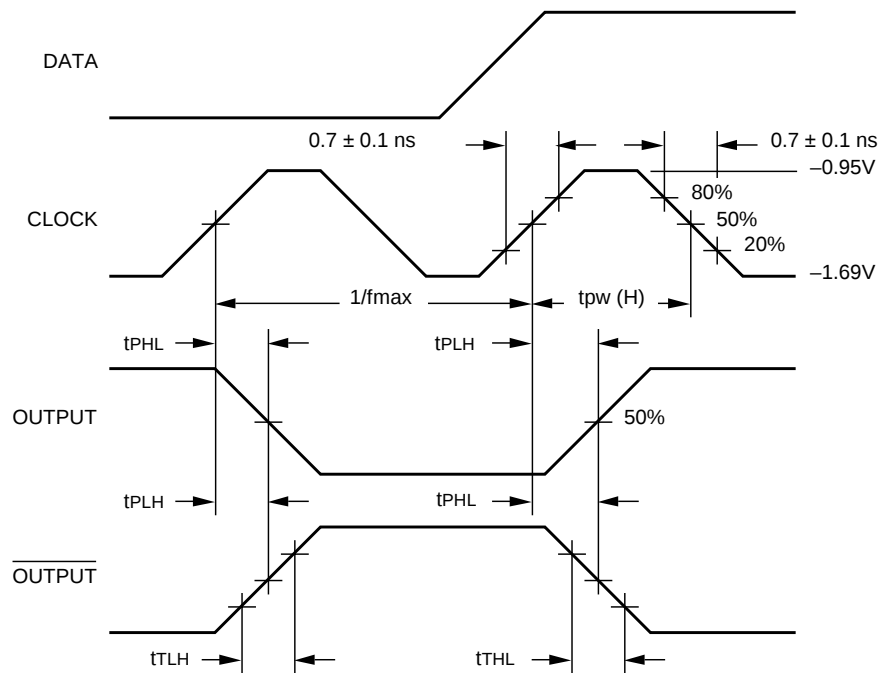
Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f _{MAX}	Toggle Frequency	700	—	700	—	700	—	MHz	
t _{PLH} t _{PHL}	Propagation Delay CP _a , CP _b to Output	—	1200	—	1200	—	1200	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	—	1200	—	1200	—	1200	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time D ₀ –D ₅ MR (Release Time)	500 1000	— —	500 1000	— —	500 1000	— —	ps	
t _H	Hold Time, D ₀ –D ₅	550	—	550	—	550	—	ps	
t _{PW} (H)	Pulse Width HIGH CP _a , CP _b , MR	1000	—	1000	—	1000	—	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f _{MAX}	Toggle Frequency	700	—	700	—	700	—	MHz	
t _{PLH} t _{PHL}	Propagation Delay CP _a , CP _b to Output	—	1200	—	1200	—	1200	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	—	1200	—	1200	—	1200	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time D ₀ –D ₅ MR (Release Time)	500 1000	— —	500 1000	— —	500 1000	— —	ps	
t _H	Hold Time, D ₀ –D ₅	550	—	550	—	550	—	ps	
t _{PW} (H)	Pulse Width HIGH CP _a , CP _b , MR	1000	—	1000	—	1000	—	ps	

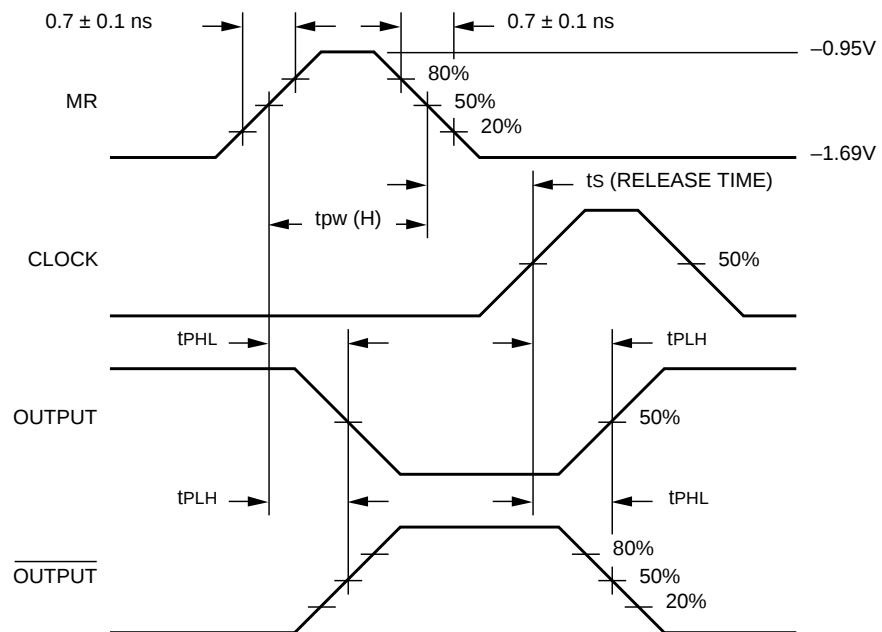
TIMING DIAGRAMS



Propagation Delay (Clock) and Transition Times

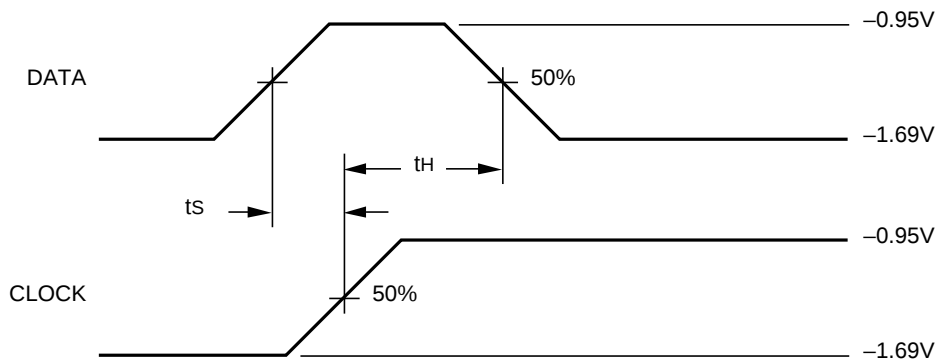
NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$



Propagation Delay (Resets)

TIMING DIAGRAMS



Data Set-up and Hold Time

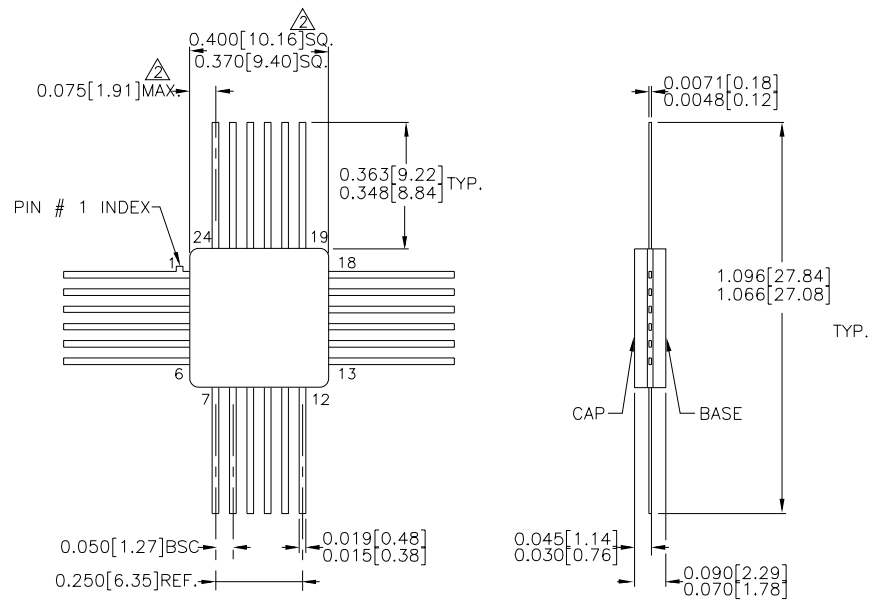
NOTES:

1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$
2. t_s is the minimum time before the transition of the clock that information must be present at the data input.
3. t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S351FC	F24-1	Commercial
SY100S351JC	J28-1	Commercial
SY100S351JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)

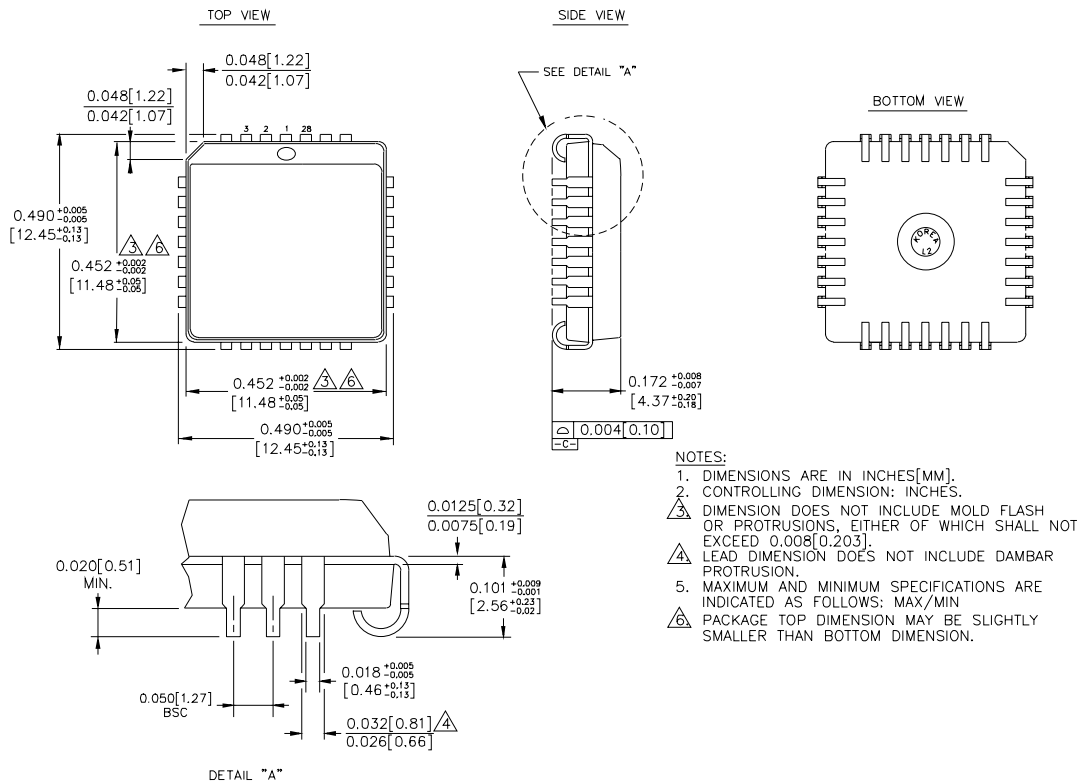


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03

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