

PIN NAMES

Pin	Function
D ₀ — D ₅	Data Inputs
$\bar{E}_a$, $\bar{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q ₀ — Q ₅	Data Outputs
$\bar{Q}_0$ — $\bar{Q}_5$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

TRUTH TABLE⁽¹⁾

Each Latch

Inputs				Outputs		Operating Mode
D _n	$\bar{E}_a$	$\bar{E}_b$	MR	Q _n	$\bar{Q}_n$	
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched ⁽²⁾	Latched ⁽²⁾	
X	H	X	L	Latched ⁽²⁾	Latched ⁽²⁾	
X	X	X	H	L	H	Asynchronous

NOTES:

1. H = HIGH State

L = LOW State

X = Don't Care

2. Retains data that is present before $\bar{E}$ positive transition.**DC ELECTRICAL CHARACTERISTICS**

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current	—	—	250	μA	V _{IN} = V _{IH} (Max.)
	MR	—	—	250		
	D _n	—	—	250		
	$\bar{E}_a$, $\bar{E}_b$	—	—	250		
I _{EE}	Power Supply Current	-98	-78	-49	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

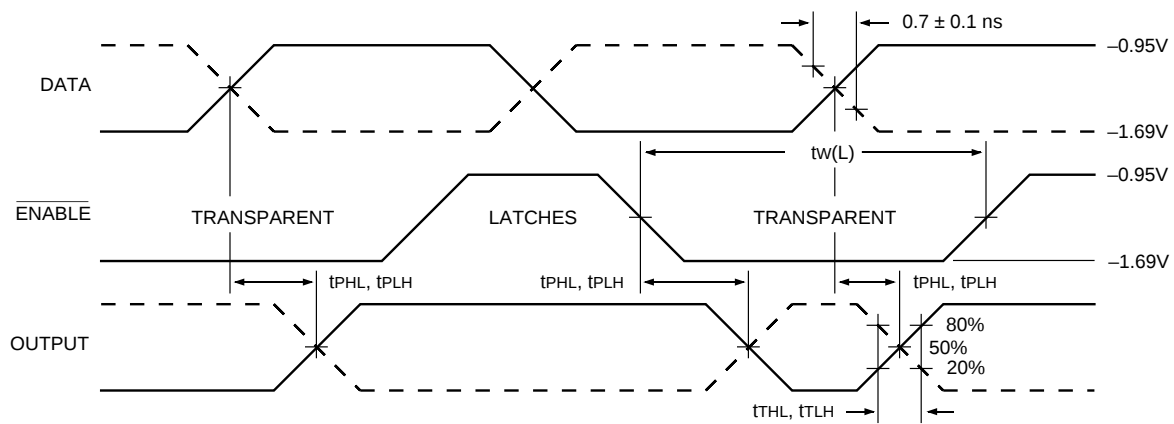
Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D _n to Output	300	1000	300	1000	300	1000	ps	
t _{PLH} t _{PHL}	Propagation Delay $\bar{E}_a$, $\bar{E}_b$ to Output	300	1100	300	1100	300	1100	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	300	1250	300	1250	300	1250	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time, D _n to $\bar{E}_n$	500	—	500	—	500	—	ps	
t _H	Hold Time, D _n to $\bar{E}_n$	500	—	500	—	500	—	ps	
t _r	Release Time, MR to $\bar{E}_n$	1000	—	1000	—	1000	—	ps	
t _{PW} (L)	Pulse Width, $\bar{E}_a$, $\bar{E}_b$	1000	—	1000	—	1000	—	ps	
t _{PW} (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D _n to Output	300	900	300	900	300	900	ps	
t _{PLH} t _{PHL}	Propagation Delay E _a , E _b to Output	300	1000	300	1000	300	1000	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _s	Set-up Time, D _n to E _n	500	—	500	—	500	—	ps	
t _H	Hold Time, D _n to E _n	500	—	500	—	500	—	ps	
t _r	Release Time, MR to E _n	1000	—	1000	—	1000	—	ps	
t _{PW} (L)	Pulse Width, E _a , E _b	1000	—	1000	—	1000	—	ps	
t _{PW} (H)	Pulse Width, MR	1000	—	1000	—	1000	—	ps	

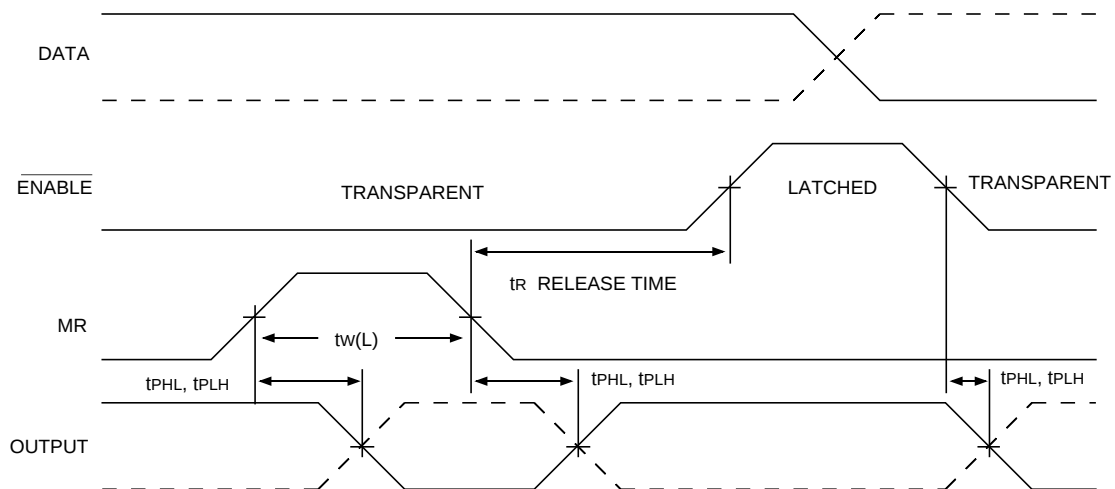
TIMING DIAGRAMS



Enable Timing

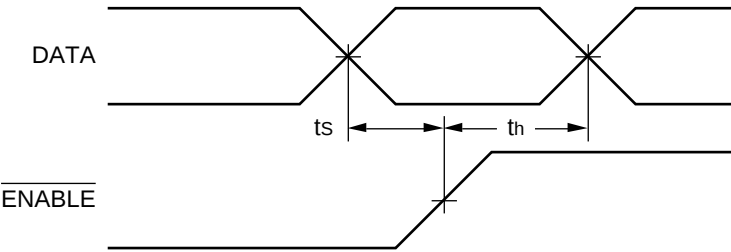
NOTE:

$V_{EE} = -4.2\text{V}$ to -5.5V unless otherwise specified; $V_{CC} = V_{CCA} = \text{GND}$



Reset Timing

TIMING DIAGRAMS



Data Set-up and Hold Times

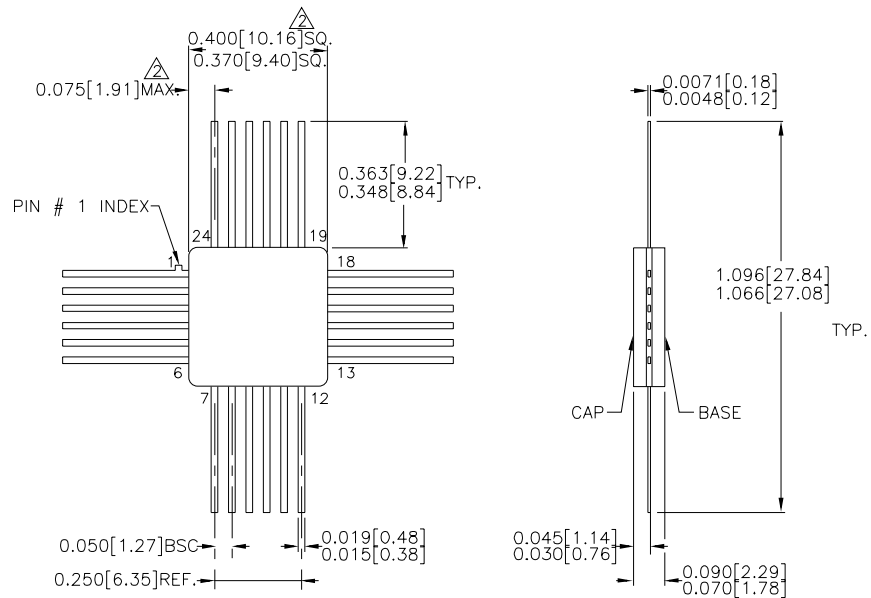
NOTES:

ts is the minimum time before the transition of the clock that information must be present at the data input.
th is the minimum time after the transition of the clock that information must remain unchanged at the data input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S350FC	F24-1	Commercial
SY100S350JC	J28-1	Commercial
SY100S350JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)

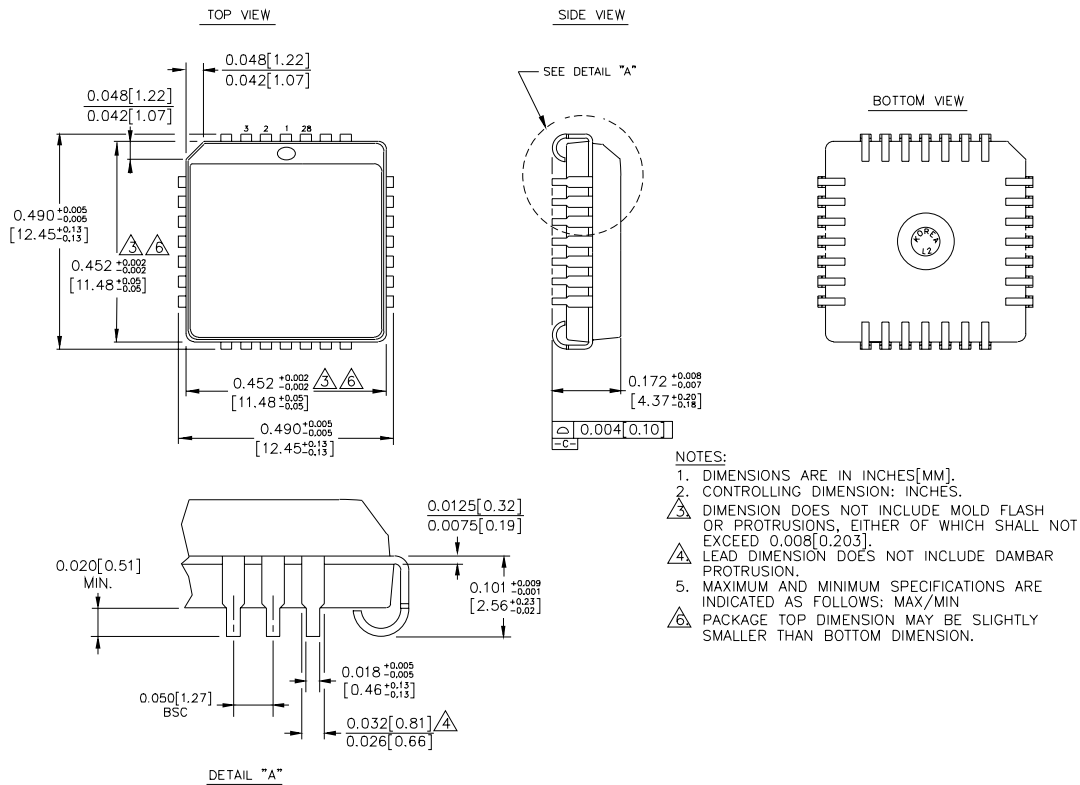


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03

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