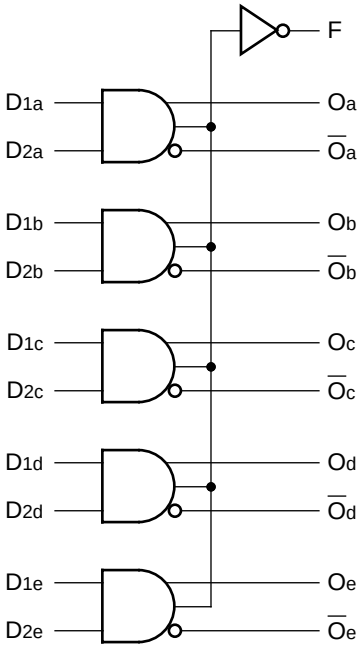
FEATURES

- **Max. propagation delay of 1050ps**
- **I_{EE} min. of –60mA**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **40% faster than Fairchild 300K at lower power**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

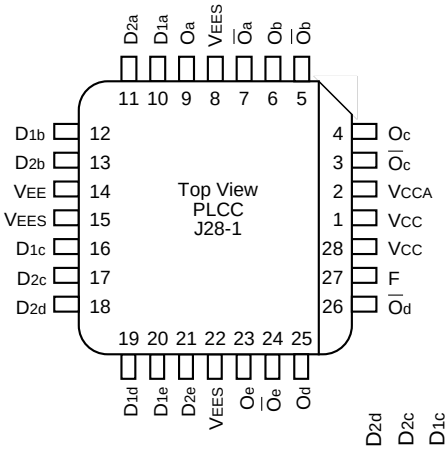
DESCRIPTION

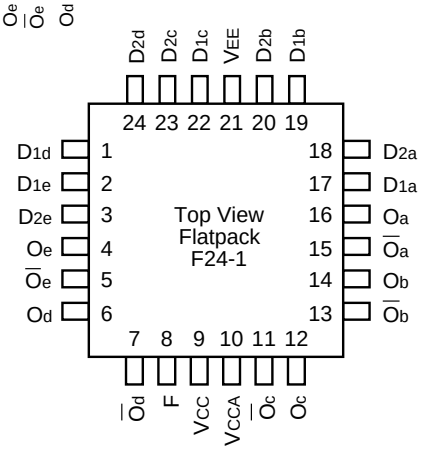
The SY100S304 is an ultra-fast quint AND/NAND gate designed for use in high-performance ECL systems. This device also features a Function (F) output which is the wire-NOR of the AND gate outputs. The inputs on the device have 75KΩ pull-down resistors.

BLOCK DIAGRAM



PIN CONFIGURATIONS





PIN NAMES

Pin	Function
D_{na} – D_{ne}	Data Inputs (n-1...5)
E	Enable Input
O_a – O_e	Data Outputs
$\overline{O_a}$ – $\overline{O_e}$	Complementary Data Outputs
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current D_{2a} — D_{2e} D_{1a} — D_{1e}	 — —	 — —	 250 250	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–60	–40	–30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

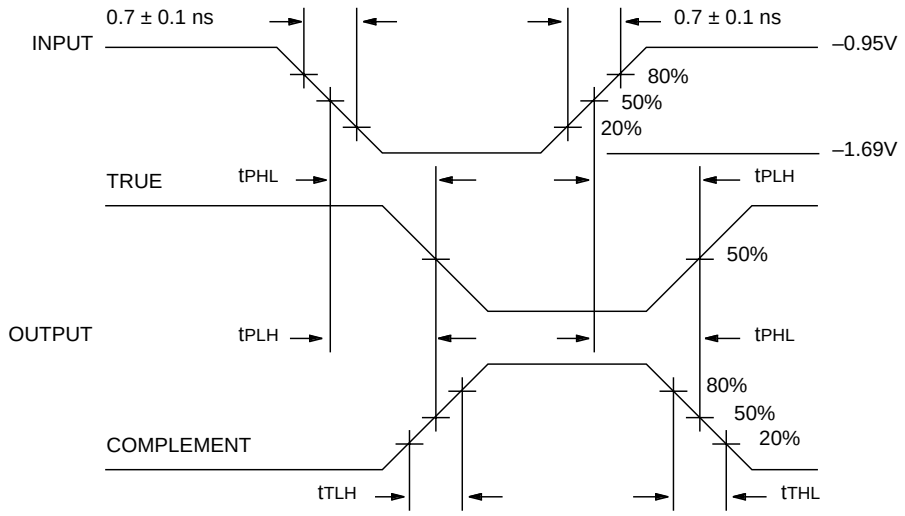
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D_{na} — D_{ne} to O, $\overline{O}$	300	1150	300	1150	300	1150	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	600	1650	600	1650	600	1650	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay D_{na} — D_{ne} to O, $\overline{O}$	300	1050	300	1050	300	1050	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	600	1550	600	1550	600	1550	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



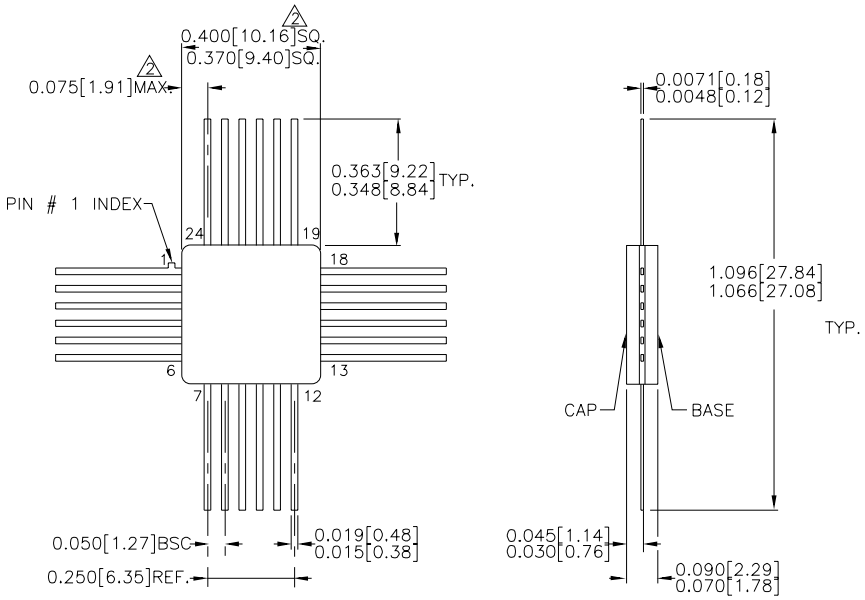
Propagation Delay and Transition Times

NOTE:
V_{EE} = –4.2V to –5.5V unless otherwise specified, V_{CC} = V_{CCA} = GND

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S304FC	F24-1	Commercial
SY100S304JC	J28-1	Commercial
SY100S304JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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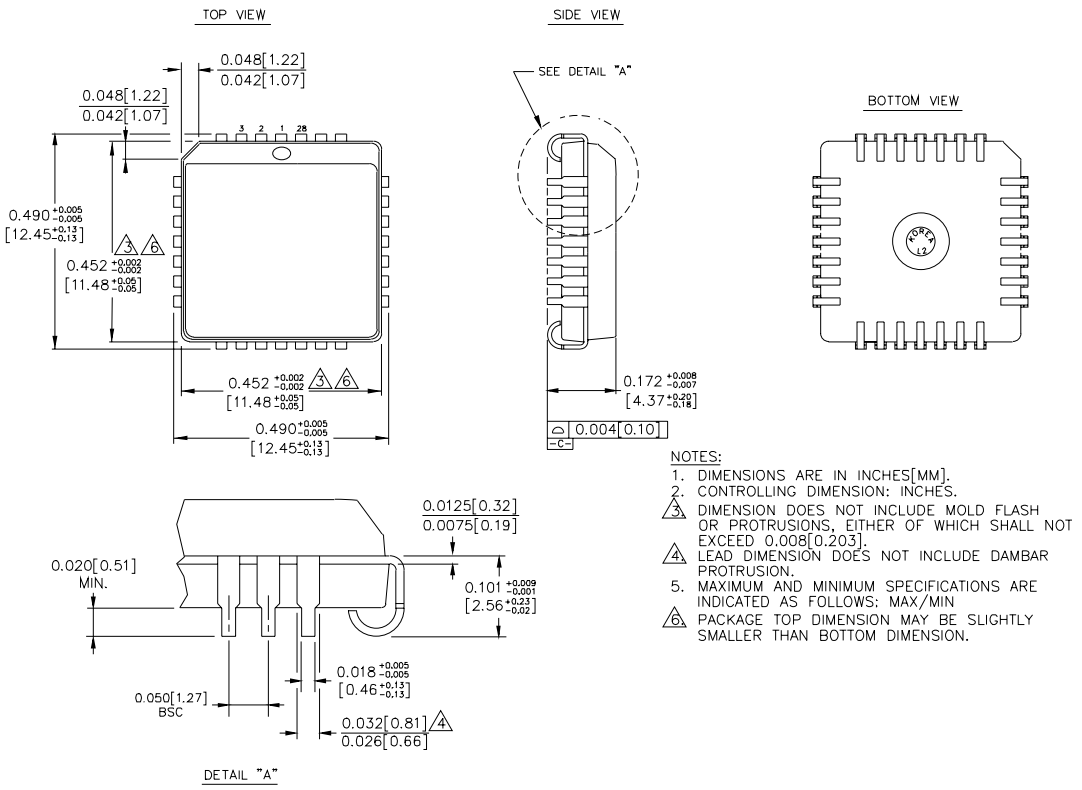
28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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