3.3V DUAL DIFFERENTIAL LVPECL-to-LVTTL TRANSLATOR

ECL Pro™
SY100EPT23L

FEATURES

- **3.3V power supply**
- **1.9ns typical propagation delay**
- **Maximum frequency > 275MHz**
- **Differential LVPECL inputs**
- **24mA LVTTL outputs**
- **Flow-through pinouts**
- **Internal input resistors: pulldown on D, pulldown and pullup on /D**
- **Q output will default LOW with inputs open or at Ground**
- **Available in 8-pin MSOP and SOIC packages**

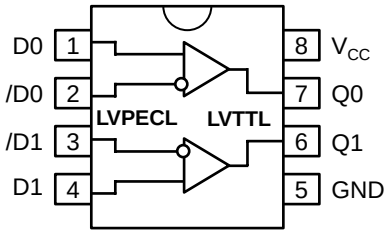
ECL Pro™

DESCRIPTION

The SY100EPT23L is a dual differential LVPECL-to-LVTTL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The tiny 8-pin MSOP and dual-gate design of the EPT23L makes it ideal for applications which require the translation of a clock and data signal.

The EPT23L is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the EPT23L does not require both ECL standard versions. The inputs can accept 10K voltage levels and any standard differential LVPECL input referenced from a V_{CC} of +3.3V

PIN CONFIGURATION/BLOCK DIAGRAM



(Available in 8-pin SOIC and 8-pin MSOP)

PIN NAMES

Pin	Function
Q0, Q1	LVTTL Outputs
D0, /D0, D1, /D1	Differential LVPECL Inputs
V_{CC}	Positive Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS(Note 1)

Symbol	Paramter	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +3.8	V
V_{IN}	PECL Input Voltage	0V to V_{CC}+0.5	V
V_{OUT}	Voltage Applied to Output at HIGH State	–0.5 to V_{CC}	V
I_{OUT}	Current Applied to Output at LOW State	Twice the Rated I_{OL}	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	–40 to +85	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

TRUTH TABLE

D	/D	Q
L	H	L
H	L	H
Open	Open	L

LVTTL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10%

		T_A = –40°C		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
V_{OH}	Output HIGH Voltage	2.0	—	2.0	—	2.0	—	2.0	—	V	I_{OH} = –3.0mA
V_{OL}	Output LOW Voltage	—	0.5	—	0.5	—	0.5	—	0.5	V	I_{OL} = 24mA
I_{CC}	Power Supply Current	—	30	—	30	—	30	—	30	mA	
I_{OS}	Output Short Circuit Current	–80	–240	–80	–240	–80	–240	–80	–240	mA	V_{OUT} = 0V

LVPECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±10%

		T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	—	µA
V_{CMR}	Common Mode Range	1.5	—	V_{CC}	1.5	—	V_{CC}	1.5	—	V_{CC}	1.5	—	V_{CC}	V
V_{PP}	Minimum Peak-to-Peak Input(Note 1)	200	—	—	200	—	—	200	—	—	200	—	—	mV
V_{IH}	Input HIGH Voltage(Note 2)	2070	—	2420	2130	—	2460	2135	—	2490	2130	—	2565	mV
V_{IL}	Input LOW Voltage(Note 2)	1350	—	1825	1350	—	1825	1350	—	1825	1350	—	1825	mV

Note 1. 200mV input guarantees full logic at output.

Note 2. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ±5%

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay	1.5	2.5	1.5	2.5	1.5	2.5	1.5	2.5	ns	C_L = 20pF
t_{skpp}	Part-to-Part Skew(Note1,4)	—	0.5	—	0.5	—	0.5	—	0.5	ns	C_L = 20pF
t_{skew++}	Within-Device Skew(Note 2,4)	—	0.3	—	0.3	—	0.3	—	0.3	ns	C_L = 20pF
t_{skew--}	Within-Device Skew(Note 3,4)	—	0.3	—	0.3	—	0.3	—	0.3	ns	C_L = 20pF
t_r t_f	Output Rise/Fall Time 1.0V to 2.0V	0.5	1.0	0.5	1.0	0.5	1.0	0.5	1.0	ns	C_L = 20pF
f_{MAX}	Maximum Input Frequency(Note 5,6)	275	—	275	—	275	—	275	—	MHz	C_L = 20pF

Note 1. Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.

Note 2. Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.

Note 3. Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.

Note 4. All skew parameters are guaranteed but not tested.

Note 5. Frequency at which guaranteed for functionality. V_{OH} and V_{OL} levels are guaranteed at DC only.

Note 6. The f_{MAX} value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

PRODUCT ORDERING CODE

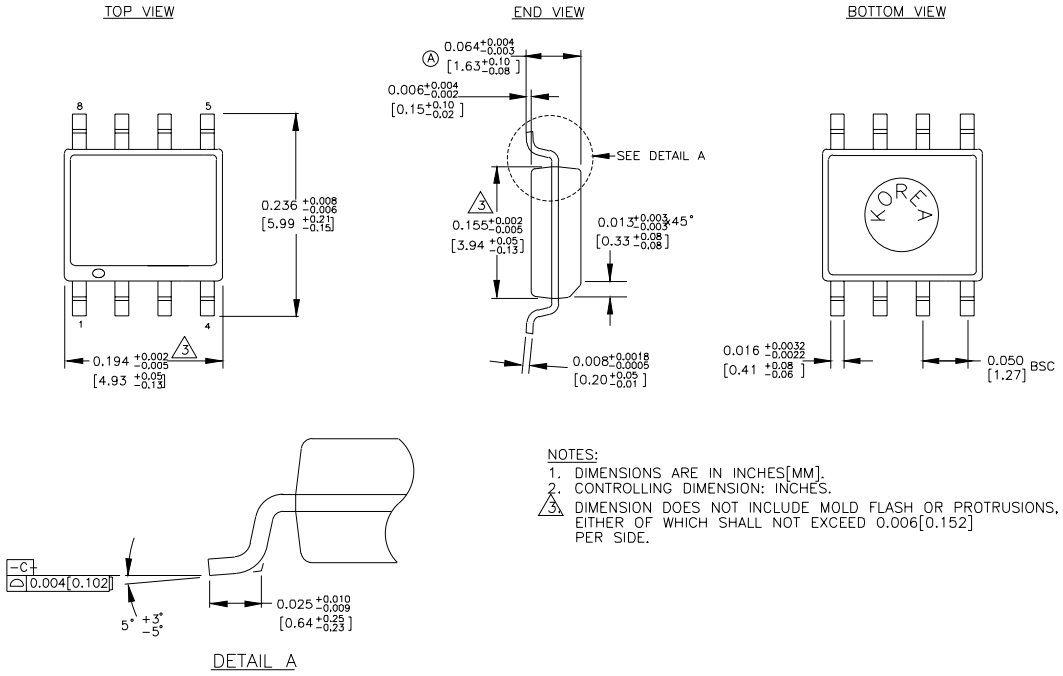
Ordering Code	Package Type	Operating Range	Package Marking
SY100EPT23LZC	Z8-1	Commercial	XEP23L
SY100EPT23LZCTR(Note 1)	Z8-1	Commercial	XEP23L
SY100EPT23LKC	K8-1	Commercial	XP23
SY100EPT23LKCTR(Note 1)	K8-1	Commercial	XP23

Ordering Code	Package Type	Operating Range	Package Marking
SY100EPT23LZI(Note 2)	Z8-1	Industrial	XEP23L
SY100EPT23LZITR(Note 1,2)	Z8-1	Industrial	XEP23L
SY100EPT23LKI(Note 2)	K8-1	Industrial	XP23
SY100EPT23LKITR(Note 1,2)	K8-1	Industrial	XP23

Note 1. Tape and Reel.

Note 2. Recommended for new designs.

8 LEAD PLASTIC SOIC (Z8-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.152] PER SIDE.

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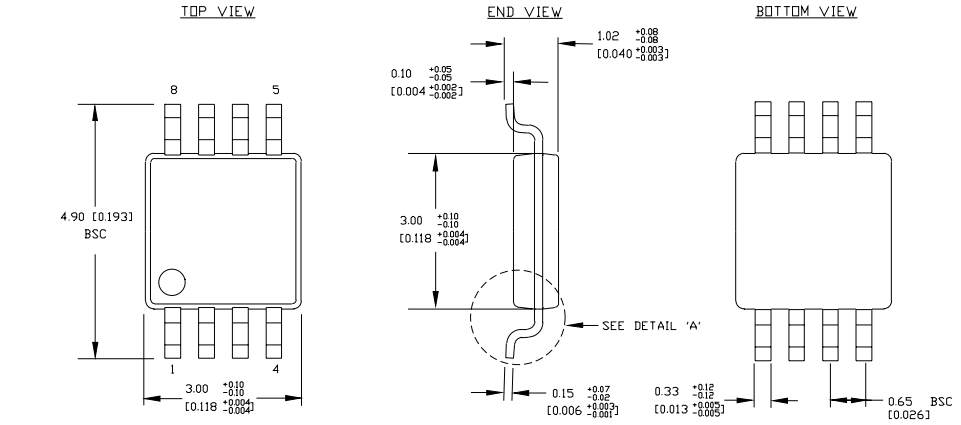
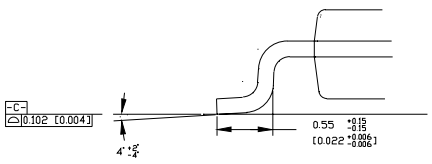
8 LEAD MSOP (K8-1)





DETAIL A

NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

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