



3.3V ECL/PECL 2:8 DIFFERENTIAL FANOUT BUFFER

Preliminary
SY100E310L

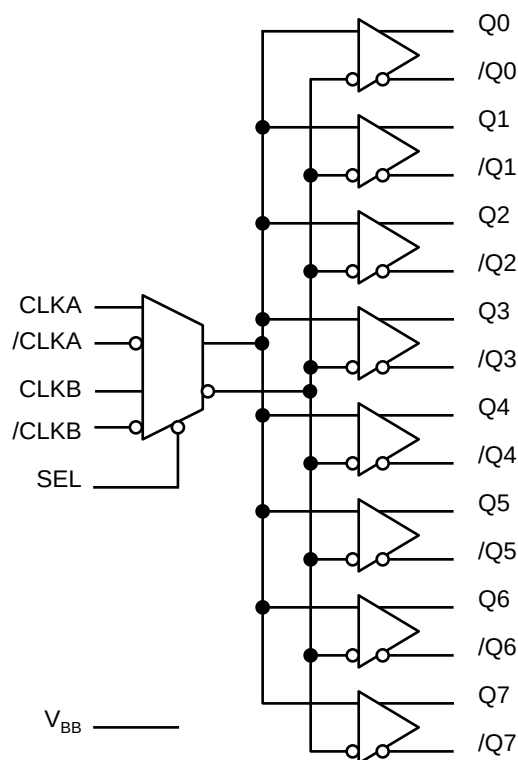
FEATURES

- **Guaranteed AC performance over temperature and voltage:**
 - > 800MHz f_{MAX} (typical)
 - < 50ps within-device skew
- **Low voltage operation:**
 - LVPECL: +3.3V $\pm 10\%$
 - LVECL: -3.3V $\pm 10\%$
- **Internal 75k Ω pull-down resistors**
- **Guaranteed over industrial temperature range:**
-40°C to +85°C
- **Pin-for-pin, plug-in replacement for MC100LVE310**
- **Available in 28-pin PLCC package**

APPLICATIONS

- **Communications clock distribution**
- **Redundant clock switchover**
- **High-end server clock distribution**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The SY100E310L is a 3.3V, precision 2:8 ECL/PECL fanout buffer optimized for precision low-skew clock distribution. The SY100E310L features fully differential clock paths to minimize both device and system skew resulting in skew performance of < 50ps. In addition, the device includes a 2:1 multiplexer input for redundant switchover applications.

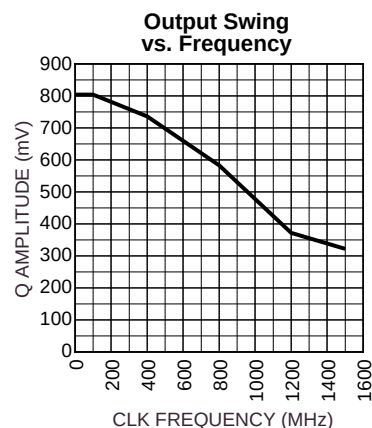
The SY100E310L is optimized for low voltage +3.3V LVPECL or -3.3V LVECL applications.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

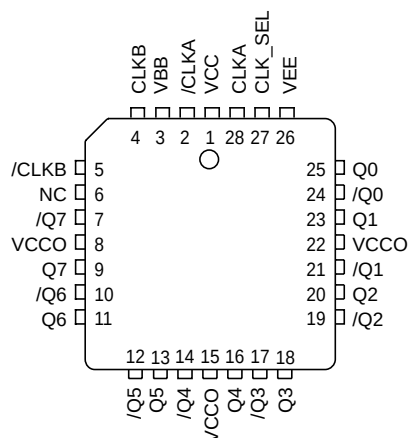
CROSS REFERENCE TABLE

Micrel Semiconductor	On Semiconductor
SY100E310LJI	MC100LVE310FN
SY100E310LJITR	MC100LVE310FNR2

TYPICAL PERFORMANCE



Ordering Information



28-Pin PLCC (J28-1)

Part Number	Package Type	Operating Range	Package Marking
SY100E310LJI	J28-1	Industrial	SY100E310LJI
SY100E310LJITR ^(Note 1)	J28-1	Industrial	SY100E310LJI

Note 1. Tape and Reel

Pin Number	Pin Name	Pin Function
1	VCC	Positive Core Power Supply. Bypass with 0.1μF//0.01μF low ESR capacitors. Not internally connected to V _{CCO} . Must be externally connected to V _{CCO} on PCB.
28, 2, 4, 5	CLKA, /CLKA CLKB, /CLKB	Differential Inputs: These input pairs are the differential data inputs to the device.
3	VBB	Reference Voltage Output. Used for AC-coupled inputs or single-ended inputs.
6	NC	No Connect.
8, 15, 22	VCCO	Positive Power Supply. Bypass with 0.1μF//0.01μF low ESR capacitors. Not internally connected to V _{CC} . Must be externally connected to V _{CC} on PCB.
24, 21, 19, 17, 14, 12, 10, 7	/Q0, /Q1, /Q2, /Q3 /Q4, /Q5, /Q6, /Q7	Differential Outputs.
25, 23, 20, 18, 16, 13, 11, 9,	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Differential Outputs.
26	VEE	Negative Supply.
27	CLK_SEL	Single-Ended Clock Select.

Absolute Maximum Ratings(Note 1)Supply Voltage (V_{CC}) -0.5V to +4.0VInput Voltage (V_{IN}) -0.5V to V_{CC} Termination Current, **Note 3**Source or sink current on V_{BB} (I_{BB}) ± 0.5 mA

Input Current

Source or sink current

(CLKA, /CLKA, CLKB, /CLKB, CLK_SEL) ± 50 mA

Lead Temperature (soldering, 10 sec.) +220°C

Storage Temperature (T_S) -65°C to +150°C**Operating Ratings**(Note 2)Supply Voltage (V_{CC}) +3.0V to +3.6VAmbient Temperature (T_A) -40°C to +85°C

Package Thermal Resistance

PLCC (θ_{JA})

Still-Air 63.5°C/W

500lfpm 43.5°C/W

DC ELECTRICAL CHARACTERISTICS(Note 4) T_A = -40°C to +85°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V

LVPECL DC ELECTRICAL CHARACTERISTICS(Note 4, 5) V_{CC} = +3.3V, V_{EE} = 0V

Symbol	Parameter	-40°C			+25°C			+85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{CC}	Power Supply Current		55	70		55	70		55	70	mA	No load, max. V_{CC}
V_{OH}	Output High Voltage (Q0-Q7, /Q0-/Q7)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV	$R_L = 50\Omega$ to $V_{CC}-2V$
V_{OL}	Output Low Voltage (Q0-Q7, /Q0-/Q7)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV	$R_L = 50\Omega$ to $V_{CC}-2V$
V_{IH}	Input High Voltage (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)	2135		2420	2135		2420	2135		2420	mV	
V_{IL}	Input Low Voltage (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)	1490		1825	1490		1825	1490		1825	mV	
V_{IHCMR}	Input High Voltage Common Mode Range (Differential) (CLKA, /CLKA, CLKB, /CLKB)	1.8		2.9	1.8		2.9	1.8		2.9	V	Note 6
V_{BB}	Output Reference Voltage	1.92		2.04	1.92		2.04	1.92		2.04	V	
I_{IN}	Input HIGH Current (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)			150			150			150	μA	
I_{IL}	Input LOW Current (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)	0.5			0.5			0.5			μA	

LVNECL DC ELECTRICAL CHARACTERISTICS(Notes 4, 5) $V_{CC} = 0V$, $V_{EE} = -3.3V$

Symbol	Parameter	-40°C			+25°C			+85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{OH}	Output High Voltage (Q0-Q7, /Q0-/Q7)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV	$R_L = 50\Omega$ to $V_{CC}-2V$
V_{OL}	Output Low Voltage (Q0-Q7, /Q0-/Q7)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV	$R_L = 50\Omega$ to $V_{CC}-2V$
V_{IH}	Input High Voltage (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)	-1165		-880	-1165		-880	-1165		-880	mV	
V_{IL}	Input Low Voltage (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)	-1810		-1475	-1810		-1475	-1810		-1475	mV	
V_{IHCMR}	Input High Voltage Common Mode Range (Differential) (CLKA, /CLKA, CLKB, /CLKB)	-1.5		-0.4	-1.5		-0.4	-1.5		-0.4	V	Note 6
V_{BB}	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V	
I_{IN}	Input HIGH Current (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)			150			150			150	μA	
I_{IL}	Input LOW Current (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)	0.5			0.5			0.5			μA	

AC ELECTRICAL CHARACTERISTICS $V_{CC} = +3.0$ to $+3.6V$ and $V_{EE} = 0V$ or $V_{CC} = 0V$ and $V_{EE} = -3.0$ to $-3.6V$

Symbol	Parameter	-40°C			+25°C			+85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Maximum Operating Frequency		800			800			800		MHz	$V_{OUT} = 400mV$
t_{pd}	Propagation Delay CLKA-to-Q, CLKB-to-Q (Differential)	525		725	525		725	525		725	ps	Note 7
	CLKA-to-Q, CLKB-to-Q (Single-ended)	500		750	500		750	500		750	ps	Note 8
t_{SKEW}	Within-Device Skew Part-to-Part Skew (Differential)			75 250			50 200			50 200	ps ps	Note 9
t_{JITTER}	Cycle-to-Cycle Jitter		1			1			1		ps(rms)	
V_{PP}	Input Swing	500		1000	500		1000	500		1000	mV	Note 10
t_r, t_f	Rise / Fall Time (20% to 80%) (Q0-Q7, /Q0-/Q7)	160	375	600	160	375	600	160	375	600	ps	

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Due to the limited drive capability use for input of the same package only.

Note 4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 5. Input and output parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.3V$.

Note 6. V_{IHCMR} is defined as the range within which the V_{IH} level may vary with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and then greater than or equal to $V_{PP}(\min)$.

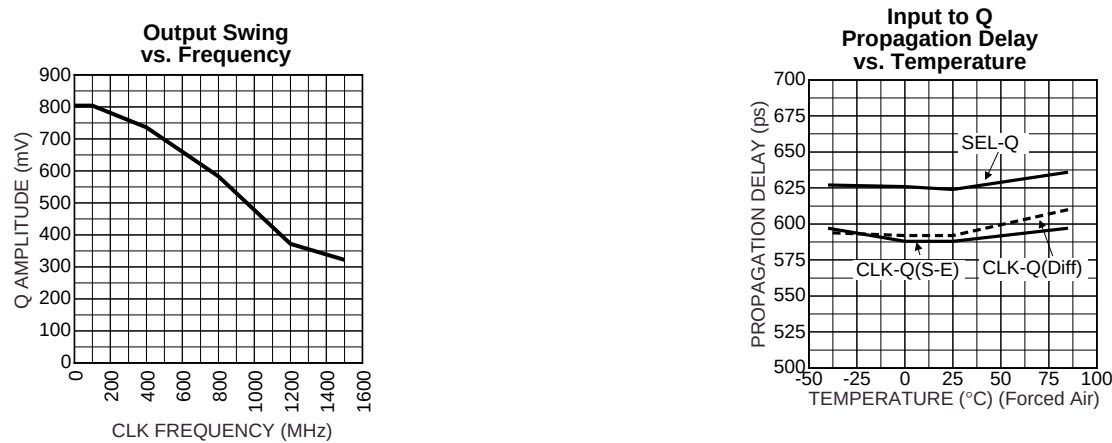
Note 7. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.

Note 8. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.

- Note 9.** The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
- Note 10.** V_{PP} (min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min) is AC limited for the E310L as a differential input as low as 50 mV will still produce full ECL levels at the output.

TYPICAL OPERATING CHARACTERISTICS

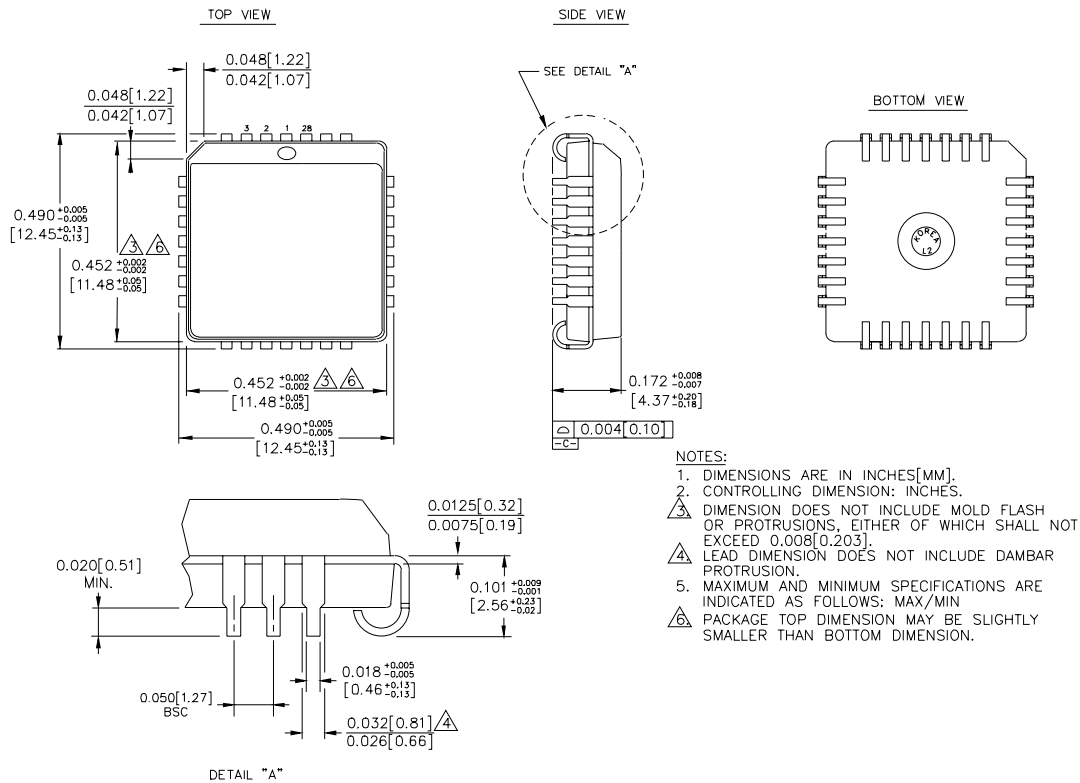
$V_{CC} = 3.3V$, $T_A = 25^{\circ}C$



RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

28 LEAD PLCC (J28-1)



Rev. 03

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