FEATURES

- 9-bit ideal for byte-parity applications
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- Dual supply
- 3.5ns max. D to Q
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- Fully compatible with Motorola MC10H/100H602
- Available in 28-pin PLCC package

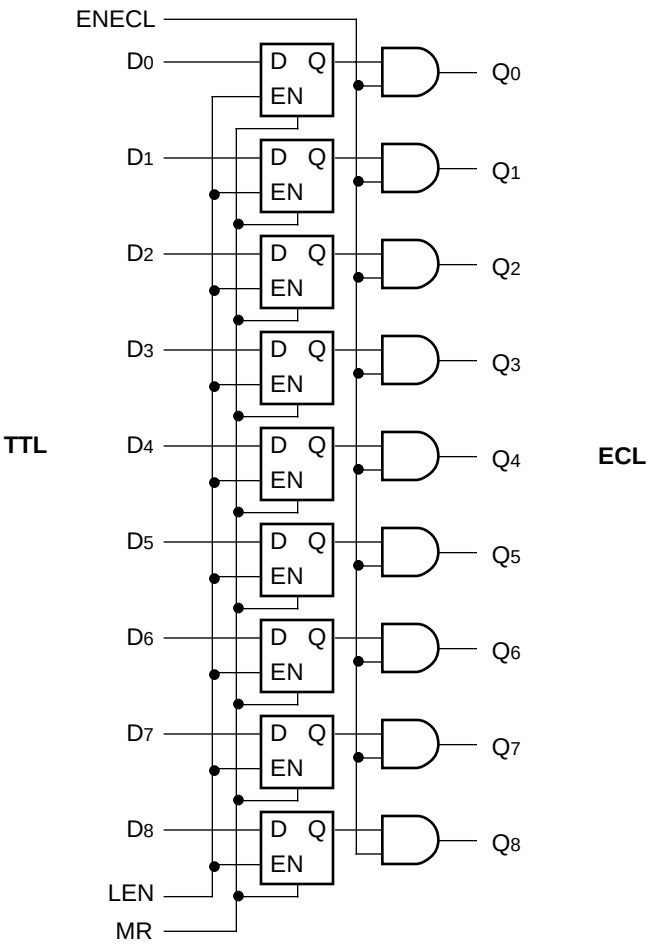
DESCRIPTION

The SY10/100H602 are 9-bit, dual supply TTL-to-ECL translators with latches. Devices in the Micrel-Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

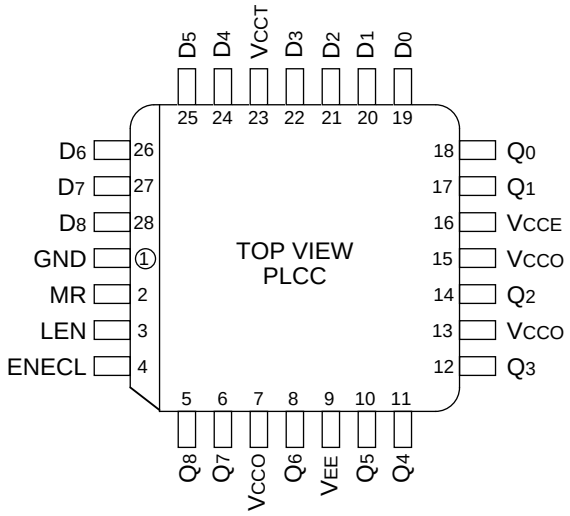
The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
V_{CCE}	ECL V_{CC} (0V)
V_{CCO}	ECL V_{CC} (0V) — Outputs
V_{CCT}	TTL Supply (+5.0V)
V_{EE}	ECL Supply (–5.2/–4.5V)
D_0–D_8	Data Inputs (TTL)
Q_0–Q_8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q_0
X	X	H	H	L
X	X	X	L	L

DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –4.75V to –5.5V (10H Version); V_{EE} = –4.2V to –5.5V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current, ECL							mA	—
	10H	—	125	—	125	—	125		
	100H	—	122	—	123	—	132		
I_{CCH}	Power Supply Current, TTL	—	48	—	48	—	48	mA	—
I_{CCL}		—	50	—	50	—	50		

AC ELECTRICAL CHARACTERISTICS

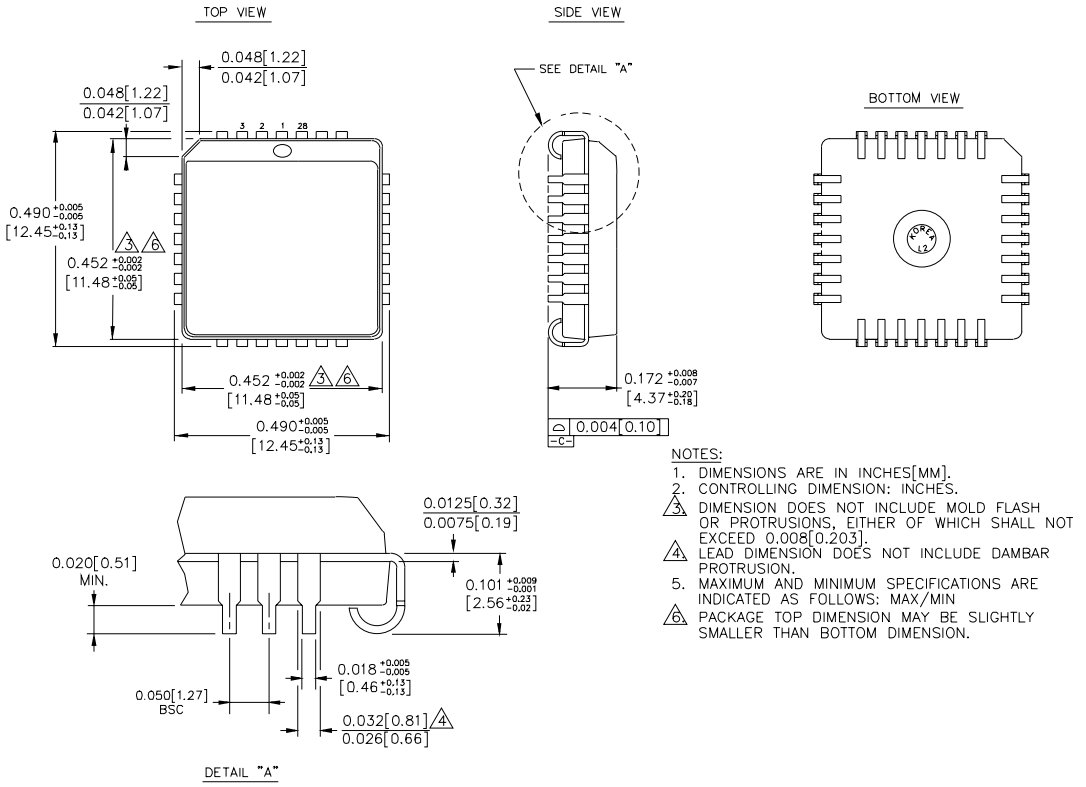
V_{CCT} = 5.0V ± 10%; V_{EE} = –4.75V to –5.5V (10H Version); V_{EE} = –4.2V to –5.5V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH}	Propagation Delay to Output							ns	—
t_{PHL}	D	1.4	3.0	1.5	3.2	1.7	3.5		
	LEN	2.0	3.4	2.1	3.5	2.4	3.7		
	MR	2.0	3.4	2.1	3.5	2.5	3.9		
	ENECL	1.6	3.2	1.7	3.3	1.8	3.7		
t_S	Set-up Time, D to LEN	2.0	—	2.0	—	2.0	—	ns	—
t_H	Hold Time, D to LEN	1.0	—	1.0	—	1.0	—	ns	—
$t_{w(L)}$	LEN Pulse Width, LOW	2.0	—	2.0	—	2.0	—	ns	—
t_r	Output Rise/Fall Time	0.5	1.5	0.5	1.5	0.5	1.5	ns	—
t_f	20% to 80%, 80% to 20%								

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H602JC	J28-1	Commercial
SY10H602JCTR	J28-1	Commercial
SY100H602JC	J28-1	Commercial
SY100H602JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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