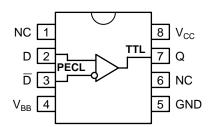
# 3.3V DIFFERENTIAL LVPECL-to-LVTTL TRANSLATOR

Precision Edge™ SY10ELT21L SY100ELT21L FINAL

## **FEATURES**

- 3.3V power supply
- 2.0ns typical propagation delay
- Low power
- **■** Differential LVPECL inputs
- 24mA TTL outputs
- **■** Flow-through pinouts
- Available in 8-pin SOIC package

## PIN CONFIGURATION/BLOCK DIAGRAM





Precision Edge™

## **DESCRIPTION**

The SY10/100ELT21L are single differential LVPECL-to-LVTTL translators using a single +3.3V power supply. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and low skew single gate design make the ELT21L ideal for applications that require the translation of a clock or data signal where minimal space, low power, and low cost are critical.

 $V_{BB}$  allows a differential, single-ended, or AC-coupled interface to the device. If used, the  $V_{BB}$  output should be bypassed to  $V_{CC}$  with  $0.01\mu F$  capacitor.

Under open input conditions, the /D will be biased at a  $V_{\rm CC}/2$  voltage level and the D input will be pulled to ground. This condition will force the Q output low to provide added stability.

The ELT21L is available in both ECL standards: the 10ELT is compatible with positive ECL 10H logic levels, while the 100ELT is compatible with positive ECL 100K logic levels.

### PIN NAMES

Pin	Function
Q	TTL Output
D, /D	Differential LVPECL Inputs
V <sub>CC</sub>	+3.3V Supply
V <sub>BB</sub>	Reference Output
GND	Ground

# ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Paramter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage	-0.5 to +3.8	V
V <sub>I</sub>	PECL Input Voltage	0V to V <sub>CC</sub> +0.5	٧
Vo	Voltage Applied to Output at HIGH State	–0.5 to V <sub>CC</sub>	V
I <sub>O</sub>	Current Applied to Output at LOW State	Twice the Rated I <sub>OL</sub>	mA
T <sub>store</sub>	Storage Temperature	-65 to +150	°C
T <sub>A</sub>	Operating Temperature	-40 to +85	°C

Т	R		П		Δ	В		
		_			-	_	_	_

D	/D	Q
L	Н	L
Н	L	Н
Open	Open	L

#### NOTE:

 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

# TTL DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = +3.3V \pm 5\%$ 

		TA = -40°C		TA = 0°C		TA = +25°C		TA = +85°C				
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Тур.	Max.	Min.	Max.	Unit	Condition
Ios	Output Short Circuit Current	-80	-275	-80	-275	-80	_	-275	-80	-275	mA	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current	_	20	_	20	_	14	20	_	20	mA	
V <sub>OH</sub>	Output HIGH Voltage	2.0	_	2.0	_	2.0	_	_	2.0	_	V	$I_{OH} = -3.0 \text{mA}$
V <sub>OL</sub>	Output LOW Voltage	_	0.5	_	0.5	_	_	0.5		0.5	V	I <sub>OL</sub> = 24mA

# PECL DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = +3.3V \pm 5\%$ 

			TA = -	-40°C	Ta =	0°C	TA	\ = +25°	Ď	TA = -	+85°C		
Symbol	Parameter		Min.	Max.	Min.	Max.	Min.	Тур.	Max.	Min.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current			150		150	_	_	150		150	μΑ	
I <sub>IL</sub>	Input LOW Current	D/D	0.5 -300		0.5 -300		0.5 -300	_		0.5 -300		μΑ	
V <sub>IH</sub>	Input HIGH Voltage <sup>(2)</sup> 100 1000	ELT ELT	2070 2135	2410 2420	2130 2135	2460 2420	2170 2135		2490 2420	2240 2135	2580 2420	mV	
V <sub>IL</sub>	Input LOW Voltage <sup>(2)</sup> 10I	ELT ELT	1350 1490	1800 1825	1350 1490	1820 1825	1350 1490	_	1820 1825	1350 1490	1855 1825	mV	
V <sub>BB</sub>	Reference Output <sup>(2)</sup> 10I 100I	ELT ELT	1870 1920	2000 2040	1920 1920	2030 2040	1950 1920	2000 1980	2050 2040	1990 1920	2110 2040	mV	

## NOTES:

1. These values are for  $V_{\rm CC}$  = 3.3V. Level Specifications will vary 1:1  $V_{\rm CC}$ .

# AC ELECTRICAL CHARACTERISTICS

 $V_{CC} = +3.3V \pm 5\%$ 

		TA = -40°C		Ta = 0°C		TA = +25°C			TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Тур.	Max.	Min.	Max.	Unit	Condition
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	1.5	2.5	1.5	2.5	1.5	2.0	2.5	1.5	2.5	ns	C <sub>L</sub> = 20pF
t <sub>skpp</sub>	Part-to-Part Skew <sup>(1,2)</sup>		0.5	_	0.5	_	_	0.5		0.5	ns	$C_L = 20pF$
f <sub>MAX</sub>	Maximum Input Frequency(2,3,4)	275	_	275	_	275	_	_	275	_	MHz	$C_L = 20pF$
$V_{CMR}$	Common Mode Range	1.2	V <sub>CC</sub>	1.2	V <sub>CC</sub>	1.2	_	$V_{CC}$	1.2	V <sub>CC</sub>	V	
V <sub>PP</sub>	Minimum Peak-to-Peak Input <sup>(5)</sup>	100	_	100	_	100	_		100	_	mV	
t <sub>r</sub>	Output Rise/Fall Time (1.0V to 2.0V)	0.5	1.0	0.5	1.0	0.5	_	1.0	0.5	1.0	ns	C <sub>L</sub> = 20pF

#### NOTES:

- 1. Part-to-Part Skew considering HIGH-to-HIGH transitions at common  $\rm V_{\rm cc}$  level.
- 2. These parameters are guaranteed but not tested.
- 3. Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
- $\textbf{4.} \ \ \textbf{The} \ \textbf{f}_{\text{MAX}} \ \textbf{value} \ \textbf{is specified as the minimum guaranteed maximum frequency}. \ \ \textbf{Actual operational maximum frequency may be greater}.$
- 5. 100mV input guarantees full logic at output.

# PRODUCT ORDERING CODE

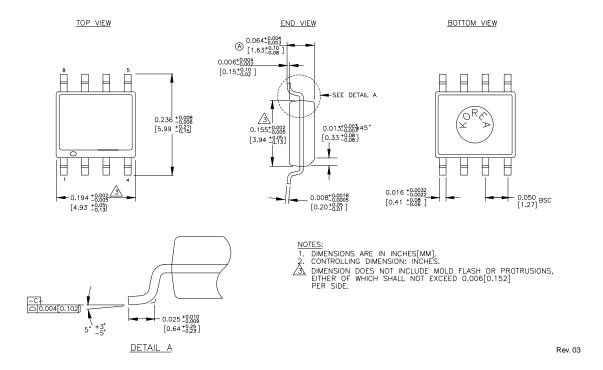
Ordering Code	Package Type	Operating Range	Marking Code
SY10ELT21LZC	Z8-1	Commercial	HEL21L
SY10ELT21LZCTR*	Z8-1	Commercial	HEL21L
SY100ELT21LZC	Z8-1	Commercial	XEL21L
SY100ELT21LZCTR*	Z8-1	Commercial	XEL21L

Ordering Code	Package Type	Operating Range	Marking Code
SY10ELT21LZI <sup>(1)</sup>	Z8-1	Industrial	HEL21L
SY10ELT21LZITR*(1)	Z8-1	Industrial	HEL21L
SY100ELT21LZI <sup>(1)</sup>	Z8-1	Industrial	XEL21L
SY100ELT21LZITR*(1)	Z8-1	Industrial	XEL21L

Note 1. Recommended for new designs.

<sup>\*</sup>Tape and Reel

# 8 LEAD SOIC .150" WIDE (Z8-1)



### MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com

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