

FEATURES

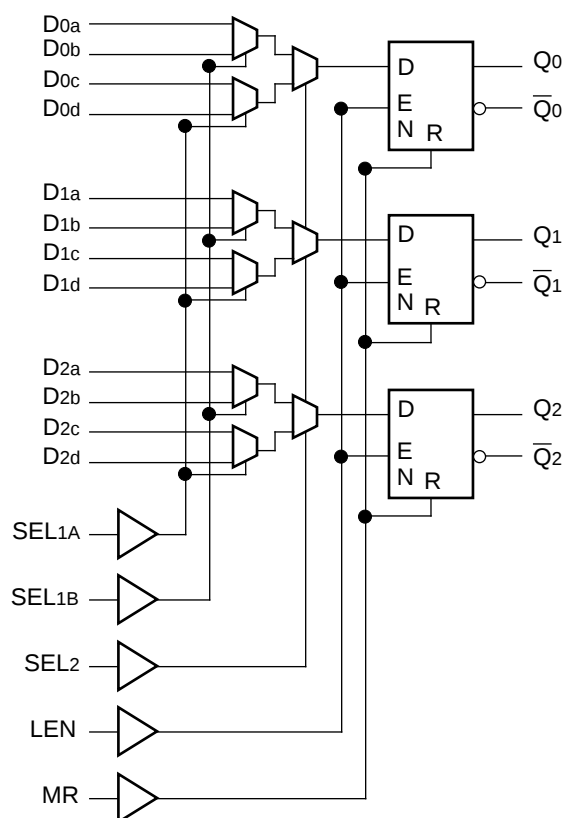
- 950ps max. data to output
- Extended 100E VEE range of -4.2V to -5.5V
- 850ps max. latch enable to output
- Separate select controls
- Differential outputs
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E256
- Available in 28-pin PLCC package

DESCRIPTION

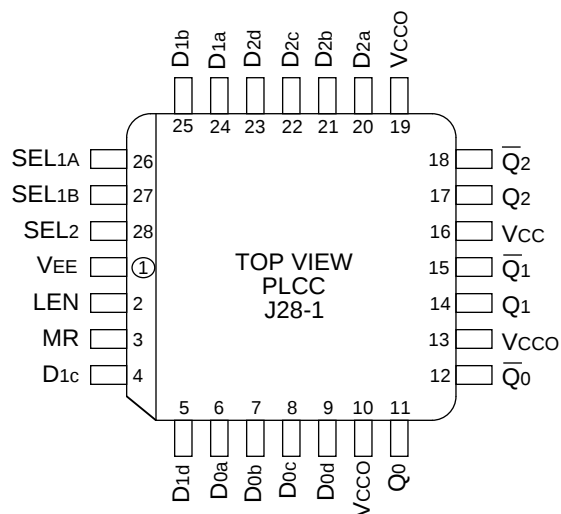
The SY10/100E256 offer three 4:1 multiplexers followed by latches with differential outputs designed for use in new, high-performance ECL systems. Separate Select controls are provided for the leading 2:1 mux pairs (see block diagram).

When the Latch Enable (LEN) is at a logic LOW, the latch is transparent and output data is controlled by the multiplexer select controls. A logic HIGH on LEN latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0x-D2x	Parallel Data Inputs
SEL1A, SEL1B	First-stage Select Inputs
SEL2	Second-stage Select Input
LEN	Latch Enable
MR	Master Reset
Q0, Q0-bar, Q1, Q1-bar, Q2, Q2-bar	Data Outputs
VCCO	Vcc to Output

TRUTH TABLE

Pin	State	Operation
SEL2	H	Output c/d Data
SEL1A	H	Input d Data
SEL1B	H	Input b Data

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	69	83	—	69	83	—	69	83		
	100E	—	69	83	—	69	83	—	79	96		

AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output D SEL1 SEL2 LEN MR	400 550 450 350 350	600 775 650 500 600	900 1050 900 800 825	400 550 450 350 350	600 775 650 500 600	900 1050 900 800 825	400 550 450 350 350	600 775 650 500 600	900 1050 900 800 825	ps	—
t _S	Set-up Time D SEL1 SEL2	400 600 500	275 300 250	— — —	400 600 500	275 300 250	— — —	400 600 500	275 300 250	— — —	ps	—
t _H	Hold Time D SEL1 SEL2	300 100 200	–275 –300 –250	— — —	300 100 200	–275 –300 –250	— — —	300 100 100	–275 –300 –250	— — —	ps	—
t _{RR}	Reset Recovery Time	700	600	—	700	600	—	700	600	—	ps	—
t _{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	275	475	700	275	475	700	275	475	700	ps	—

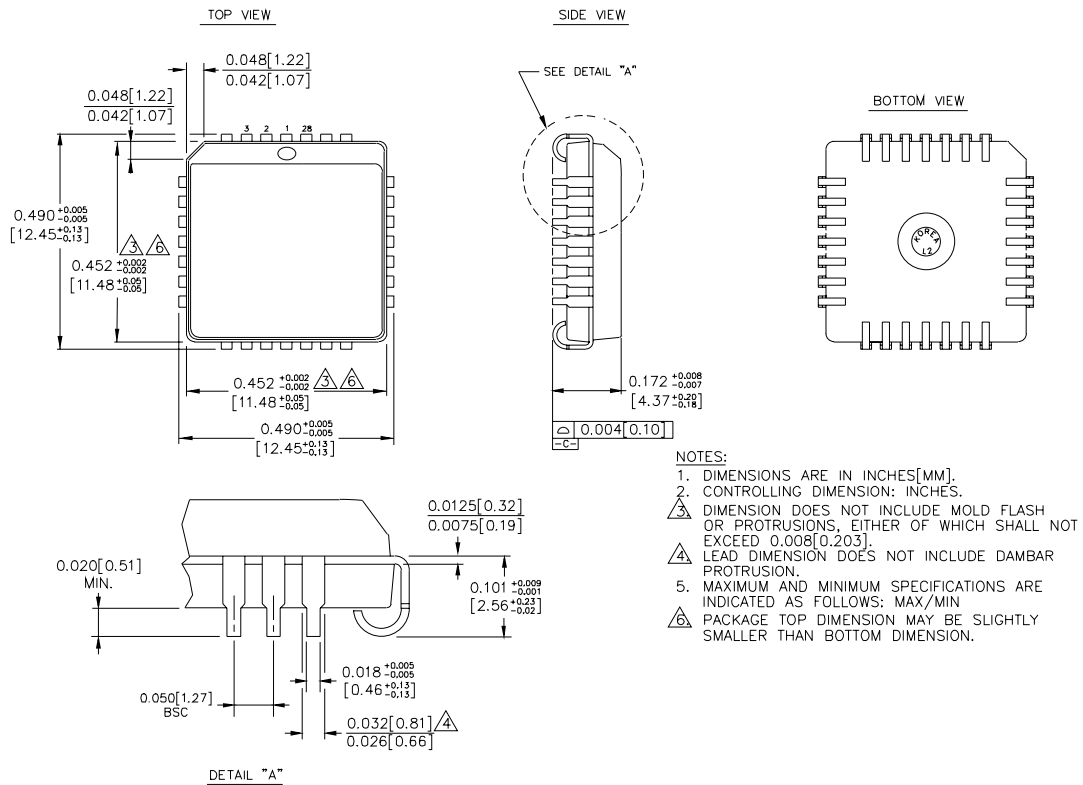
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E256JC	J28-1	Commercial
SY10E256JCTR	J28-1	Commercial
SY100E256JC	J28-1	Commercial
SY100E256JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

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