

FEATURES

- 900ps max. D to output
- Extended 100E VEE range of -4.2V to -5.5V
- 800ps max. LEN to output
- Differential outputs
- Asynchronous Master Reset
- Dual latch enables
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75K Ω input pulldown resistors
- Fully compatible with Motorola MC10E/100E156
- Available in 28-pin PLCC package

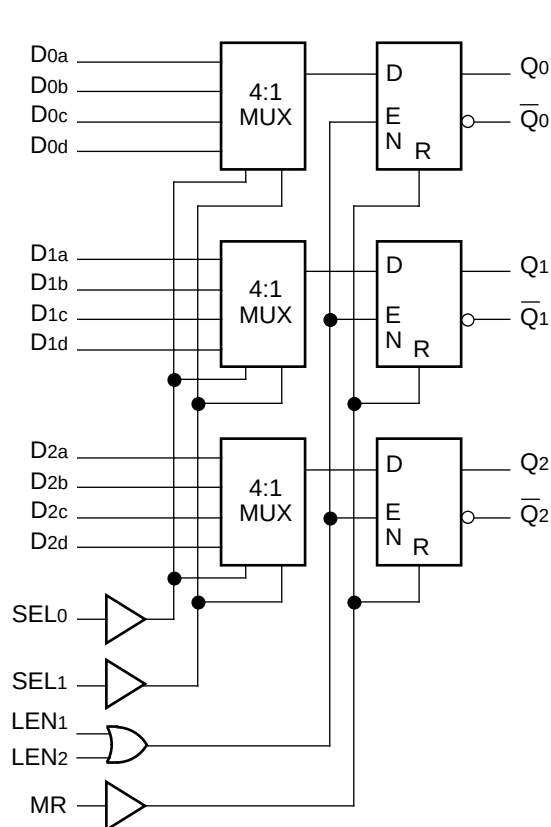
DESCRIPTION

The SY10/100E156 offer three 4:1 multiplexers followed by latches with differential outputs, designed for use in new, high-performance ECL systems. The two external latch enable signals (LEN1 and LEN2) are gated through a logical OR operation before use as control for the three latches. When both LEN1 and LEN2 are at a logic LOW, the latches are transparent, thus presenting the data from the multiplexers at the output pins. If either LEN1 or LEN2 (or both) are at a logic HIGH, the outputs are latched.

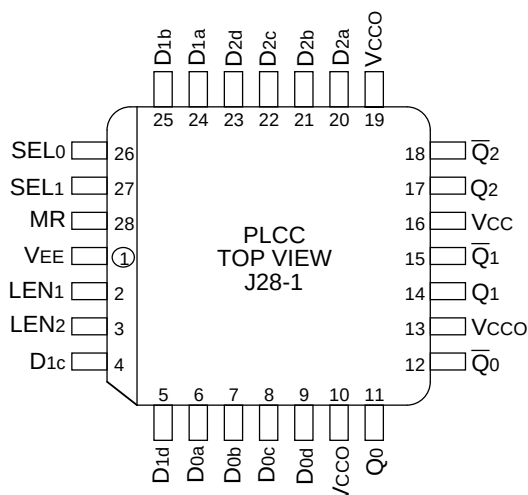
The multiplexer operation is controlled by the Select (SEL0, SEL1) signals which select one of the four bits of input data at each mux to be passed through.

The MR (Master Reset) signal operates asynchronously to take all outputs to a logic LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0x-D2x	Input Data
SEL0, SEL1	Select Inputs
LEN1, LEN2	Latch Enables
MR	Master Reset
Q0-Q2	True Outputs
Q0-Q2	Inverted Outputs
VCCO	Vcc to Output

TRUTH TABLES

LEN ₁	LEN ₂	Latch
L	L	Transparent
H	X	Latched
X	H	Latched

SEL ₀	SEL ₁	Data
L	L	a
H	L	b
L	H	c
H	H	d

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	75	90	—	75	90	—	75	90		
	100E	—	75	90	—	75	90	—	86	103		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output D SEL ₀ SEL ₁ LEN MR	400 550 450 350 350	600 775 650 500 600	900 1050 900 800 825	400 550 450 350 350	600 775 650 500 600	900 1050 900 800 825	400 550 450 350 350	600 775 650 500 600	900 1050 900 800 825	ps	—
t _s	Set-up Time D SEL ₀ SEL ₁	400 700 600	275 300 400	— — —	400 700 600	275 300 400	— — —	400 700 600	275 300 400	— — —	ps	—
t _H	Hold Time D SEL ₀ SEL ₁	300 100 200	–275 –300 –400	— — —	300 100 200	–275 –300 –400	— — —	300 100 200	–275 –300 –400	— — —	ps	—
t _{RR}	Reset Recovery Time	800	600	—	800	600	—	800	600	—	ps	—
t _{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t _{skew}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t _r t _f	Rise/Fall Time 20% to 80%	275	475	700	275	475	700	275	475	700	ps	—

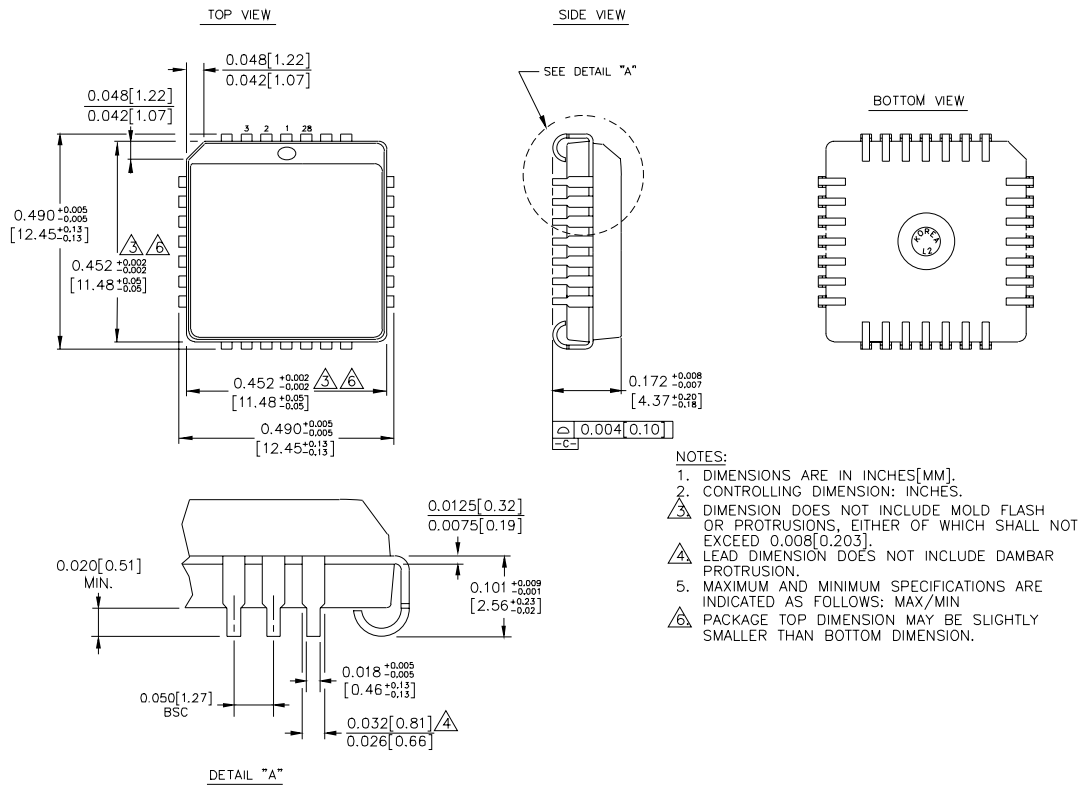
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E156JC	J28-1	Commercial
SY10E156JCTR	J28-1	Commercial
SY100E156JC	J28-1	Commercial
SY100E156JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



Rev. 03

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB <http://www.micrel.com>

This information is believed to be accurate and reliable, however no responsibility is assumed by Micrel for its use nor for any infringement of patents or other rights of third parties resulting from its use. No license is granted by implication or otherwise under any patent or patent right of Micrel Inc.

© 2000 Micrel Incorporated
