SIEMENS AG IC-SPECIFICATION

TDA 4362

Differences to the last edition

Last Edition: **DOK-Nr. V66047-S1603-C100-G1** date: **16.12.97**

Page 11: #P11: Test values and units changed
#P12: Test values and units changed
#P16: Test values changed, wrong values in previous version
Page 12: #P25,26: Min max values added
#P27: Load resistor added and values changed

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Table of Contents

AM- Updown - Conversion

This specification replaces the previous editions

DOK-Nr.	date	DOK-Nr.	date
V66047-S1603-C100-G1	16.12.97		

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Functional Description, Application

Dual-Conversion-AM-Receiver

The TDA 4362 is an integrated Dual-Conversion- AM-Receiver for use in car radios.

The input signal passes a linear mixer for conversion into the 1.IF (~10 MHz) . Via an external bandpass-filter (CER-filter, quartz filter) the 1. IF is converted in a second linear mixer to the 2. IF (~450kHz).

After an external narrowband-selectivity (CER-filter) the 2. IF passes an automatic gain controlled amplifier and is then demodulated to the AF.

For counter controlled search tuning stop (STS) the frequencies of the 1. LO and the 2. IF are available.

For Narrowband-FM-Demodulation a coincidence demodulator is implemented. A search tuning stop (STS) feature is also part of IC.

Features

- **High flexibility with an external preamplifier stage**
- **2 Symmetrical or asymmetrical mixer inputs**
- **2-Pin-Oscillator for the 1. LO**
- **1st LO with LC-tank circuit**
- **1st LO in, 60 to 160 MHz range**
- **Low narrow band noise**
- **Divider for 1st LO by 2, 4, 6, 8, 10, 12**
- **Integrated AGC generation for the prestages**
- **Strictly symmetrical RF path**
- **Decoupled direct and divided counter outputs**
- **2st LO with quartz or external source**
- **Output for gain controlled 2. IF**
- **FM-coincidence demodulator**
- **Two Inputs for the 2nd IF-Stage**

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Circuit Description

The integrated circuit includes 2-Pin oscillator (1st LO) with sym. input, buffered output and 2 double balanced mixers with symmetrical inputs. These stages convert the AM-Inputsignal to a 1st IF, which is much higher (~10 MHz) than the input frequencies. The 1st LO operates as a LC-varactor tuned oscillator in the same 100 MHz range like the FM-Tuner oscillator (e.g. TUA 4310 X) . So the same peripherial elements can be used.

Depending on the signal strength the prestage AGC controls PIN-Diode and MOSFET-prestage amplifiers.

The 1st IF passes an external selectivity and is then converted in a symmetrical double balanced mixer to the 2nd IF.

The 2nd LO operates as a quartz controlled oscillator or as an amplifier for an external forcing signal.

The 2nd IF signal passes an automatic gain controlled IF amplifier and is then demodulated to the AF in a quasi-synchronous-demodulator. Two inputs allow different CER-Filters in the signal path.

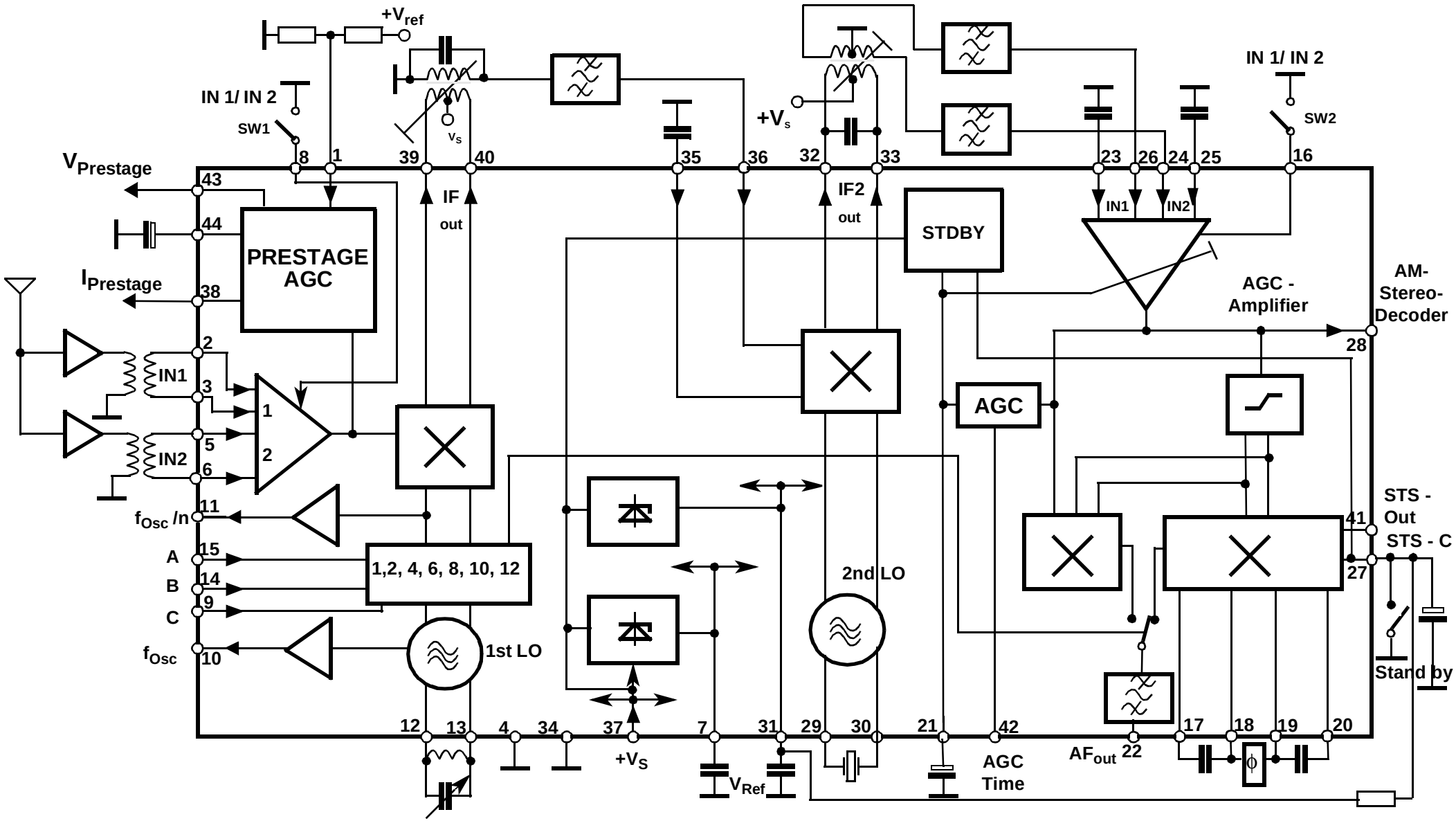
For the demodulation of Narrowband-FM-Signals a coincidence demodulator is implemented, in this mode the 2nd IF amplifier is working as a limiter.

For AM-Stereo application a gain controlled output of the 2nd IF is available.

The TDA 4362 is prepared to work with a PLL in the 100MHz range. When applied with a standard AM-PLL the oscillator frequency divided by 4, 6, 8, 10 or 12 has to be used. In this case a higher phase noise is to be expected.

The open collector output for search tuning stop (STS) is also controlled by this demodulator. For search tuning mode a fast AGC mode is added. In Narrowband FM search tuning mode the 2nd IF amplifier is working as AGC amplifier to provide a fieldstrength information.

Block Diagram



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Pin Assignment

Pin configuration

1. Prestage Threshold
2. Mixer 1 input
3. Mixer 1 input
4. Ground
5. Mixer 2 input
6. Mixer 2 input
7. Reference voltage (RF)
8. Mixer 1/Mixer 2 Switch
9. Counter Ratio C
10. Counter output direct
11. Counter output divided
12. Local Oscillator
13. Local Oscillator
14. Counter Ratio B
15. Counter Ratio A
16. LIF1 / LIF2 Switch
17. Coincidence Demodulator
18. Coincidence Phaseshifter
19. Coincidence Phaseshifter
20. Coincidence Demodulator
21. LIF Time Constant
22. AF Output
23. LIF Input 1 (blocked to LF GND)
24. LIF Input 2 active
25. LIF Input 2 (blocked to LF GND)
26. LIF Input 1 active
27. Search Tuning Stop Time constant , Stand by
28. AM Output
29. 2. LO Quartz
30. 2. LO Quartz
31. Reference Voltage (LF)
32. 2. Mixer Output
33. 2. Mixer Output
34. Ground (LF)
35. 2. Mixer Input
36. 2. Mixer Input
37. Supply Voltage
38. Prestage Current output
39. 1. Mixer output
40. 1. Mixer output
41. Search Tuning Stop output
42. AGC-Time constant Switch
43. Prestage Voltage output
44. Prestage Time constant.

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Pin Description

Pin 1:	**DC-Voltage alters the threshold voltage of the prestage AGC-circuit.**
Pin 2,3:	**Sym. input for the AM-Signal in the frequency range of 100 kHz to 160 MHz .**
Pin 4:	**GROUND: All DC-Values are referred to this pin. All RF blocking capacitors should be connected to this point.**
Pin 5,6:	**Sym. input for the AM-Signal in the frequency range of 100 kHz to 160 MHz .**
Pin 7:	**Output for the internal reference voltage. This pin is to be blocked with a ceramic capacitor to RF ground.**
Pin 8:	**DC input to activate mixer 1 or mixer 2.**
Pin 9,14,15:	**Input for the frequency divider. See Appendix A**
Pin 10:	**Buffered output for the oscillator frequency**
Pin 11:	**Buffered output for the by n divided (n= 8 or 10) Oscillator frequency**
Pin 12,13:	**The ext. LC-Circuit determines the oscillator frequency**
Pin 16:	**DC input to activate LIF1 or LIF2 inputs.**
Pin 17,20:	**Inputs to the coincidence demodulator.**
Pin 18,19:	**Phase shifter for FM-Discriminator**
Pin 21:	**Blocking capacitor for the IF-AGC-Circuit to suppress AF-frequencies**
Pin 22:	**Buffered AF output**
Pin 23,26:	**Input-Pins for the DC-coupeled AGC-Amplifier 1.**
Pin 24,25:	**Input-Pins for the DC-coupeled AGC-Amplifier 2.**
Pin 27:	**Blocking capacitor to ground**
Pin 28:	**Buffered output for the AGC-controlled lower IF-Signal. This pin is connected to the AM-Stereo-Decoder.**
Pin 29,30:	**Input for the 2nd Local oscillator (LO). The pins can be connected via a quartz or the oscillator is to be forced with an ext. signal**
Pin 31:	**Output for the internal reference voltage. This pin is to be blocked with a ceramic capacitor to ground. All LF blocking capacitors should be connected to this point.**
Pin 32,33:	**Open collector output of mixer 2 for the lower IF (~450 kHz)**
Pin 34:	**GROUND: All LF blocking capacitors should be connected to this point.**
Pin 35,36:	**Sym. mixer 2 input for the upper IF (~10.7 MHz). Asym. operation is possible. The input signal is converted to the lower IF corresponding the equation $f_{LIF} = f_{UIF} - f_{2.LO}$**
Pin 37:	**Supply-voltage. This point is to be blocked to ground for AF and for RF-Signals**
Pin 38:	**Current output for PIN-Diode controlling in the prestage.**
Pin 39,40:	**Sym collector output of the mixer 1. The external tank circuit is tuned to the upper IF.**
Pin 41:	**Open collector output for STS**
Pin 42:	**DC-Voltage determines the AGC-Time GND: normal mode Vref: fast mode**
Pin 43:	**Buffered prestage AGC output**
Pin 44:	**Blocking capacitor for the prestage AGC**

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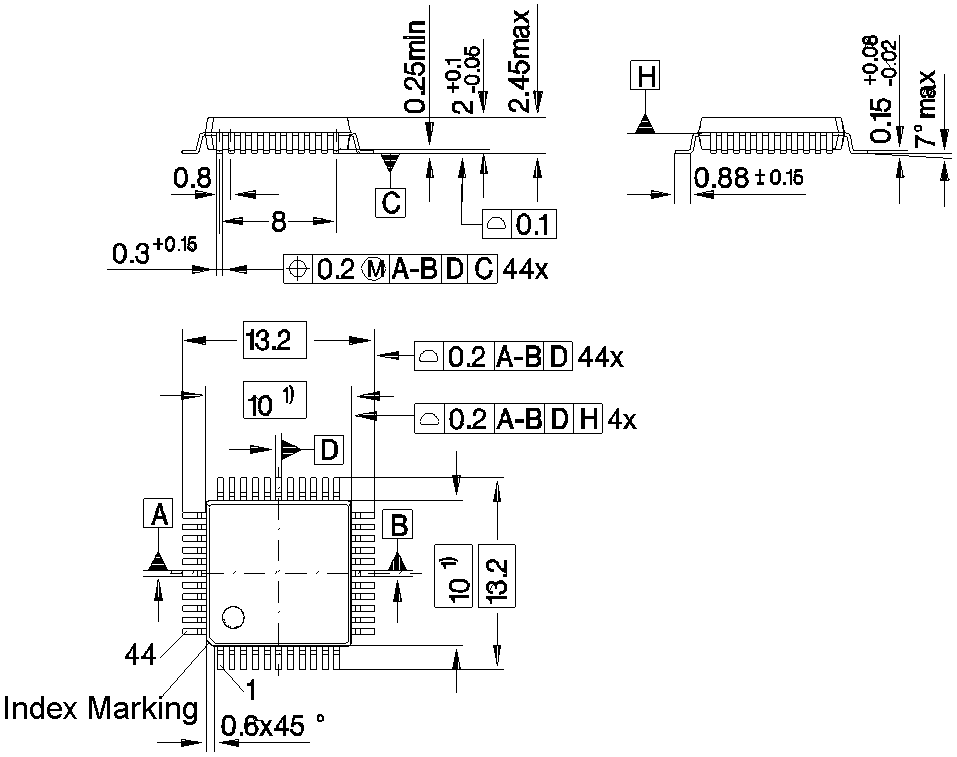
Package Outline

Plastic Package
P-MQFP-44-2



Does not include plastic or metal protrusion of 0.25 max. per side

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Absolute Maximum Ratings

The maximal ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

#	Max. Ratings for ambient temperature T_{amb} -40°C to 85°C	Symbol	Min	Max	Units	Remarks
1	Supply voltage	V_{37}	0	13.2	V	
2	Reference voltage	$V_{7,31}$	0	5	V	
3	Reference current	$I_{7,31}$	0	1	mA	
4	Prestage threshold	V_1	0	5	V	
5	Mixer 1 input	V_2, V_3	0	5	V	
6	Mixer 2 input	V_5 , V_6	0	5	V	
7	Switch for Mixer, LIF input	V_8 , V_{16}	0	13.2	V	
8	Logical divider input	V_9 , V_{14}, V_{15}	0	13.2	V	
9	Counter output	V_{10}	0	13.2	V	
10	Divided counter output	V_{11}	0	13.2	V	
11	1.LO	V_{12}, V_{13}	0	5	V	
12	Coincidence demodulator	V_{17} , V_{18} V_{19} , V_{20}	0	5	V	
13	Time constant for 2 IF AGC	V_{21}	0	5	V	
14	Leakage current	I_{21}		1	µA	
15	AF-output	V_{22}	0	13.2	V	
16	AGC-Timer constant	V_{27}	0	5	V	
17	AGC 1 input	V_{23} , V_{26}	0	5	V	
18	AGC 2 input	V_{24} , V_{25} , V_{27}	0	5	V	
19	AM-Stereo output	V_{28}	0	13.2	V	
20	2. LO input	$V_{29,30}$	0	5	V	
21	2. Mixer output	$V_{32,33}$	0	5	V	
22	2. Mixer input	$V_{35,36}$	0	5	V	
23	PIN-Diode output	V_{38}	0	5	V	
24	1. Mixer output	$V_{39,40}$	0	13.2	V	
25	STS-Output	V_{41}	0	13.2	V	
26	AGC-Time	V_{42}	0	13.2	V	
27	Prestage AGC	V_{43}	0	13.2	V	
28	PrestageTime constante	V_{44}	0	13.2	V	
29	ESD voltage human body modul 100 pF/1500 Ω	V_{ESD}	-2	+2	kV *)	
30	Thermal Resistance	Rthst		65	k/W	

***) 2 kV ESD protection is not valid for pin 29 and 30.**

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Operational Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

#	Parameter	Symbol	Min	Max	Units	Remarks
1	Supply Voltage	V_{37}	7.5	13.2	v	
2	Ambient temperature	T_{amb}	-40	+85	°C	

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AC / DC Characteristics

AC / DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

#	Parameter	Symbol	Test Conditions	Test Circuit	Min	Typ	Max	Units
	Supply voltage		V_S=8.5V					
	Ambient temperature		T_{amb}= 25 °C					
			f_i= 1 MHz ; f_{IF1}= 10.7 MHz ; f_{IF2}= 450 kHz					
			Divided by n= Appendix A					
1	Current consumption	I_{37}+ I_{32}+I_{33}+ I_{39}+I_{40}	n=12,V_{42}=0	1	50	62	77	mA
Mixer 1 RF								
2	Interceptpoint 3. Order	IP3	$\|V_2-V_3\|$	Lab		130		dBµV
3	Mixer gain	v	20 lg V_{36} / $\|V_2-V_3\|$	1	0	2	4	dB
4	Max. input voltage	$\|V_2-V_3\|$	for -1 dB compression	1			600	mV_{pp}
5	Noise figure (10 MHz)	F		Lab			10	dB
Mixer 2 RF								
6	Interceptpoint 3. Order	IP3	$\|V_5-V_6\|$	Lab		130		dBµV
7	Mixer gain	v	20 lg V_{36} / $\|V_5-V_6\|$	1	0	2	4	dB
8	Max. input voltage	$\|V_5-V_6\|$	for -1 dB compression	1			600	mV_{pp}
9	Noise figure (10 MHz)	F		Lab			10	dB
10	Tracking mixer 1/2	$dv_{M1/2}$		1		0		dB
1st LO								
11	Frequency range	$f_{1.LO}$		1	60		160	MHz
12	Counter output	V_{10}	R_L=330Ω	1	70	100		mV_{rms}
13	Divided counter output	V_{11}	R_L=330Ω	1	35	50		mV_{rms}
14	Output impedance	R_{ex10}		Lab		330		Ω
15	Output impedance	R_{ex11}		Lab		330		Ω
Converter IF								
16	Mixer gain	V		1	2	5	8	dB
17	Noise figure (10 MHz)	F		Lab			10	dB
18	Max. input voltage	$\|V_5-V_6\|$	for -1 dB compression	1			600	mV_{pp}
2. LO								
19	Frequency range	$f_{2.LO}$		1	25			MHz
20	External force voltage	V_{29}		1	60			mV_{rms}
Prestage AGC output								
21	AGC-Voltage	U_{43}	V_1= 2.4; $\|V_2-V_3\|$=100mV_{rms}	1	6.3	7.2	Vs	V
22	AGC-Voltage	U_{43}	V_1= 4.4; $\|V_2-V_3\|$=100mV_{rms}	1		0.7	1	V
23	AGC-Current	I_{38}	V_1= 2.4; $\|V_2-V_3\|$=100mV_{rms}	1		12		mA
24	AGC-Current	I_{38}	V_1= 4.4; $\|V_2-V_3\|$=100mV_{rms}	1		0.1		mA

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AC / DC Characteristics

AC / DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

#	Parameter	Symbol	Test Conditions	Test Circuit	Min	Typ	Max	Units
25	Integrator current	I_{44}	$\|V_2-V_3\|=0mV_{rms}$	1		-30		µA
26	Integrator current	I_{44}	$\|V_2-V_3\|=200mV_{rms}$	1		30		µA

***) integrator currents are measured between the output pin (- Pole of the measurement equipment and a voltage source with a value of $3V_{DC}$ (+ Pole)**

AGC-Amplifier			$V_i= \|V_{25}-V_{26}\|$					
23	AGC-Range			1	60	66		dB
24	AGC-Voltage	V_{21}	$V=0\ mV_{rms}$	1			1	V
25	AGC-Voltage	V_{21}	$V=500\ µV_{rms}$	1	1.1	1.45	1.8	V
26	AGC-Voltage	V_{21}	$V=30\ mV_{rms}$	1	2.7	3.1	3.7	V
27	reg. output voltage	V_{28}	$R_L=100k\Omega$	1	48	60		mV_{rms}
28	Input sensitivity	V_{22}	$V_{22\|100mV}$ - 3dB	1		100		$µV_{rms}$
29	AGC-current	I_{21}	$V_i=100mV_{rms}$ AGC=fast	1	400	500	650	µA
30	AGC-current	I_{21}	$V_i=\ 0mV_{rms}$ AGC=fast	1	-400	-500	-660	µA
31	AGC-current	I_{21}	$V_i=100mV_{rms}$ AGC=slow	1	15	25	35	µA
32	AGC-current	I_{21}	$V_i=\ 0mV_{rms}$ AGC=slow	1	-13	-25	-33	µA
AM-Demodulator			$V_{i1}= \|V_{23}-V_{26}\|$, $V_{i2}= \|V_{24}-V_{25V}\|$					
33	AF output voltage	V_{22}	V_{i1},V_{i2}, m=0.3	Lab		180		mV_{rms}
34	AF output voltage	V_{22}	V_{i1},V_{i2}, m=0.8	1	400	480	560	mV_{rms}
35	Total harm. distortion	k	V_{i1},V_{i2}, m=0.8	1		1	1.7	%
36	Input voltage for S+N/N=6 dB	V_{22}	V_{i1},V_{i2}, m=0.3	Lab	10			$µV_{rms}$
37	Input voltage for S+N/N=26 dB	V_{22}	V_{i1},V_{i2}, m=0.3	Lab	100			$µV_{rms}$
38	S+N/N		V_{i1},V_{i2}=10 mV, m= 0.8	1	58	64		dB
39	AF-Linearity	ΔV_{22}	100µV/100 mV	1			3	dB
FM-Demodulator			fi_{RF}=450 kHz, AGC=slow, $V_{i1}= \|V_{23}-V_{26}\|$, $V_{i2}= \|V_{24}-V_{25V}\|$, CCIR					
40	FM-Output voltage	V_{22}	Δf= 2.5 kHz	1		180(tbd)		mV_{rms}
41	Limiter threshold	V_{22}	$V_{22\|100mV}$ -3 dB	1		60		$µV_{rms}$
42	S+N / N		V_{i1},V_{i2}= 10 mV_{rms}	1		65(tbd)		dB
STS			Δf_{STS}=3 kHz, U_i=10 mV_{rms} R_{STS}=330 k to Us					
43	STS-out	V_{41}	$f_{IF} + \Delta f_{STS}$	1		8.5		V
44	STS-out	V_{41}	f_{IF}	1			0.2	V
45	STS-out	V_{41}	$f_{IF} - \Delta f_{STS}$	1		8.5		V

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AC / DC Characteristics

AC / DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

#	Parameter	Symbol	Test Conditions	Test Circuit	Min	Typ	Max	Units
	MODES							
	Divider Ratios PORTS ABC							
46	Input voltage "L"	V_9, V_{14}, V_{15}		1	0		1.5	V
47	Input voltage "H"	V_9, V_{14}, V_{15}	s. Appendix A	1	3.0		V_S	V
	MIXER 1 / MIXER 2 SW 1							
48	Mixer 2 active, Mixer 1 passiv	V_8	s. Appendix A	1	2.0		V_S	V
49	Mixer 1 active, Mixer 2 passiv	V_8		1	0		1.4	V
	LIF 1 / LIF 2 SW 2							
50	LIF 1 active, LIF 2 passiv	V_{16}	s. Appendix A	1	0		1.2	V
51	LIF 2 active, LIF 1 passiv	V_{16}		1	2.0		V_S	V
	Standby							
52	Standby active	V_{27}	Standby	1	0	0.7	1.0	V
53	Standby current	I_{37}		1		1		mA
	AGC-Times							
54	Fast	V_{42}		1	2.0		V_S	V
55	Slow	V_{42}		1	0		0.7	V
	Reference voltage							
56	Reference voltage AM	V_{31}		1	4.5	4.8	5.1	V
57	Reference voltage FM	V_7		1	4.5	4.8	5.1	V

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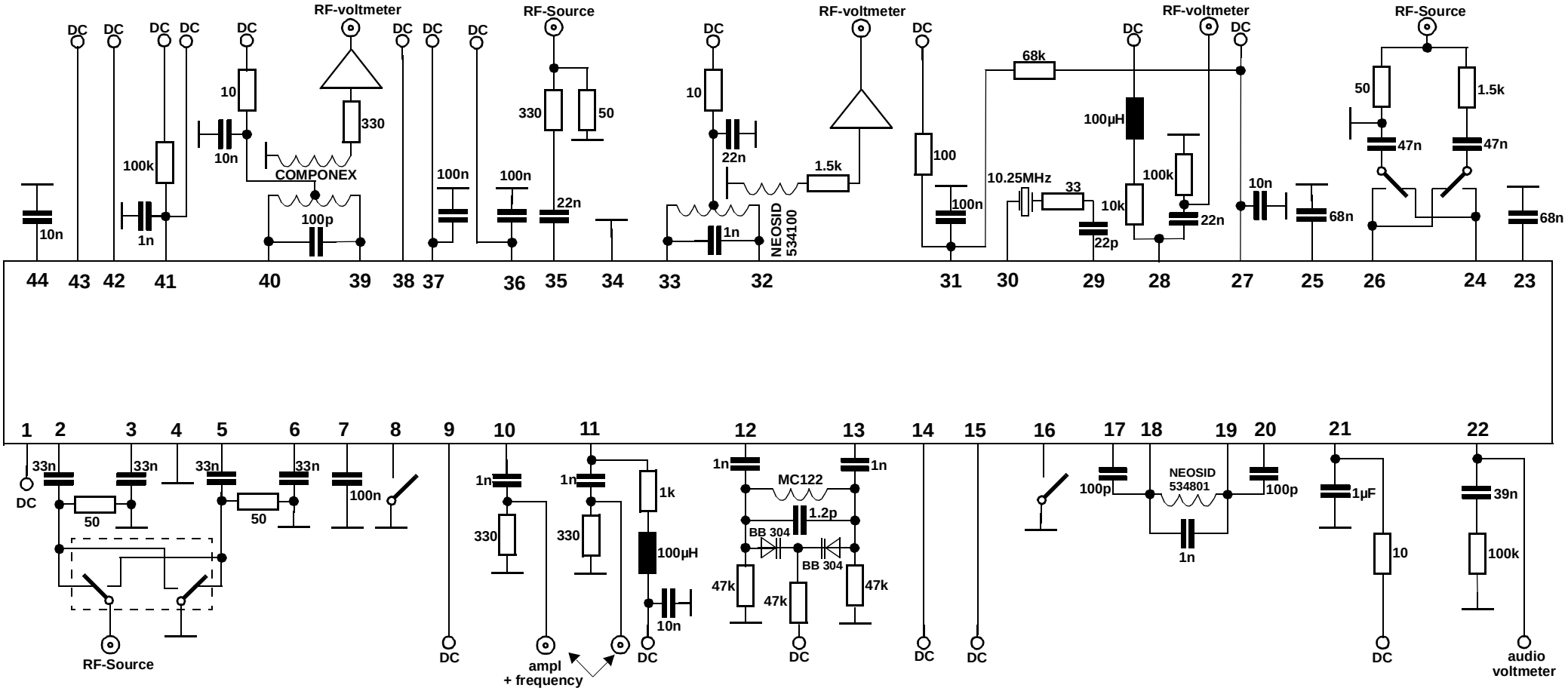
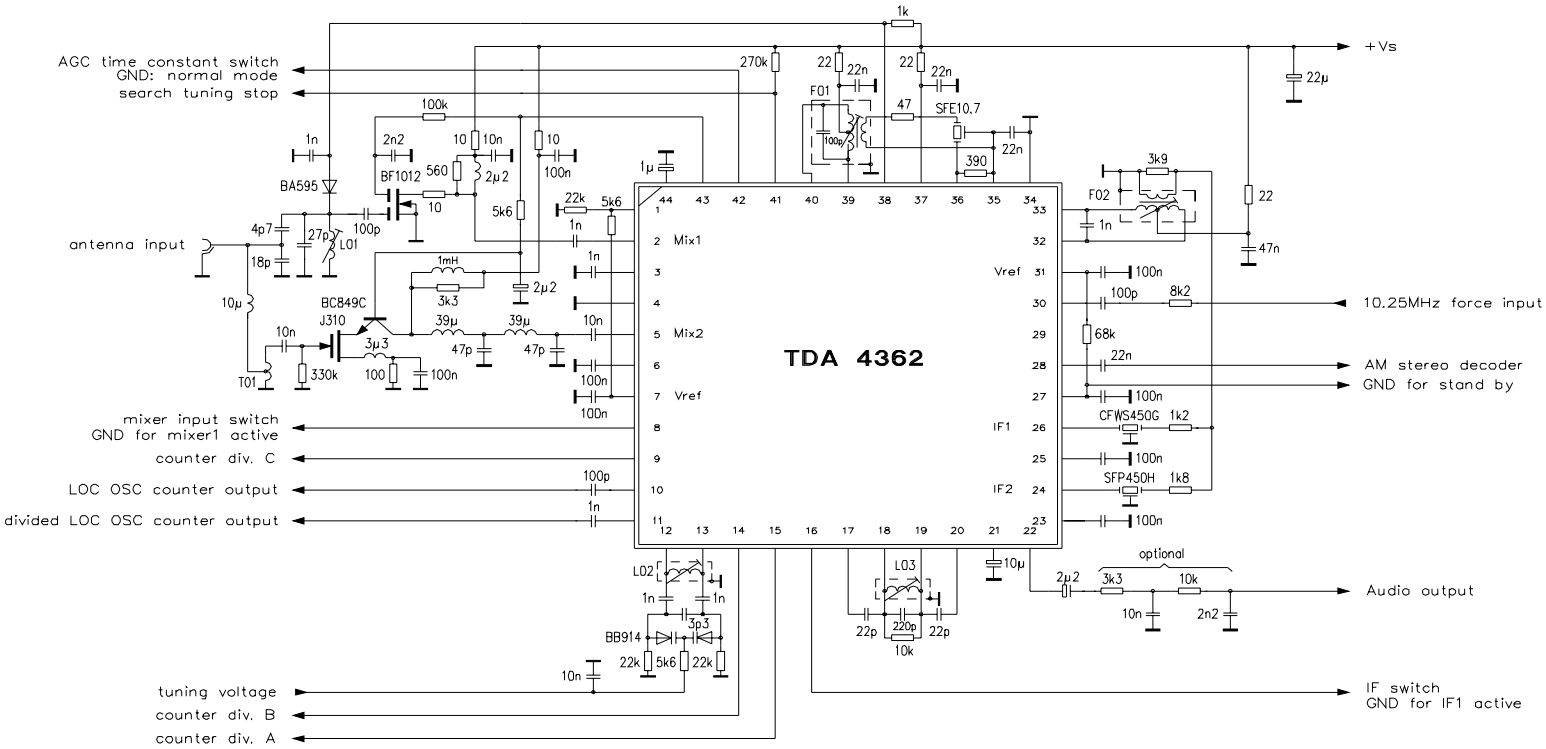
Test Circuit



Application Circuit



Appendix A

Tabelle 1: Divider Ratios n

n	1	2	4	6	8	8	10	12
A	0	1	1	0	1	1	0	0
B	0	1	1	1	0	0	1	0
C	0	0	1	1	1	0	0	1

SW 1 = H : Mixer 2 active Inputs: pin 5 ; 6
SW 1 = L : Mixer 1 active Inputs: pin 2 ; 3

SW 2 = L : LIF-pin 26 (signal); LIF-pin 23 (blocked to LF - GND)
SW 2 = H : LIF-pin 24 (signal); LIF-pin 25 (blocked to LF - GND)

AGCT= L : Normal Mode: slow AGC mode
AGCT= H : STS Mode : fast AGC mode

STDBY= L : Standby
STDBY= open : Normal Mode

With n=1 the FM demodulator is active and the gain of the AGC amplifier is maximum, except AGCT=H