February 2000

SuperH™ RISC engine

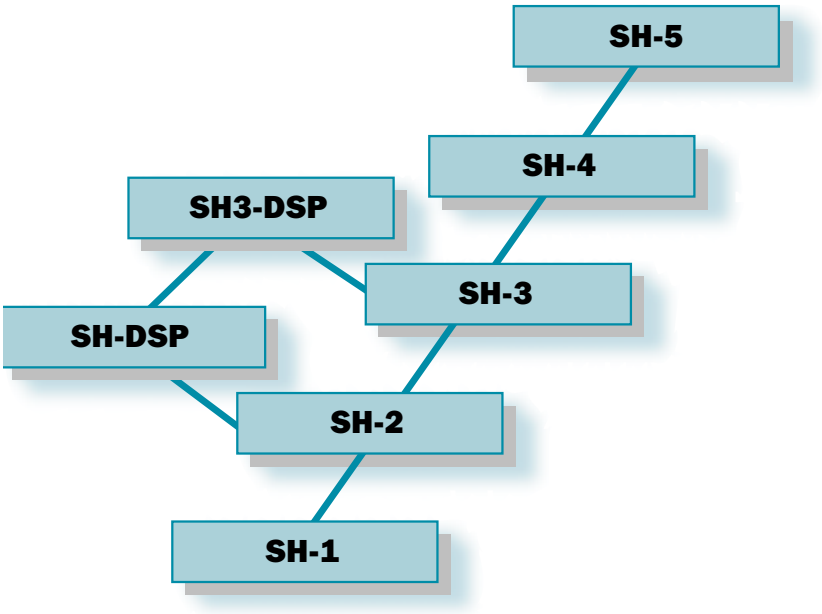
32-bit microcontrollers and microprocessors

System Solutions

HITACHI

SuperH™ RISC engine

introducing the SuperH™ family



Reader's Guide

This document provides an overview of Hitachi's 32-bit SuperH™ embedded microcontrollers and microprocessors. This document includes 3 main sections. The 1st covers general overviews and some background information. The 2nd introduces the SuperH™ CPU architecture providing an overview of the most relevant technical details. Finally, section 3 provides in-depth discussions of the individual SuperH™ series. You will also find tables helping you to select the right SuperH™ device for your application.

We strongly recommend you read all sections before making your decision.

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Welcome

Creating the information society with all its new products and services is one of the biggest challenges of this decade. As one of the major players in the global electronic's industry, Hitachi is committed to play a very active role to build this information society.
Hitachi's general strategy is working closely together with its customers at the leading edge for all of its products and services while providing a maximum of quality and reliability.
Advanced and next-generation microprocessors play a very important role in products and services for the information society. Hence, Hitachi developed an advanced 32-bit RISC processor family called SuperH™.
This 32-bit processor family is based on a broad range of devices optimised for a wide variety of applications.
It is not sufficient just to provide leading-edge technology to make processors a success. With this in mind, Hitachi also offers technical support, software, and tools helping customers and partners get their products on the market. What is more, Hitachi even establishes global partnerships to enhance support and quality of products and services.
This explains that the SuperH™ 32-bit processor family is one of the leading architectures in the world.
Currently offering devices from 10 to 360 MIPS, the SuperH™ series can be used as basis for low-end embedded control applications up to high-end products with stringent performance requirements.
When offering SuperH™ solutions to our customers we benefit from the wide knowledge we collected by developing and marketing 4-, 8- and 16-bit embedded controllers, LCD controllers, ASIC technology, memory devices, and LCD displays.
The next pages will guide you through the most important features of Hitachi's SuperH™ 32-bit embedded microcontroller and microprocessor family and will provide useful background information.

SuperH™ Architecture **Evolution**

Choosing a microprocessor leads to a long-term relationship between user and microprocessor provider. Thus, several criteria play a decisive role for the success of a microprocessor architecture. It is not only the technical leadership, it is also the support environment as well as the processor roadmap where users have to co-operate with the provider for a long time. The facility to switch from low-cost to a very high-performance device with a minimum of redesign effort can be a crucial factor for the future success.

This is not restricted to, but especially true for the 32-bit embedded domain. Maybe the most important feature of the SuperH™ processor family is the availability of a series of upward compatible architectures being optimised for a lot of different applications and markets.

The SuperH™ - also simply called SH - provides even object-code upward compatibility throughout the family. Based on a common 32-bit RISC architecture, Hitachi developed the SH-1 architecture, further extended by SH-2, SH-3 and SH-4. The SH-1 architecture has been created for 32-bit embedded control applications requiring a high performance at very low costs combined with an integration of peripherals and on-chip RAM and ROM. The SH-2 enhances the SH-1 mainly by offering an extended instruction set and a cost-optimised cache mechanism.

The higher performance SH-3 features an extended SH-2 instruction set, a memory management unit, additional register banks, extended cache mechanisms and dedicated peripherals.

The SH-4 is currently introduced to give the user a maximum of throughput and performance for next generation high-end embedded multimedia applications.

When writing code for the SH-1 it can be re-used in object-code format even for the SH-4. This kind of software re-usability helps Hitachi to shorten the design-cycle of new products and helps partners to stay at the forefront of application development while reducing the overall costs.

Based on these architectures, Hitachi offers leading-edge 32-bit microcontrollers and processors and is steadily developing further products to ensure that you are always at the leading edge.

Hitachi is also a forerunner in combined CPU and Digital Signal Processor (DSP) architectures. The SH-DSP and SH3-DSP architectures feature an integrated single architecture approach for general purpose microcontroller and DSP tasks. While the SH-DSP extends the instruction set of the SH-1 and SH-2, the SH3-DSP's instruction set is a superset of SH-1, SH-2, SH-3 and SH-DSP, also offering instruction set upward compatibility.

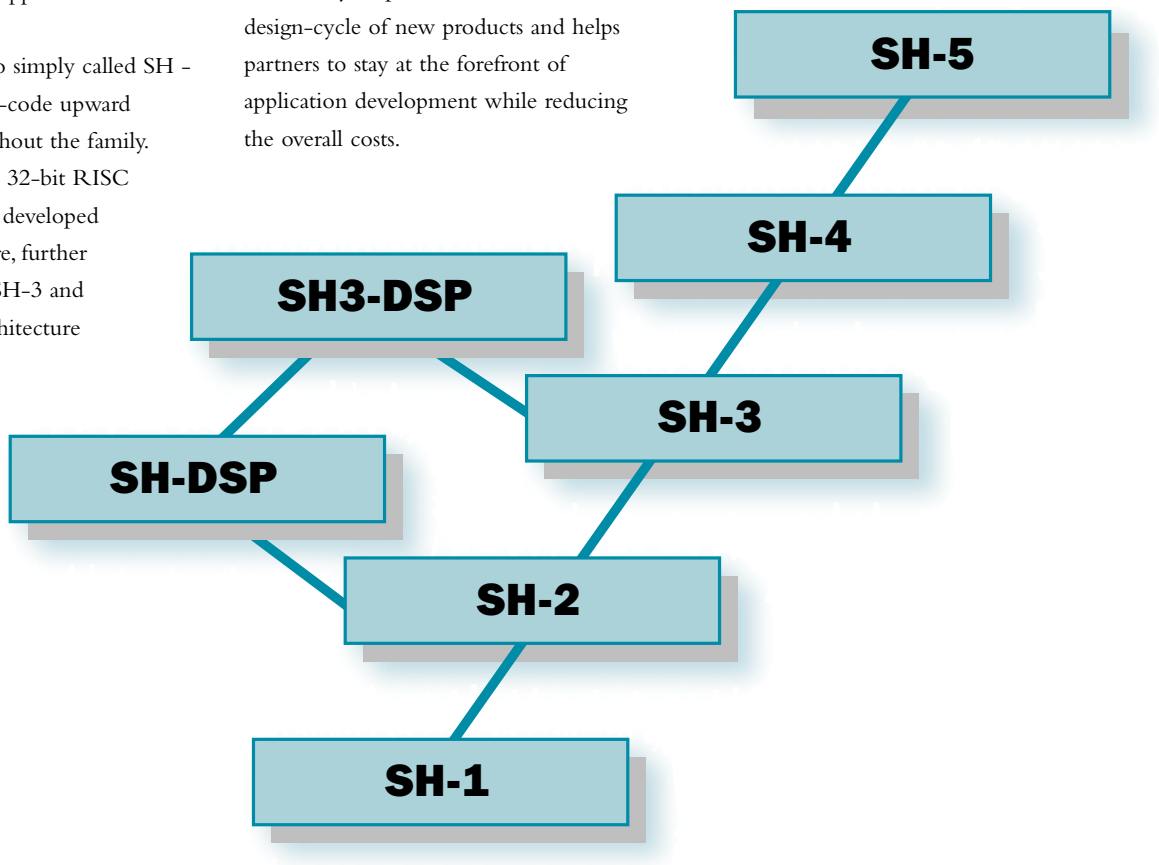


Figure 1: SuperH™ Architecture Evolution

SuperH™ Family of 32-bit **Microcontrollers** and **Microprocessors**

The previously introduced SuperH™ family is defined by the main line SH-1 to SH-4 and includes a sub-line, the SH-DSP and SH3-DSP architecture line. These architectures can be separated into a major embedded controller line and an embedded processor line. The embedded controller line is based on the SH-1, SH-2, and SH-DSP architectures, the embedded processor line on the SH-3, SH3-DSP and SH-4 architecture. Figure 2 provides an overview of the individual implementations separated into the aforementioned controller and processor line and gives a first indication of the performance of the individual devices. Several lines have been designed to offer cost reductions by integrating special application-oriented peripherals for dedicated markets. Users can chose from a huge number of compatible devices and derivatives. Thus, users will find members of the SuperH™ family for industrial automation as well as for multimedia applications such as video game consoles and lots of other applications.

Because of the compatibility across the family, users have the security of finding the right device for different applications while reducing the costs of redesign or learning curves to a minimum.

SuperH™ represents a family of devices which focused right from the start and across all family members on low-power consumption, high code density, high level of integration and system cost reduction.

Thus, members of the SuperH™ product family are leaders in the 32-bit embedded arena in terms of power consumption (MIPS/Watt), code density and system costs.

While spanning a range from 10 to 360 MIPS, the SuperH™ family offers devices for nearly all 32-bit embedded applications.

Besides offering standard devices such as the SH7040 line (see below)Hitachi is also a leader in ASIC technology. With the CBIC and µCBIC approach Hitachi created the basics to enable efficient ASIC design and system-on-a-chip solutions based on the SuperH™ CPU core family. A library of state-of-the-art modules and an open system design approach enables Hitachi together with customers to provide optimised controller solutions in a very early stage of the overall product design cycle.

The µCBIC approach is not restricted to the 32-bit SuperH™ CPU core family, also 16-bit H8/300H and H8S cores are available for further integration.

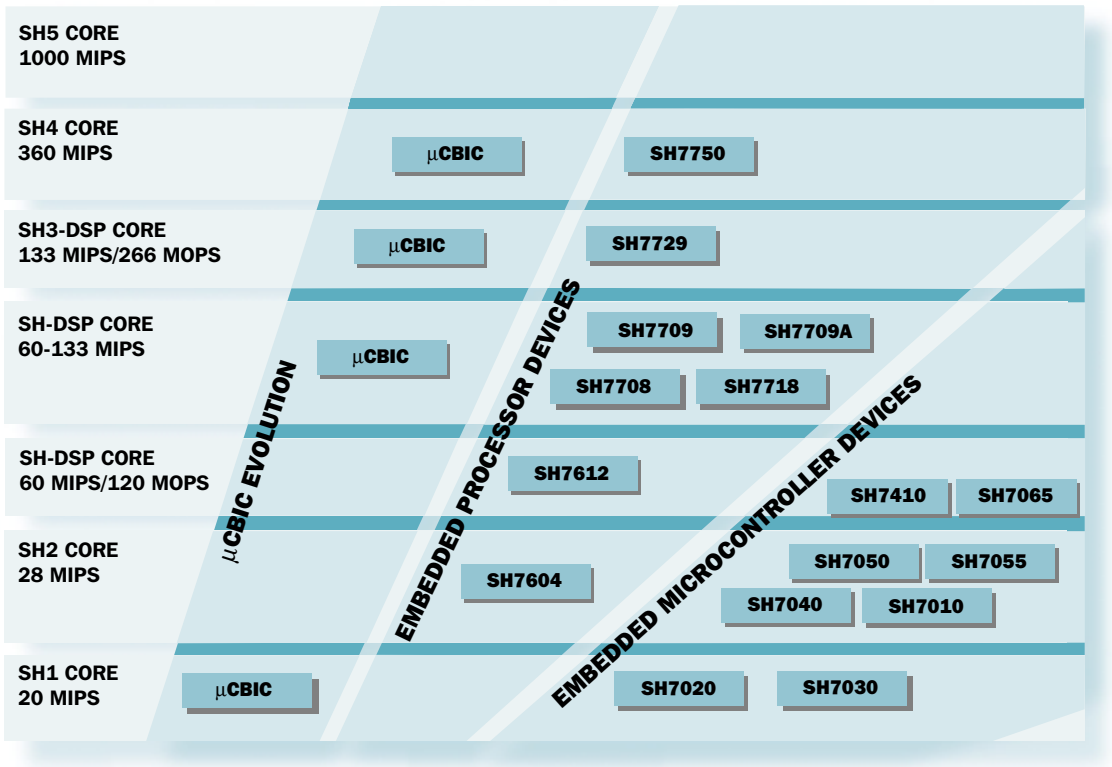


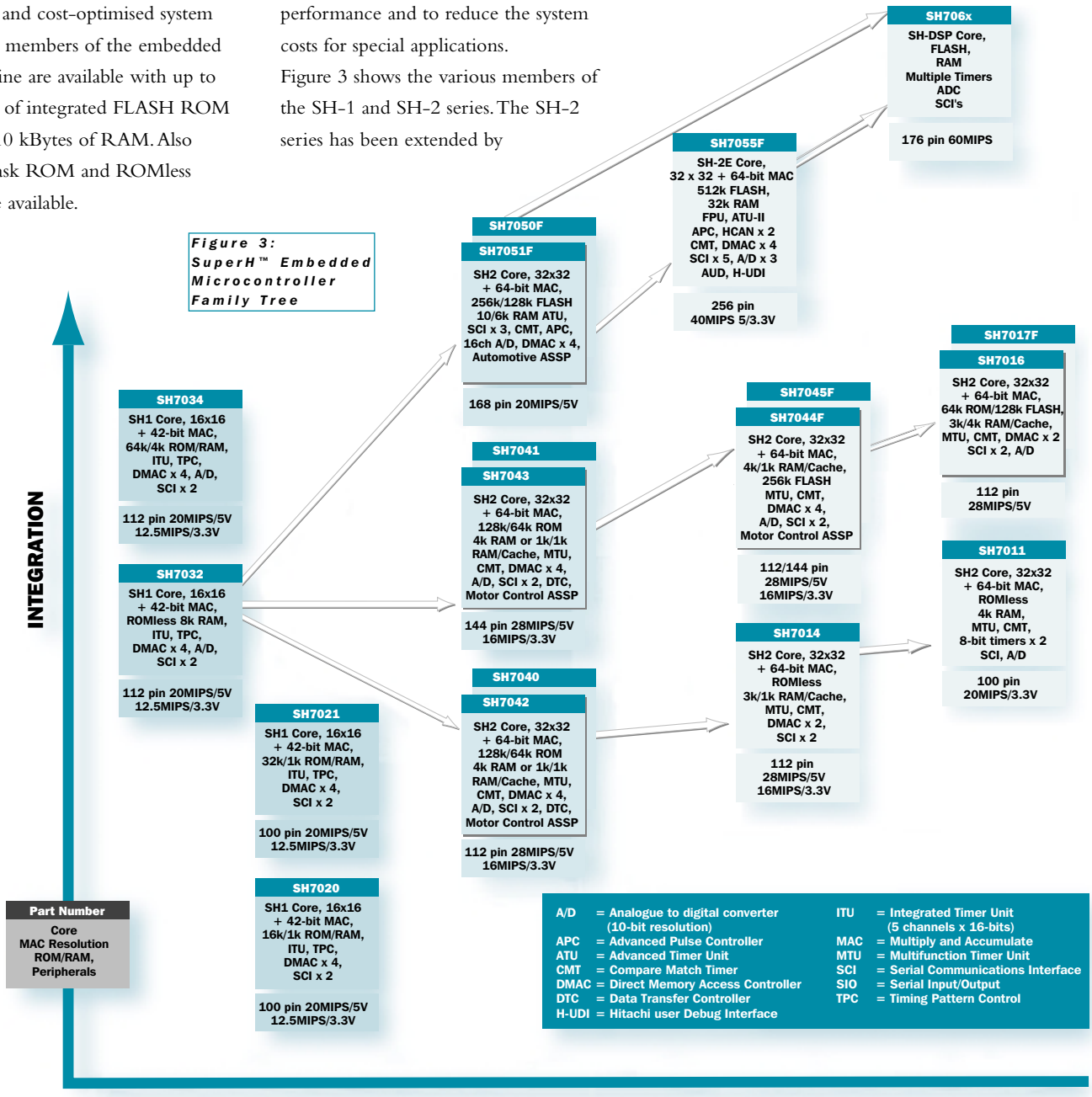
Figure 2: SuperH™ CPU Family Overview

SuperH™ 32-bit **Embedded** Controllers

Embedded Controllers need a clear focus on high integration, high code density, as well as low power consumption. The SH-1, SH-2, and SH-DSP have been designed and are continuosly further developed for the 32-bit embedded control market. Thus, the SH 32-bit embedded controller line focuses on integrated memory, integration of peripherals and cost-optimised system design. The members of the embedded controller line are available with up to 256 kBytes of integrated FLASH ROM and up to 10 kBytes of RAM. Also PROM, mask ROM and ROMless versions are available.

Cost plays the decisive role throughout the embedded controller line. A set of peripherals integrated into the members of the series provides glueless connection to a huge variety of external devices or even makes external devices obsolete in many cases. Several members of the SH-2 series have been designed for dedicated applications to even improve the performance and to reduce the system costs for special applications.
Figure 3 shows the various members of the SH-1 and SH-2 series. The SH-2 series has been extended by the SH-DSP series offering an extended instruction set to serve the need for additional DSP performance with a single architecture.

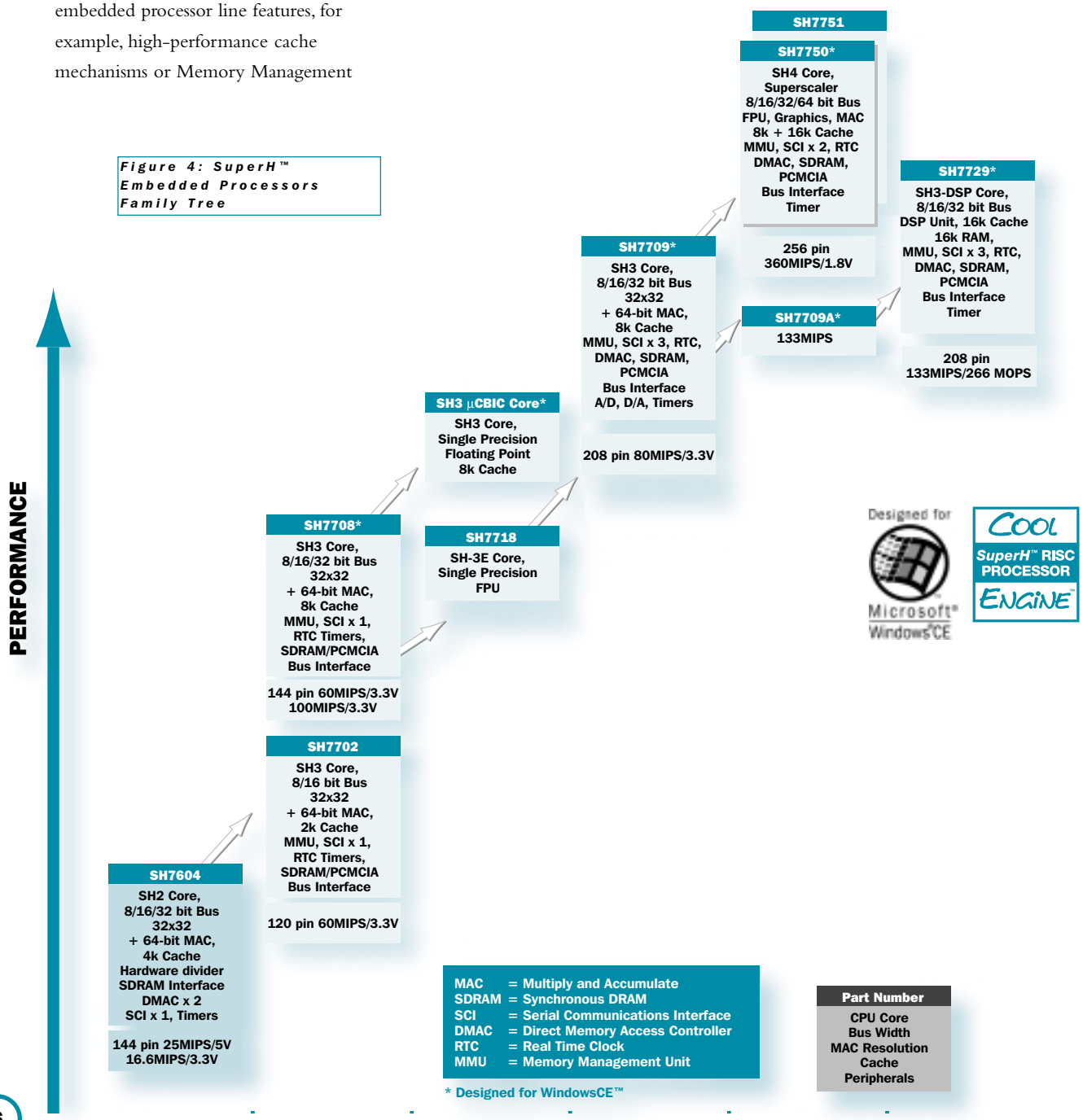
Figure 3: SuperH™ Embedded Microcontroller Family Tree



SuperH™ 32-bit **Embedded** Processors

The SuperH™ embedded processor line of Hitachi has been designed to match the needs of advanced embedded computing requirements. Starting with the SH-3 architecture, extended by the SH3-DSP and the SH-4 CPU core a set of compatible devices has been created for the needs of embedded processor applications of today. The SuperH™ embedded processor line features, for example, high-performance cache mechanisms or Memory Management Units and other peripherals. Members of the embedded processor line have been designed for consumer applications such as PC companions or other handheld devices. Other application areas are telecommunication, multimedia and automotive applications. Figure 4 gives an overview of the various members of the embedded processor line. The SuperH™ embedded processor line is a leader in the Windows® CE area offering optimised and complete system solutions for PC companions as well as other Windows® CE based systems.

Figure 4: SuperH™ Embedded Processors Family Tree



SuperH™ **Market** View

The SuperH™ CPU family is one of the most successful architectures in the 32-bit embedded domain. With shipments of roughly 20 million units per year (based on 1997 data) the SuperH™ family has a broad customer base using these devices in a huge variety of applications.
Hitachi is also the second biggest supplier of 16-bit microcontrollers to the European market (according to Dataquest), as well as the third for 4-bit, sixth for 8-bit. Hitachi produces and ships over 12 million H8 microcontrollers every month, this includes almost 4 million H8 Flash devices.
Hitachi semiconductor products are used all over the world and Hitachi offers services and support in nearly all corners of the world. This ensures a proper worldwide sales and support service helping the customers to shorten the design cycle and to get the right support in time. Hitachi partner's providing third-party assistance and support can also be found throughout the world providing additional resources and capacities for your system design based on SuperH™.

At Hitachi, we went even further by setting up a European engineering and tool design subsidiary 12 years ago: Hitachi Microsystems Europe (HMSE) based in Maidenhead (UK).

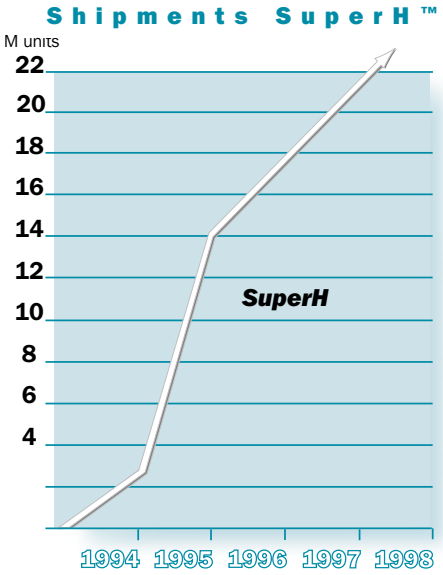


Figure 5: SuperH™ Shipments over the years

HMSE provides our customers with locally designed and supported tools ranging from low cost evaluation boards to fully featured real time emulators based on IBM-compatible PC's at a very competitive price. Software ranges from Assembler, an ANSI C-Compiler via a C-level debugger to MakeApp, a tool that sets up peripherals and creates driver routines on the click of a mouse.
HMSE also offers support and engineering resources for customers wishing to use Hitachi's ASIC capabilities. This also applies to our µCBIC program, enabling our customers to select one of Hitachi's CPU cores and combine it with peripherals from our library and adding customer specified logic via VHDL or Verilog.
In addition, Hitachi is also establishing strategic partnerships with other key players in the embedded world to ensure the future success and evolution of the product lines in the growing embedded marketplace.
But after all we do not forget, it is the customer who decides if a microprocessor line is successful. More than 2000 design-wins illustrate that the SuperH™ is the right choice for a huge variety of applications. Hitachi is committed to further extend the product line to stay at the forefront of the business and technology of tomorrow.

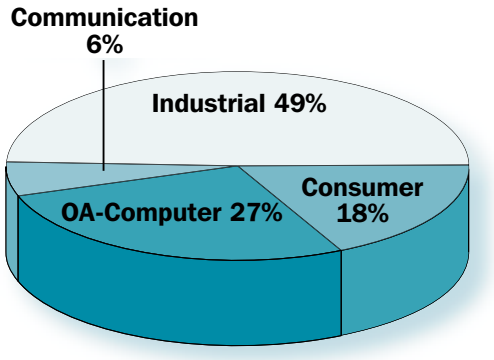


Figure 6: SuperH™ Design Win Overview by Product Classification

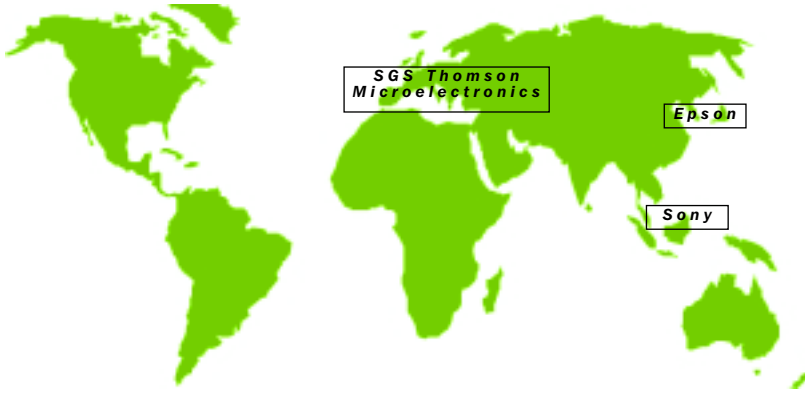


Figure 7: Strategic Alliances for SuperH™

SuperH™ CPU **Architecture** Overview

All devices in all families in the SuperH™ series employ a common 32-bit RISC (Reduced Instruction Set Computer) architecture, designed specifically by Hitachi to meet the needs of next-generation applications. This architecture is implemented in the SH-1 series. The SH-2, SH-3, and SH-4 feature upwardly compatible extensions.

Typically, RISC architectures feature:

- Load/Store approach
- Register orientation
- Simple instruction set
- Uniform instruction issuing
- Instruction pipelining

These basic features have been extended by Hitachi to meet the requirements of modern embedded applications. For example, Hitachi introduced in the SH architecture a fixed 16-bit instruction length offering a very high code density and thus saving memory and instruction fetch bandwidth.

Basic SH Features

The SH architecture has the following basic features:

- Load/Store architecture
- 32-bit internal data path
- General Purpose 32-bit Register bank
- 32-bit Control Registers
- 32-bit System Registers
- RISC-type instruction set
- 16-bit fixed-length instruction set
- 4 Gbyte address space
- Basic 5-stage RISC instruction pipeline

The address space is uniform and unsegmented. The instruction set has been carefully chosen to provide a high-level language orientation, thus simplifying programming of the individual devices. All basic SH CPU cores feature the integration of power saving strategies and implement methods to control the power consumption of peripherals.

Register Configuration

In case of the SH architecture, arithmetic and logical instructions operate normally on the 32-bit general purpose registers. Special load/store instructions are provided to transfer data from memory to registers and vice versa. Figure 8 below shows the basic General Purpose 32-bit register bank which is used for source and destination operands. The SH-3, SH3-DSP and the SH-4 architecture feature in addition to the basic 16 registers, 8 32-bit shadow registers which can be accessed in the so-called privileged mode. Besides the general purpose registers, the SH architecture provides 4 System Registers providing a Program Counter (PC), Procedure Register (PR), and 2 32-bit Multiply and Accumulate Registers (MACH/MACL). A block of Control Registers finally completes the set of registers in the basic SH architecture. The Control Register Block contains the Status Register (SR), the Global Base Register (GBR), the Vector Base Register (VBR) , and in case of SH-3, SH3-DSP and SH-4 the Saved Status Register (SSR), and the Saved Program Counter (SPC) .

The General Purpose Register R0 functions as index register for indirect indexed addressing modes (see below). In the case of SH-1, SH-2, and SH-DSP the register R15 is also used as a hardware stack pointer (SP). Register operands are always 32-bit longwords. When the memory operand is only a byte or a 16-bit word, it is sign-extended into a longword when loaded into a register.

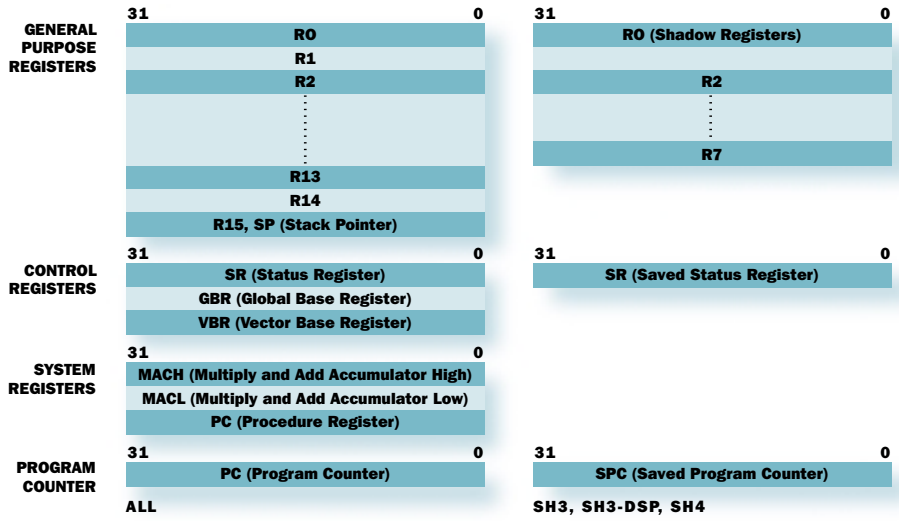


Figure 8: SH Architecture General Purpose Register Bank, Control Registers, and System Registers

Instruction Set

One main strength of the SH processor family is the instruction set upward compatibility of the various CPU cores. Figure 9 gives an overview of the instruction set compatibility. The basic SH instructions are all 16 bits long and thus tentatively offer a twice as efficient code density compared to conventional 32-bit RISC architectures.

The advantage of the used RISC approach can be seen by pipeline mechanism allowing very high clock frequencies.
The SH's pipelining mechanism provides a single cycle peak throughput for the basic instructions (2 in case of the superscalar SH-4). For that purpose, the SH architecture is using a basic 5-stage pipeline, see Figure 10. The pipeline is automatically reduced if an instruction does not need all stages, and extended if an instruction needs some more latency cycles to be completed or if pipeline contention occurs. To reduce pipeline penalties, a delay-slot mechanism has been provided, reducing pipeline-breakages.
The instruction set can be classified into the following operation categories:

- Data transfer
- Arithmetic
- Logical
- Shift
- Branch
- System control
- Extended such as Floating Point or DSP operations (not for SH-1, SH-2, and SH-3)

The data transfer instructions can be used with following addressing modes:

- Direct register addressing
- Indirect register addressing
- Postincrement indirect register addressing
- Predecrement indirect register addressing
- Indirect register addressing with displacement
- Indirect indexed register addressing
- Indirect GBR addressing with displacement
- Indirect indexed GBR addressing
- Indirect PC addressing with displacement
- PC relative addressing
- Immediate addressing

Figure 11 illustrates an example of the various addressing modes. This set of addressing modes allows an efficient code generation of modern compilers.

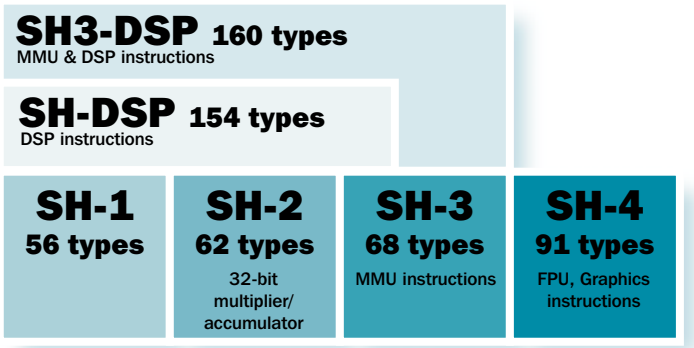


Figure 9: Instruction Set Upward Compatibility

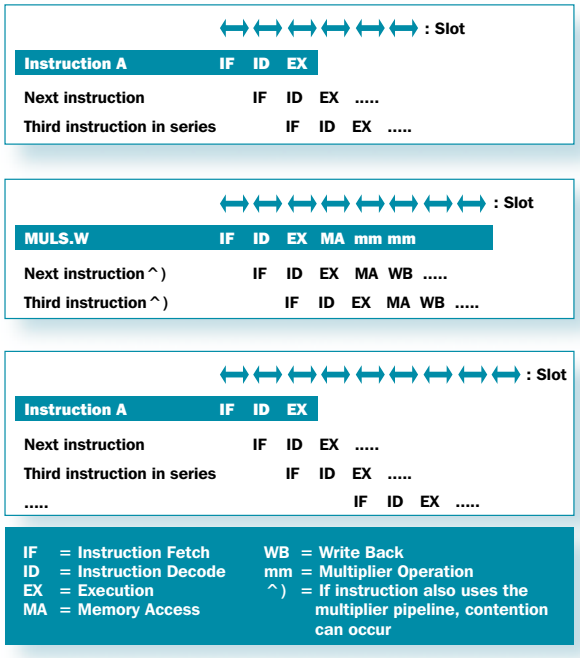
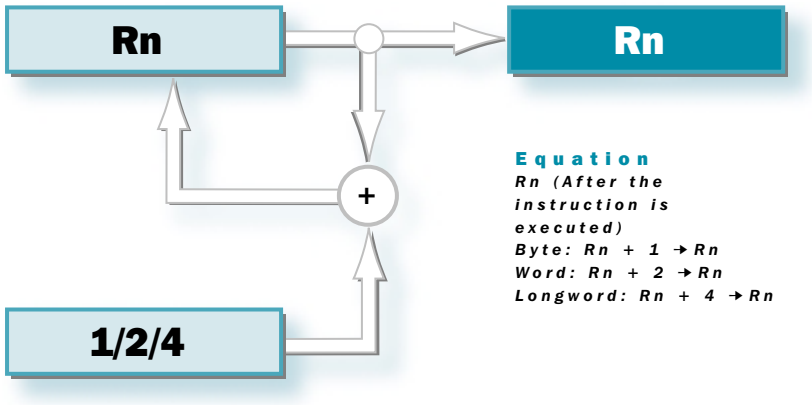


Figure 10: Instruction Pipelining, Examples

Description

The effective address is the content of register Rn. A constant is added to the content of Rn after the instruction is executed. 1 is added for a byte operation, 2 for a word operation, and 4 for a longword operation



Equation

Rn (After the instruction is executed)
Byte: Rn + 1 → Rn
Word: Rn + 2 → Rn
Longword: Rn + 4 → Rn

Figure 11: Postincrement indirect register addressing mode

Applicable Instructions

Class	Operation Code	Function	SH -1	SH -2	SH -3	#Instructions /#Types
Data transfer	MOV, MOVA, MOVT. SWAP, XTRCT	Data transfer	✓	✓	✓	SH-1: 39/5 SH-2: 39/5 SH-3: 40/6
Arithmetic operations	ADD, ADDC, ADDV, CMP/cond, DIV1, DIVOS, DIVOU, EXTS, EXTU, MAC, MULU, MULS, NEG, NEGC, SUB, SUBC, SUBV	Add, Subtract, Multiply, Divide (initialize and step), Multiply-And-Accumulate, Negate, Extract	✓	✓	✓	SH-1: 26/17 SH-2: 33/21 SH-3: 34/21
	MUL, DMULS, DMULU. DT	Double-Length Multiply, Decrement-and-Test		✓	✓	
Logic operations	AND, NOT, OR, TAS, TST, XOR	Bitwise logic operations, Memory Test-And-Set, Bit Test	✓	✓	✓	14/6
Shift	ROTL, ROTR, ROTCL, ROTCR, SHAL, SHAR. SHLL, SHLLn, SHLR, SHLRn	Rotate, Shitt-one-bit (arithmetic/logical), Shift-n-bits (logical, n=1,2,8, or 16)	✓	✓	✓	SH-1: 14/10 SH-2: 14/10 SH-3: 16/12
	SHAD, SHLD	Shift-n-bits dynamic (arithmetic/logical, -325≤ n≤ 31)			✓	
Branch	BF, BT, BRA. BSR, JMP, JSR, RTS	Conditional branch unconditional branch/calljump/return with delayslot	✓	✓	✓	SH-1: 7/7 SH-2: 11,9 SH-3: 11/9
	BRAF, BSRF, BF/S. BT/S	Far branch/call, conditional branch with delayslot		✓	✓	
System control	CLRT, CLRMAC, LDC, LDS, NOP, RTE, SETT. SLEEP, STC, STS. TRAPA	Clear T-bit	✓	✓	✓	SH-1: 31,11 SH-2: 31,11 SH-3: 74/14
	LDTLB, PREF, SETS. CLRS				✓	
Total						SH-1: 133/56 SH-2: 142/62 SH-3: 189/66

Table 1: SH Instruction set overview

Instruction Fetch

Besides optimising the costs for storage media, the fixed 16-bit instruction length also solves the bottleneck problem of conventional 32-bit RISC architectures. On a 32-bit memory access, 2 instructions can be loaded in parallel reducing the necessary memory accesses by a factor of 2.

MUL/MAC Operation

The SH architecture and thus all SH devices include a hardware multiplier providing a very high arithmetic performance. The multiply instruction (MUL) operates on register contents and stores the data in the dedicated system registers MACL/MACH. The multiply-accumulate instruction (MAC) directly operates on memory locations. The result is stored as before in the system registers. This is especially useful as the MAC instruction operates normally on a big linear set of data. General Purpose registers are used for storing the current memory addresses, which are automatically updated upon completion of a MAC instruction.

Immediate Data

The SH architecture provides a very efficient mechanism to process immediate data values. Byte immediate data are directly located in the 16-bit instruction code. Word or longword immediate data are stored in a memory table, which can be accessed by an immediate data transfer instruction. When the immediate data is loaded, the value is transferred to the register bank.

Data Format

Memory data formats are classified into bytes, words, and longwords. The SH architecture is basically a big-endian machine, but SH-3, SH3-DSP and SH-4 devices also support little-endian mode, see Figure 12. Figure 13 illustrates the data format of registers. When the memory operand is only a byte or a 16-bit word, it is sign-extended into a longword when loaded into a register

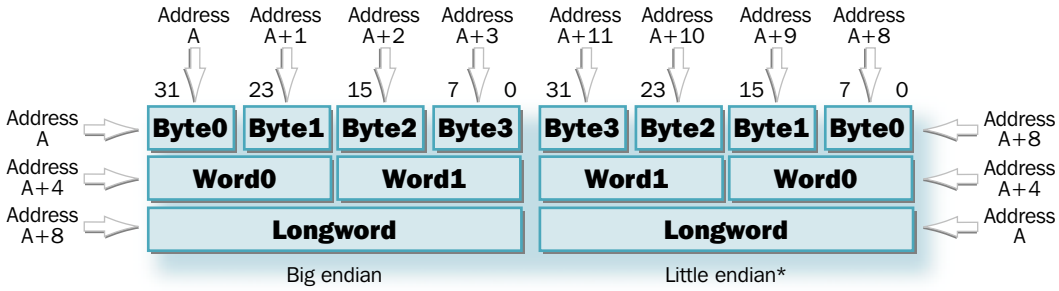


Figure 12: Memory data formats, Byte, Word, and Longword Alignment

**only SH-3, SH-3-DSP, SH-4*

Figure 13: Longword Register Operand

Processor States and Modes

The SH architecture provides a set of processor states:

- Reset state
- Exception handling state, transient state during which the CPU's processor state flow is altered by a reset, general or interrupt exception
- Program execution state
- Power-down state, CPU halts operation and power consumption is reduced
- Bus-released state, the CPU has released the bus to a device that requested it

All SH devices have built-in power-down modes:

- Sleep, on-chip peripherals still run
- Standby, on-chip peripherals halt
- Module stand-by (only SH-3, SH3-DSP, SH-4), specified modules halt

The SH-3, SH3-DSP, and SH-4 architecture incorporate 2 processor modes: user mode and privileged mode. Normal program execution is done in user mode, privileged mode is normally entered when an exception occurs. Also the shadow registers, see Figure 8, are then accessible.

Exception Processing

The SH family provides a single, uniform mechanism for handling all exceptions, wether caused by hardware or software conditions. Exception handling is resolved around a single table, the Excpetion Vector Table. The Vector Base Register (VBR) points to the beginning of that table. Exception conditions are prioritized by dedicated hardware. An Exception Handler, which is a kind of hardware-dispatched subroutine call, automatically stores and restores registers. The details of the exception processing depends on the individual architecture implementation and by the implemented Interrupt Controller (INTC), for further details see below.

Peripherals

All SH processors feature around the basic CPU core a set of peripherals. Details of the individual SH families and series are listed below.
Nevertheless, all SH devices feature a set of common peripherals, such as:

- Interrupt Controller (INTC)
- Watchdog Timer (WDT)
- Serial Communication Interface (SCI)
- Bus State Controller (BSC)
- User Break Controller (UBC)

The implementation may differ between individual devices. In addition to these peripherals, various devices in the series provide for example:

- DMA Controller (DMAC)
- Parralel I/O Ports
- Real-Time Clock RTC)
- A/D Converter (ADC)

And a lot more other peripherals.

DSP Extensions

In more and more embedded control applications it is necessary to include so-called Digital Signal Processing (DSP) capabilities. In traditional approaches this has been solved by adding to the microcontroller-system a dedicated DSP processor which differs a lot from traditional microcontrollers and microprocessors. The architecture of DSP processors is normally memory-oriented, includes special addressing modes and the DSP processors' instruction set is focusing on the processing of DSP algorithms such as Finite or Infinite Impulse Response Filters (FIR/IIR), or the Fast Fourier Transform (FFT). Based on such basic algorithms, DSP processors are , for example, especially useful for modem algorithms, and audio or image processing software.

The classical approach, using a microcontroller and a dedicated DSP processor leads to complex systems, with very often 2 operating systems, and several heterogeneous bus systems which often make system design and debugging very difficult. Within the SuperH™ family a new and innovative approach has been designed offering an integrated, combined CPU/DSP architecture approach. Based on the SH-2 CPU core, Hitachi added dedicated DSP capabilities resulting in the SH-DSP core concept. The same is being done with the SH-3 core, resulting in the advanced SH3-DSP CPU core.

Users now have 2 cores integrated in a single architecture with a single instruction stream. This simplifies system design and offers an overall cost reduction. This approach makes the utilisation of additional and expensive accelerator hardware superfluous in most cases.

Figure 14 illustrates the advances of the integrated CPU/DSP approach over traditional approaches.

In the SH-DSP and SH3-DSP architecture, Hitachi added mainly:

- an additional X-Y-on-chip bus structure
- loop hardware
- fixed-point arithmetic support
- DSP-oriented addressing modes
- an DSP-oriented instruction set extension.

The SH-DSP architecture offers object-code upward compatibility from the SH-1 and SH-2 architecture, the SH3-DSP from the SH-1, SH-2, SH-DSP and SH-3 architecture providing an easy upgrade path for future products.

DSP vs. MAC Functionality

For several applications it is sufficient to use the SH's integrated MAC functionality and accelerator, respectively. As this MAC has been optimised for memory accesses, it is especially useful for running filter algorithms. This already offers enough performance for several DSP algorithms. With the SH-DSP and SH3-DSP, the SH family will offer alternatives to run DSP algorithms if a higher performance is required.

Figure 14: Conventional vs. Integrated CPU/DSP System Solution Approach

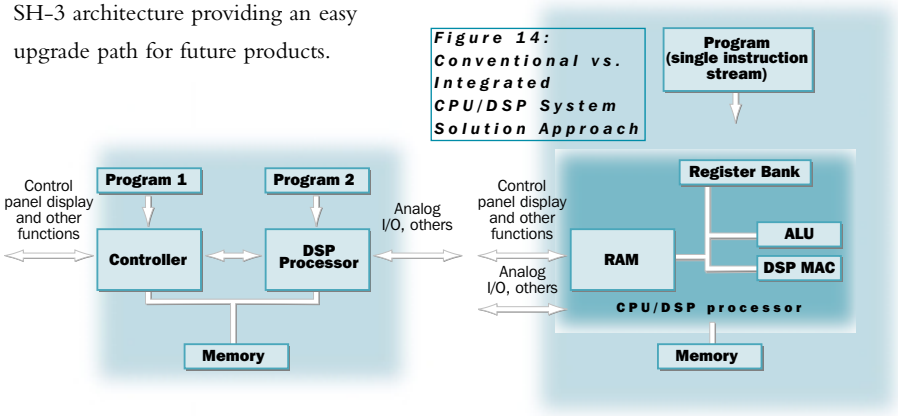
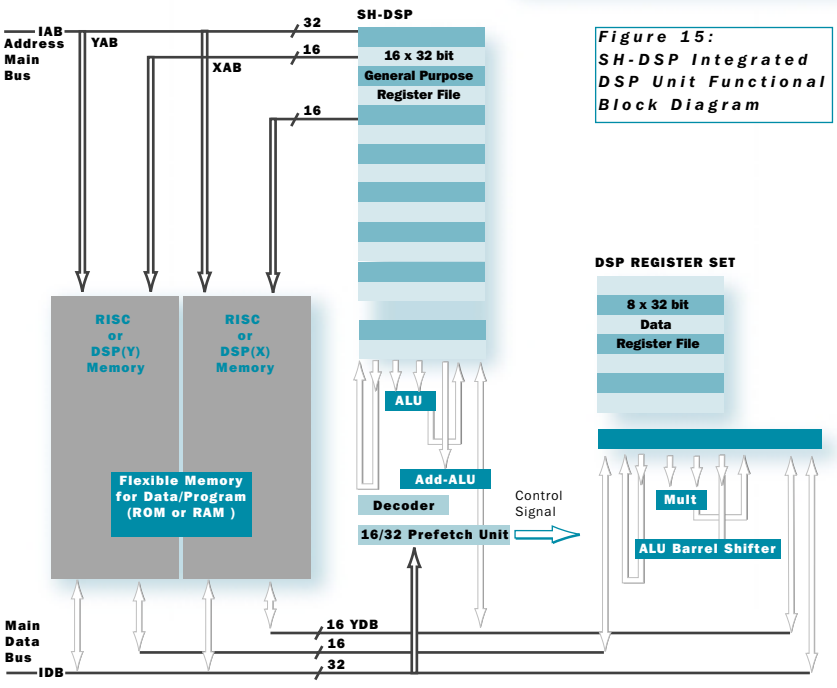


Figure 15: SH-DSP Integrated DSP Unit Functional Block Diagram



SH-1: Low-cost, **Highly Integrated 32-bit Embedded** Controllers

The SH-1 series forms the basis of the SuperH™ embedded controller family. The members of this family have been optimised for low cost and high integration while offering the performance of a 32-bit controller. The SH-1 series integrates on-chip RAM and ROM. All SH-1 implementations incorporate a 16-bit hardware multiplier, which produces a 32-bit result. What is more, all SH-1 devices implement a 42-bit accumulator for 16-bit data giving you the performance needed in most of the 32-bit applications of today.

SH-1 Architecture:

- 32-bit internal data path
- 16-bit fixed-length RISC-type instruction set
- Load/Store architecture
- 5-stage pipeline
- 4 Gbyte address space
- 16 x 32-bit general registers
- 3 x 32-bit control registers
- 4 x 32-bit system registers
- Basic instructions are executed in 1 cycle
- Multiplication operations (16x16(32) executed in 1-3 cycles, multiplication /accumulation operation (16x16+42(42) executed in 2-3 cycles, 42-bit accumulator
- Processing states: program execution, exception processing, bus release, reset, sleep mode, standby

Common SH-1 Peripherals:

- Interrupt Controller (INTC) for 8+1 external and a set of internal interrupt sources, up to 16 priority levels can be programmed
- User Break Controller (UBC) simplifying debugging of user programs
- Clock Pulse Generator (CPG) supplying the LSI and external devices with clock pulses from a connected crystal resonator or an external clock
- 16-bit Integrated-Timer Pulse Unit (ITU) with 5 channels, up to 12 different pulse outputs and 10 different pulse inputs can be processed, compare match waveform, input capture, counter clearing, PWM mode, phase counting, DMAC activation
- Watchdog Timer (WDT) for monitoring system operations
- Programmable Timing Pattern Controller (TPC), maximum output of 16-bit data, output can be enabled on a bit-by-bit basis
- Serial Communication Interface (SCI), 2 channels, supports clocked synchronous and asynchronous mode, selectable bit rates via on-chip baud generator, full duplex communication
- 4 Channel DMA Controller (DMAC)
- Parallel I/O Ports, 2 16-bit input/output ports, each port has a register for storing pin data
- Bus State Controller (BSC), for details see below
- Pin Function Controller (PFC) is composed of registers for selecting the function of multiplexed pins
- Single cycle access on-chip ROM and RAM (32-bit)

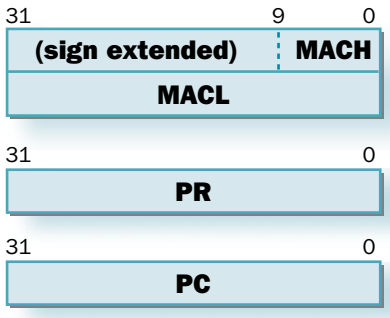


Figure 16: SH-1 System registers

Multiply and accumulate (MAC) registers high and low (MACH, MACL): Store the results of multiply and accumulate operations. MACH is sign-extended when read because only the lowest 10 bits are valid.

Procedure register (PR): Stores a return address from a subroutine procedure.

Program counter (PC): Indicates the fourth byte (second instruction) after the current instruction.

Bus State Controller (BSC)

The BSC divides the address space into 8 areas. A maximum of 4 Mbyte of linear address space for each area can be addressed (area 1 up to 16 Mbyte when set to DRAM).
The BSC supports the following features:

- 8-/16-bit external data bus
- On-chip ROM and RAM can be accessed in 1 cycle (32-bit)
- Wait states can be inserted using the WAIT pin
- Direct interface to DRAM, SRAM, and ROM
- Control signals
- Access control
- Supports parity check and generation for data bus
- Refresh counter can be used as 8-bit interval timer

SH7020 Series

The SH7020 series includes 1 Kbyte of RAM and is available with 16 and 32 Kbyte of ROM, also a ROMless version is available.
The SH7020 series includes all the above mentioned peripherals.

SH7030 Series

The SH7030 series is available with 4 and 8 Kbyte of RAM. It either has 64 Kbyte of ROM or comes as ROM-less version. In addition to the above introduced peripherals, the SH7030 series features :

- A/D Converter, 10 bits x 8 channels
- 8-bit input port, additional register for storing pin data

Individual SH7020/7030 devices are available in extended temperature range qualification.

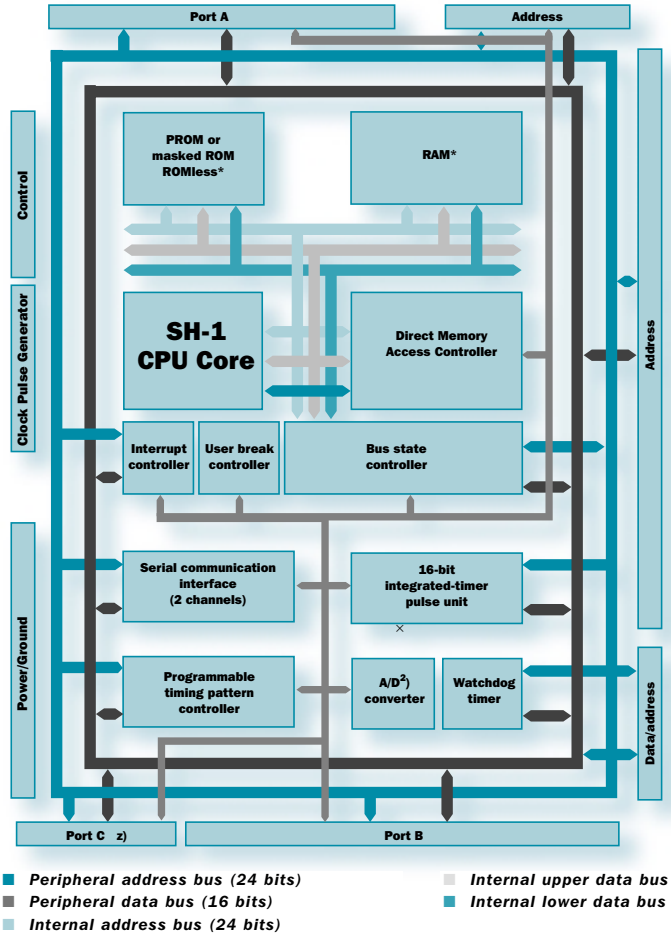


Figure 17: Functional Block Diagram of the SH7020/SH7030 series
1) see selection guide for details
2) only SH7030 series

Table 2: SH-1 Series Microcontroller Overview
1)Part names differ for 5V and 3.3V devices, for different package types, and for different temperature ranges
2)Temperature range: -20 to +75 °C
3)Temperature below 50 °C

Product Name	Part name 1)	ROM (kByte)	ROM type	RAM (kByte)	Frequency (MHz=MIPS)		Typ. Power (mW) 2)	Typ. Sleep Current (mA) 2)	Typ. Standby Current (uA) 3)	Package
					5V	3.3V		3.3V		
SH7020	HD6417020xx	-	-	1	20	12.5	215	30	0.01	100 TQFP
	HD6437020Sxx	16	Mask ROM							
SH7021	HD6477021xx	32	OTP							
	HD6437021Sxx	32	Mask ROM							
SH7032	HD6417032xx	-	-	8			198	40	0.01	112 QFP/
SH7034	HD6417034xx	-	-	4						120 TQFP
	HD6477034xx	64	OTP							
	HD6437034Axx	64	Mask ROM							

SH Family Devices

SH-1 Family Devices

Device	SH7020	SH7020S ROMless	SH7021	SH7032 ROMless	SH7034
Core	SH-1	SH-1	SH-1	SH-1	SH-1
Vcc (V) / Max. Clock (MHz)	5 / 20 3.3 / 12.5	5 / 20 3.3 / 12.5	5 / 20 3.3 / 12.5	5 / 20 3.3 / 12.5	5 / 20 3.3 / 12.5
External Bus Width	16	16	16	16	16
On-chip ROM (kByte)	16		32		64
Mask ROM Version	yes		yes		yes
ZTAT (OTP) Version			yes		yes
On-chip RAM (kByte)	1	1	1	8	4
Interrupts (Internal/External)	13 / 9	13 / 9	13 / 9	13 / 9	13 / 9
DMA Controller (channels)	4	4	4	4	4
Watch Dog Timer (channel)	1	1	1	1	1
Serial Communication Interface	2	2	2	2	2
I/O Ports (including input-only)	40	40	40	40	40
Timing Pattern Controller	yes	yes	yes	yes	yes
Integrated Timer Unit	yes	yes	yes	yes	yes
Bus State Controller	yes	yes	yes	yes	yes
User Break Controller	yes	yes	yes	yes	yes
Clock Pulse Generator	yes	yes	yes	yes	yes
A/D Converter (bits x channels)				10 x 8	10 x 8
Data Book	19-015A	19-015A	19-015A	19-011B	19-011B
Package	TQFP-100	TQFP-100	TQFP-100	QFP-112	QFP-112 TQFP-120
Part Name	HD6437020xxx	HD6417020xxx	HD64x7021xxx	HD6417032xxx	HD64x7034xxx

SH-2 Family Devices

Device	SH7014 ROMless [1]	SH7016[1]	SH7017F[1]	SH7011[1]	SH7040A	SH7041A	SH7042A	SH7043A
Core	SH-2	SH-2	SH-2	SH-2	SH-2	SH-2	SH-2	SH-2
ock (MHz)	5 / 28.7	5 / 28.7	5 / 28.7 16	3.3 / 20	5 / 33 3.3 / 16	5 / 33 3.3 / 16	5 / 33 3.3 / 16	5 / 33 3.3 / 16
Bus Width	16	16	128	16	16	32	16	32
M (kByte)		64		ROMless	64	64	128	128
M Version		yes			yes	yes	yes	yes
P) Version							yes	yes
) Version			yes					
M (kByte)								
e is used)	3 (1)	3(1)	4(2)	4	4 (2)	4 (2)	4 (2)	4 (2)
e (kByte)	1	1	2		1	1	1	1
/External)	43 / 7	43 / 7	43 / 7	43 / 7	44 / 9	44 / 9	44 / 9	44 / 9
channels)	2	2	2	2	4	4	4	4
(channel)	1	1	1	1	1	1	1	1
Interface	2	2	2	1	2	2	2	2
nput-only)	43	82	82	11	82	106	82	106
mer/Pulse	3	3	3	3	5	5	5	5
channels)								
re Match	2	2	2	2	2	2	2	2
channels)								
Controller								
imer Unit								
Controller	yes	yes	yes	yes	yes	yes	yes	yes
Controller					yes	yes	yes	yes
Generator	yes	yes	yes	yes	yes	yes	yes	yes
channels)	10 x 8	10 x 8	10 x 8	10 x 7	10 x 8	10 x 8	10 x 8	10 x 8
ata Book					19-033A	19-033A	19-033A	19-033A
Package	QFP-112	QFP-112	QFP-112	QFP-100	QFP-112	QFP-144	QFP-112	QFP-144
art Name	HD6417014RFxx	HD6437016Fxx	HD64F7017Fxx	HD6417011Fxx	HD6437040Axx	HD6437041Axx	HD64x7042Axx	HD64x7043AFxx

1) Contact your local sales office for availability

SH-3 Family Devices

Device	SH7044A	SH7045A	SH7044F	SH7045F
Core	SH-2	SH-2	SH-2	SH-2
Vcc (V) / Max. Clock (MHz)	5 / 33 3.3 / 16	5 / 33 3.3 / 16	5 / 28	5 / 28
External Bus Width	16	32	16	32
On-chip RAM (kByte)	256	256	256	256
Cache (kByte) (if RAM mode is used)	yes	yes		
Memory Management Unit				
Interrupt Controller			yes	yes
External Interrupt Pins				
DMAC (channels)	4 (2)	4 (2)	4 (2)	4 (2)
Watch Dog Timer (channel)	1	1	1	1
Serial Communication Interface	44 / 9	44 / 9	44 / 9	44 / 9
IrDA 1.0 Support	4	4	4	4
Smart Card Support	1	1	1	1
PCMCIA Interface Support	2	2	2	2
I/O Ports (including input-only)	82	106	82	106
32-bit Timer (channels)	5	5	5	5
Real Time Clock				
Bus State Controller	2	2	2	2
SDRAM Interface				
User Break Controller				
Clock Pulse Generator				
A/D Converter (bits x channels)	yes	yes	yes	yes
D/A Converter (bits x channels)	yes	yes	yes	yes
Litte-endian Support	yes	yes	yes	yes
Big-endian Support	yes	yes	yes	yes
Data Book 19-029C 19-036	10 x 8	10 x 8	10 x 8	10 x 8
Package LQFP-144 QFP-208	19-033A	19-033A	19-033A	19-033A
Part Name	QFP-112	QFP-144	QFP-112	QFP-144
	HD64x7044Afxx	HD64x7045Axx	HD64F7044Fxx	HD64F7045Fxx

Device	SH7709
Core	SH-3
Vcc (V) / Max. Clock (MHz)	3.3 / 80
External Bus Width	32
On-chip RAM (kByte)	(4)
Cache (kByte) (if RAM mode is used)	8 (4)
Memory Management Unit	yes
Interrupt Controller	yes
External Interrupt Pins	7
DMAC (channels)	4
Watch Dog Timer (channel)	1
Serial Communication Interface	3
IrDA 1.0 Support	yes
Smart Card Support	yes
PCMCIA Interface Support	yes
I/O Ports (including input-only)	12 x 8-bit
32-bit Timer (channels)	3
Real Time Clock	yes
Bus State Controller	yes
SDRAM Interface	yes
User Break Controller	yes
Clock Pulse Generator	yes
A/D Converter (bits x channels)	10 x 8
D/A Converter (bits x channels)	8 x 2
Litte-endian Support	yes
Big-endian Support	yes
Data Book 19-029C 19-036	19-036
Package LQFP-144 QFP-208	QFP-208
Part Name	HD6417709F80B

Development Tools

The development of applications based on the SH-1 family is supported by evaluation boards and emulators. Hitachi provides the EVB7032 evaluation board featuring a SH7032 device and PCE low-cost in-circuit emulators. The PCE Emulators feature

- Zero wait-state, real-time emulation
- Emulation memory
- PC breakpoints
- Hardware comparison breakpoints
- Trace buffer
- Oscilloscope trigger facility
- Multiple clock selection
- Performance analysis

The development support comprises of a C compiler and debugger. A wide variety of third-party tools are also available for the SH-1 series.

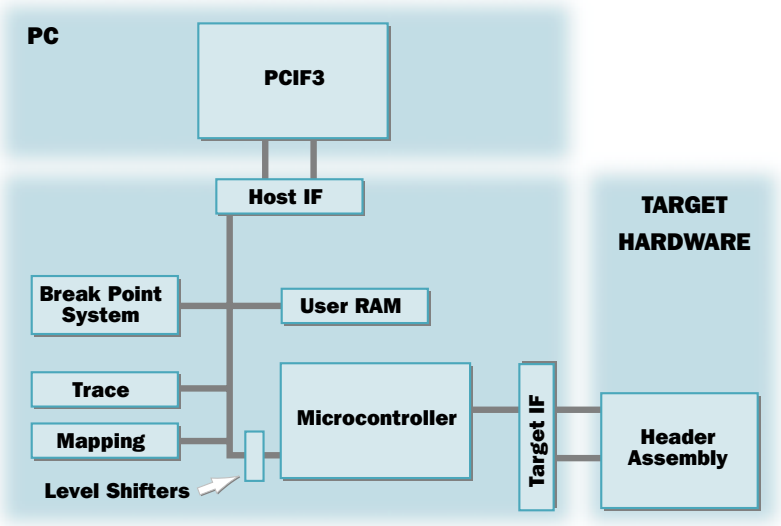


Figure 18: PCE Emulator Block Diagram

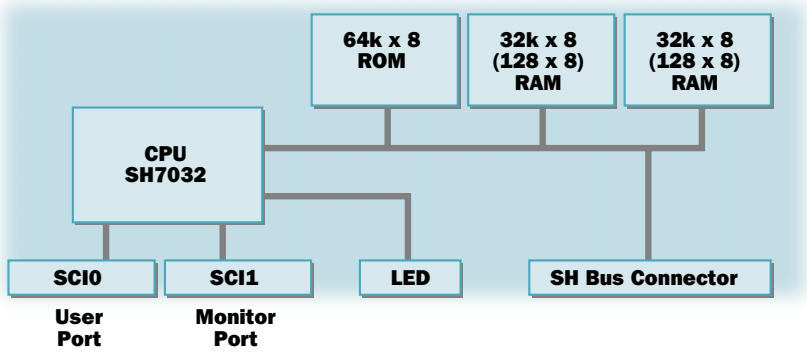


Figure 19: EVB7032 Block Diagram

Application Examples

The SH-1 series focuses on embedded control applications such as printers, fax machines, motor control, cameras, musical instruments, household appliances, card reader, phones, radio equipment, inverter, security systems, robotics.

Related Documents
SH7020, SH7021 Hardware Manual (Document No. 19-015A
SH7032, SH7034 Hardware Manual (Document No. 19-011B
SH-1/SH-2 Programming Manual (Document No. 19-005B
SH7000 Series CPU Application Note (Document No. 19-026

SH-2: Advanced **32-bit Embedded** Controllers

Based on the SH-2 architecture two basic types of device have been introduced, the SH7040 and the SH7050 series.

Both series offer a leading-edge price/performance ratio, integrated peripherals and the advantage of being object-code upward compatible from the SH-1 family. In addition, several peripherals are similar to program, thus, the SH-2 family provides a straight forward upgrade path from SH-1 solutions.

SH-2 Architecture

- 32-bit internal data path
- 16-bit fixed-length RISC-type instruction set
- Load/Store architecture
- 5-stage pipeline
- 4 Gbyte address space
- 16 x 32-bit general registers
- 3 x 32-bit control registers
- 4 x 32-bit system registers
- Basic instructions are executed in 1 cycle
- Multiplication operations (16x16(32, 32x32(32) and multiplication /accumulation operation (16x16+64(64, 32x32+64(64) executed in 1-4 cycles, 64-bit accumulator
- Processing states: program execution, exception processing, bus release, reset, sleep mode standby

Common SH-2 Peripherals

The SH7040 and SH7050 series have the following peripherals in common.

- Interrupt Controller (INTC) for 8+1 external and a set of internal interrupt sources, up to 16 priority levels can be programmed
- User Break Controller (UBC) simplifying debugging of user programs
- Clock Pulse Generator (CPG/PLL) supplying the LSI and external devices with clock pulses from a connected crystal resonator or an external clock, a PLL provides clock multiplication
- Watchdog Timer (WDT) for monitoring system operations
- 4 Channel DMA Controller (DMAC)
- Compare Match Timer (CMT) configured of 16-bit timers for 2 channels, includes 16-bit counters and can generate interrupts at set intervals
- I/O Ports, several I/O ports have been integrated into SH-2 devices.
- Bus State Controller (BSC).
- A/D Converters (ADC), for details see below
- Serial Communication Interface (SCI), at least 2 channels supporting clocked synchronous and asynchronous mode, selectable bit rates via on-chip baud generator, full duplex communication, multiprocessor communication function.
- Pin Function Controller (PFC) is composed of registers for selecting the function of multiplexed pins
- Single cycle access on-chip ROM and RAM (32-bit), amount of on-chip ROM and RAM varies, some devices (SH7040 series) can be configured to split the RAM into a RAM block and a cache memory block.

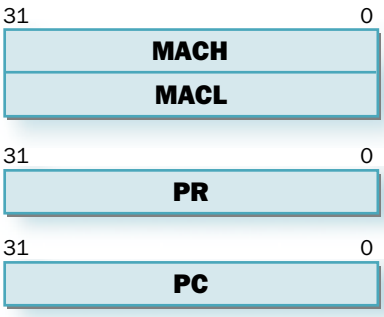


Figure 20: SH-2 System Registers

Multiply and accumulate (MAC) registers high and low (MACH, MACL): Stores the results of multiply and accumulate operations.

Procedure register (PR): Stores a return address from a subroutine procedure.

Program counter (PC): Indicates the fourth byte (second instruction) after the current instruction.

SH7040

The SH7040 series offer different versions with a variety of different A/D converters, different on-chip memory sizes and types. Throughout the SH7040 series you will find the following additional peripherals offering you system solution support and an overall cost reduction for a wide range of applications:

- Cache memory, 1 kbyte instruction cache and PC relative read data used in common with on-chip RAM (2 kbytes of on-chip RAM are used for address/data array when cache is enabled), direct map method, 256 entry cache tags, 4-byte lines, cache can be disabled for full use of on-chip RAM
- Bus State Controller (BSC), memory address space is divided into 5 areas, 1 area for on-chip ROM mode, 3 areas of up to 4 Mbytes linear address space, 1 area up to linear 16 Mbytes of DRAM dedicated space, DRAM controller, 8-/16-/32-bit external data bus size (32-bit only for 144-pin devices), number of wait cycles can be set, 1 cycle on-chip RAM and ROM access
- Multifunction Timer/Pulse Unit (MTU), up to 16 types of waveform outputs or up to 16 types of pulse I/O processing based on 16-bit timer, 5 channels, capture registers, 16 comparators, counter input clock, input capture, pulse output mode, PWM mode, phase calculation
- 2 Channel Serial Communication Interface (SCI)
- I/O Ports, 5 ports for general purpose I/Os (1x10 bits, 2x16 bits, 112-pin 2x16 bits, 144-pin 1x24 bits and 1x32 bits) and 1 port as general 8-bit input port

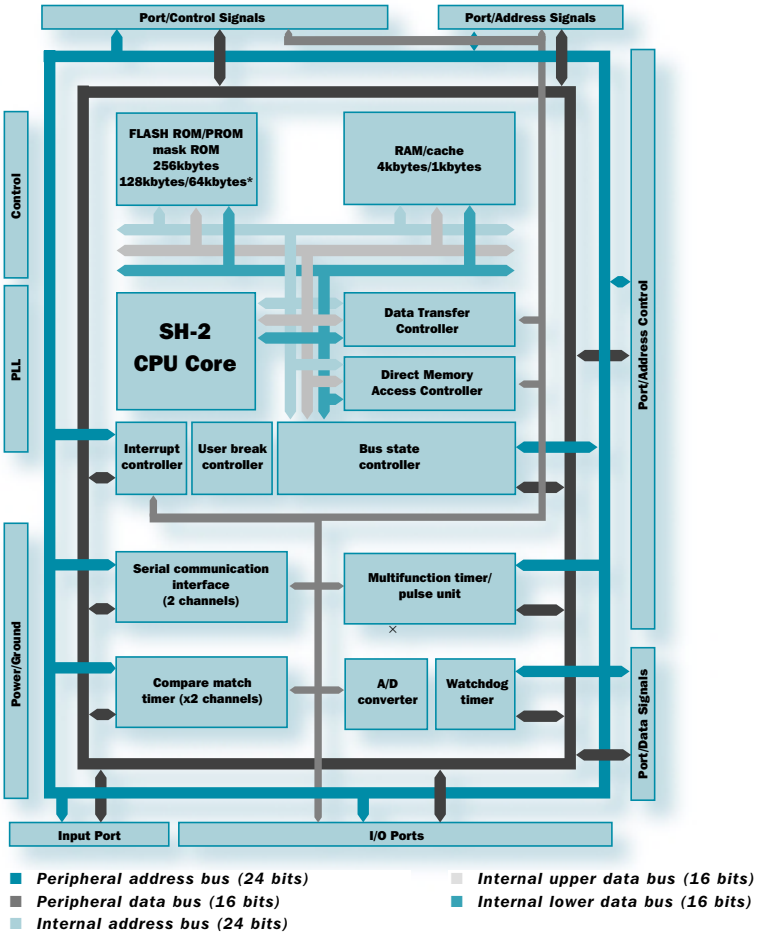


Figure 21: SH7040 Series Functional Block Diagram

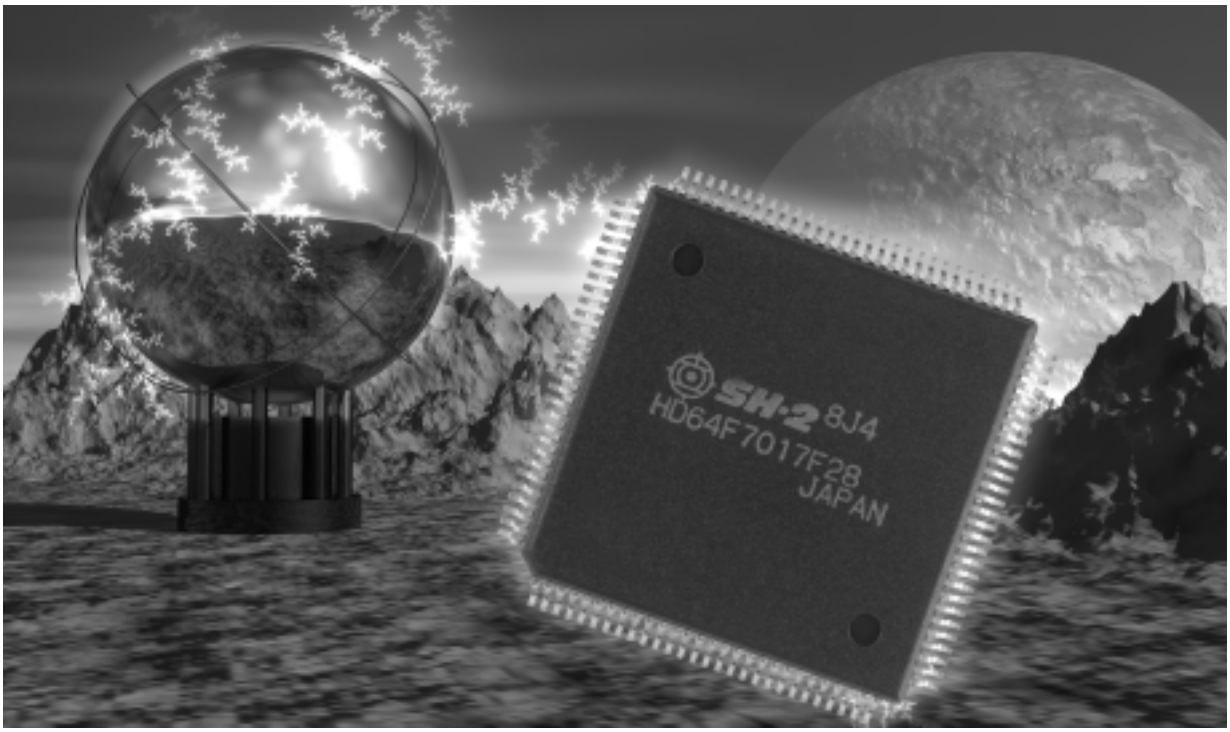
**See selection guide for details*

- Data Transfer Controller (DTC) performing data transfers, activation by interrupts or software, several transfer modes
- A/D Converter (ADC), 10 bits x 8 channels, sample and hold function with 2 on-chip units, multiple conversion modes, 8 data registers

SH7010 (SH-2 Compact Version)

Hitachi is introducing a set of SH7040 compact derivatives offering an application-oriented line-up named SH7010 series. This series features very cost effective ROMless devices (SH7011 and SH7014), the SH7016 derivative with 64 Kbyte on-chip mask ROM and 3 Kbyte RAM as well as a pin-compatible FLASH derivative. This SH7017F device with 128 Kbyte on-chip FLASH memory and 4 Kbyte RAM allows high intergrated solutions for different applications.
The SH7010 series offers a lot of integrated peripheral functions. These "Compact" versions are featuring the modifications compared to the SH7040 series illustrated in the subsequent tables:

SH7014	SH7016/7017F	SH7011
ROMless	64 KB ROM / 128 KB FLASH	ROMless
3 KB RAM	3 KB / 4 KB	4 KB RAM
1 KB Cache	1 KB / 2 KB Cache	-
43 I/O ports	82 I/O ports	11 I/O ports
3 channels MTU	3 channels MTU	3 channels MTU
-	-	8 bit Timer x 2
1ch. S&H ADC, 8ch	1ch. S&H ADC, 8ch	1ch. S&H ADC, 7ch
SCI 2 channels	SCI 2 channels	SCI 1 channel
no DTC	no DTC	no DTC
no UBC	no UBC	no UBC
28.7 MHz / 5v	28.7 MHz / 5v	20 MHz / 3.3v
QFP-112 pin	QFP-112 pin	TQFP-100 pin



Flash Memory

Several devices of the SH7040 and SH7050 series integrate 256 kbytes of Hitachi's flash memory F-ZTAT technology providing an increased flexibility for system design. The integrated flash memory features:

- **4 flash memory operating modes (program, erase, program-verify, erase-verify)**
- **32 bytes at a time programming with a typical programming time of 10 ms (300 µs typical per byte)**
- **On-board programming modes**
- **Automatic bit rate adjustment**
- **Flash memory real-time emulation by overlapping a part of RAM**
- **Protect modes**

SH7060 Series

Based on the SH-DSP CPU core, Hitachi is currently developing a new lineup of it's SH-2 embedded microcontrollers. Members of this series will feature a high clock frequency, integrated flash memory and other peripherals dedicated to specific markets. The SH7060 series will offer an upgrade path from the SH7040 series.

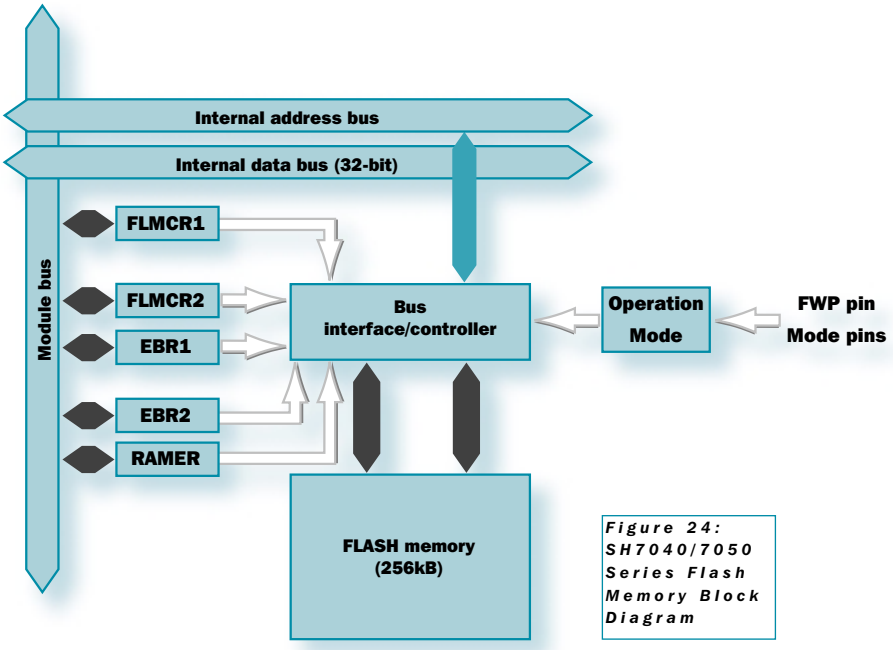


Figure 24: SH7040/7050 Series Flash Memory Block Diagram

FLMCR1: FLASH memory control register 1
FLMCR2: FLASH memory control register 2
EBR1: Block specification register 1
EBR2: Block specification register 2
RAMER: RAM emulation register

Table 3: SH-2 Series Microcontroller Overview
**1 Part names differ for 5V and 3.3V devices, for different package types, and for different temperature ranges*
**2 When cache is used*
**3 Typical, 3.3V. F=16.7 MHz, temperature range: -20 to +75°C*
**4 Typical, 5V. F=20 MHz, temperature range: -40 to +85°C*
**5 Preliminary data please contact your local Sales Office for availability*

Product Name	Part name*[1]	ROM (kByte)	ROM type	Cache (kByte)	RAM (kByte)	Frequency MHz		External Bus Width	Current Consumptive (mA)	Package
						5V	3.3V			
SH7011★[5]	HD6417011Fxx				4		20	16		TQFP100
SH7014★[5]	HD6417014Rxx			1	3/1★[2]	28.7				QFP 112
SH7016★[5]	HD6437016Fxx	64	MASK							
SH7017F★[5]	HD64F7017Fxx	128	FLASH	2	4/2★[2]					
SH7040A	HD6437042Axx	64	MASK	1		28/33	16		80★[3]	
SH7041A	HD6437041Axx							32		QFP 144
SH7042A	HD6437042Axx	128	MASK					16		QFP112
	HD6477042Axx		PROM							
SH7043A	HD6437043Axx		MASK					32		QFP144
	HD6477043Axx		PROM							
SH7044A	HD6437044Axx	256	MASK					16		QFP112
	HD6477044Axx		PROM							
SH7044AF	HD64F7044Axx		FLASH			28				
SH7045A	HD6437045Axx		MASK					32		QFP144
	HD6477045Axx		PROM							
SH7045AF	HD64F7045Axx		FLASH							

Development Tools

The development of applications based on the SH-2 family is supported by evaluation boards and emulators. Hitachi provides the EVB7045F featuring a SH7045F device and the E6000 in-circuit emulators. The E6000 emulators feature:

- Zero wait-state, real-time emulation
- Emulation memory
- 256 PC breakpoints
- Complex Event System (CES)
- Up to 12 hardware breakpoints using the event and range channels in the CES
- Trace buffer acquisition filtering using the CES
- Execution time measurement
- 4 user logic probes for triggering Events in the CES
- Automatic tracking of the target system power supply
- Multiple target clock selection

The development support comprises a C compiler and debugger. A wide variety of third-party tools and software are also available for the SH-2 series.

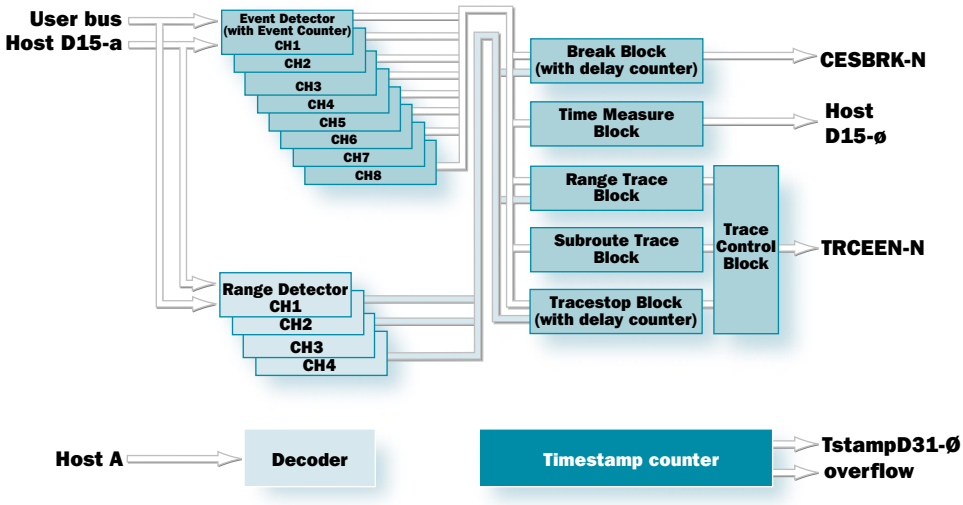


Figure 25: E6000 CES Block Diagram

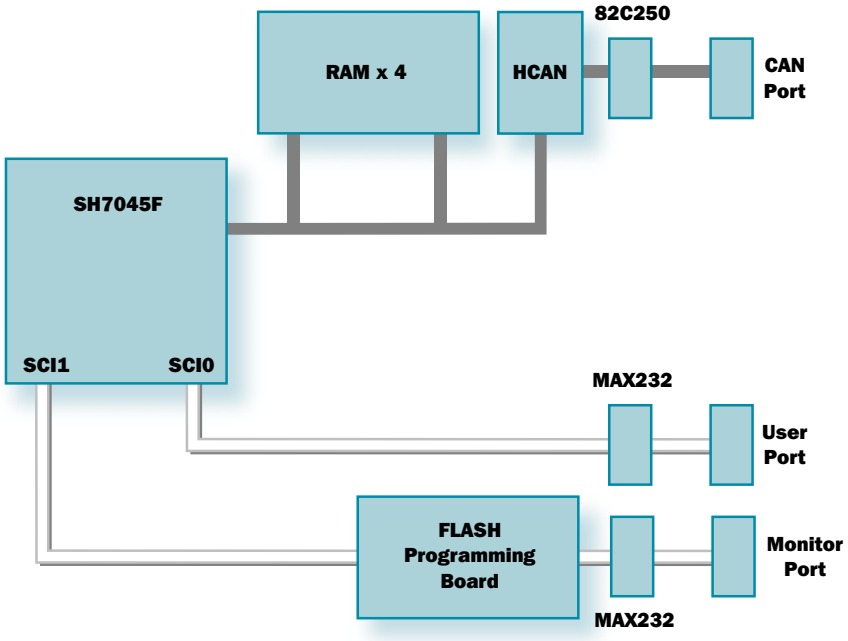


Figure 26: EVB7045F Block Diagram

Application Examples

The SH-2 family has been specifically designed for advanced 32-bit embedded control systems. Target applications of the SH-2 series are, for example, phones, radio equipment, motor control, robotics, control terminals, printers, scanners, music instruments, audio applications, cameras, plotters, and projectors.

Related Documents
SH7040 Series User's Manual (Document No. 19-033A
SH-1/SH-2 Programming Manual (Document No. 19-005B
SH7040 Series On-chip supporting modules (Document No.19-032

SH-3: High-performance, **Cost-effective 32-bit Embedded** Processors

The SH-3 architecture is a further development of the SH-1 and SH-2 architecture featuring Memory Management Unit (MMU) support and additional units for high-performance, cost-optimised embedded processor systems. In the centre of the SH-3 family is the SH7700 series with a focus on the SH7709 embedded processor. The SH7709 device is the first choice for Windows® CE powered systems. The dedicated companion chip HD64461 for the SH7709 makes optimised system design for Windows® CE applications possible. Hitachi is a system solutions provider for Windows® CE applications .

SH-3 Architecture

- 32-bit internal data path
- 16-bit fixed-length RISC-type instruction set
- Load/Store architecture
- 5-stage pipeline
- 4 Gbyte address space
- 16 x 32-bit general registers
- 8x32-bit shadow registers
- 5 x 32-bit control registers
- 4 x 32-bit system registers
- Basic instructions are executed in 1 cycle
- Multiplication operations (16x16(32, 32x32(32) and multiplication /accumulation operation (16x16+64(64, 32x32+64(64) executed in 1-5 cycles, 64-bit accumulator
- Processing states: program execution, exception processing, bus release, reset, sleep mode standby

SH7709 Embedded Processor

The SH7709 32-bit embedded processor is based on the SH-3 CPU core and provides a set of peripherals making system design cost-effective. The SH7709 features 8 kByte of Cache, a Windows® CE compliant Memory Management Unit (MMU), a Bus State Controller (BSC) featuring also SDRAM support and an optimised mix of further peripherals simplifying system design and reducing overall system costs.

The SH7709 is available with 80 MHz internal clock frequency and provides a set of power down mechanisms and modes especially useful for battery-powered handheld systems. At full speed the SH7709 has a typical power consumption of 100 mA at 3.3V.
The SH7709 interfaces glueless to the HD64461 companion chip which includes a set of further interfaces and a colour LCD graphics controller.
The SH7709 can be used with and without the HD64461 device.

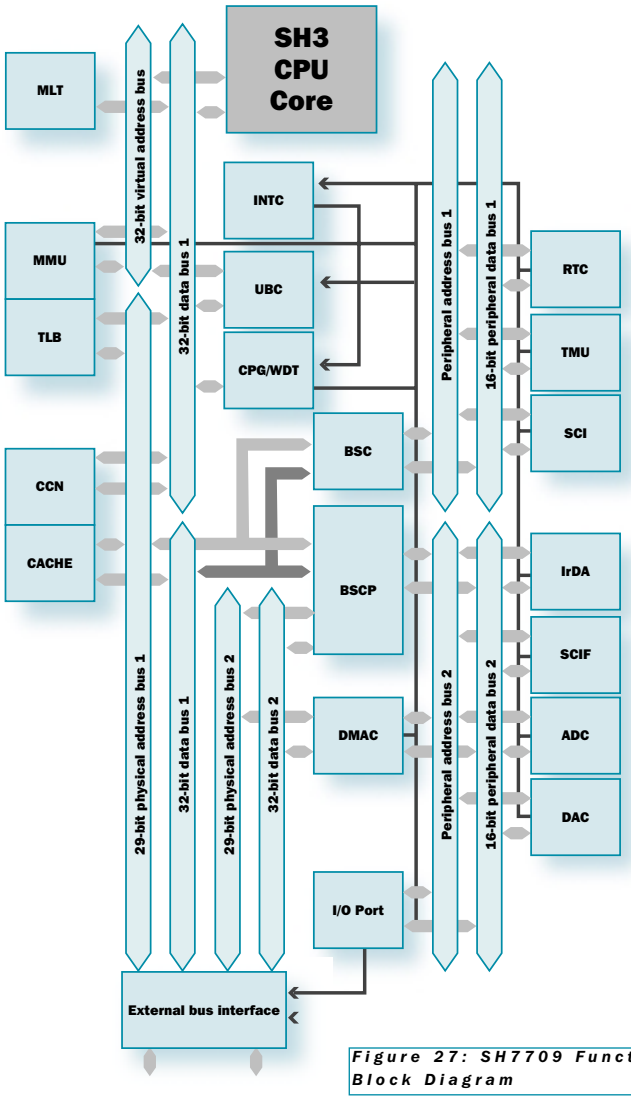


Figure 27: SH7709 Functional Block Diagram

SH7709 Peripherals

The peripheral mix of the SH7709 includes out of the following modules:

- 8 kByte of mixed instruction/data cache memory, 128-entry. 4-way associative TLB, cache can be divided into 4 kByte/2-way cache plus 4 kByte RAM
- Memory Management Unit (MMU) supporting 4 Gbytes of address space, 256 address spaces, page unit sharing
- Interrupt Controller (INTC) with 7 external interrupt pins
- 3 x Serial Communication Interfaces (SCI), 2 with 16 byte FIFO for transmit/receive, including IrDA 1.0 interface, smart crad interface support
- User Break Controller (UBC) simplifying debugging of user programs
- Clock Pulse Generator (CPG/PLL) supplying the LSI and external devices with clock pulses from a connected crystal resonator or an external clock, a PLL provides clock multiplication
- Real-Time Clock (RTC) with calendar and alarm functions, on-chip 32-kHz crystal oscillator
- 3 channel autoreload 32-bit timer with input capture function, maximum resolution of 2 MHz
- 4 channel DMA Controller (DMAC), burst mode and cycle steel mode
- I/O ports up to 16 bits
- A/D Converter (ADC), 8 channels, 10 bits
- D/A Converter (DAC), 2 channels 8 bits
- Bus State Controller (BSC) for glueless connection of external devices, physical address space is divided into 6 areas, maximum pof 64 Mbytes, bus size of 8/16/32 bits, number of wait cacles settable, direct connection of SRAM, DRAM, SDRAM, and burst ROM, 2 channel PCMCIA interface support, DRAM/SDRAM controller, usable as little and big endian machine
- Pin Function Controller (PFC) is composed of registers for selecting the function of multiplexed pins

HD64461 Companion Chip

To give full system solution support a companion chip has been developed. The HD64461 also features a set of power saving stand-by modes. The typical power consumption of the HD64461 is about 50 mA at 3.3V.

The HD64461 device can be connected to the SH7709 directly and has the following main features:

- Colour/monochrome STN LCD Controller, up to 64 grey scales, 256/256K and 64K colours, CRT interface support, maximum resolution 640x480, 10 types of hardware BitBLT hardware acceleration, solid line drawing, rectangular solid colour fill function, 256Kx16 EDO DRAM display memory interface, standby mode
- PC Card Controller, v2.1 compliant, control of 2 slots simultaneously, supports IC memory card, I/O and memory card interface, external buffer control signals
- General Purpose I/O (GPIO)
- 2 channel 16-bit Timer,
- IrDA interface
- Standard 16550 compatible UART

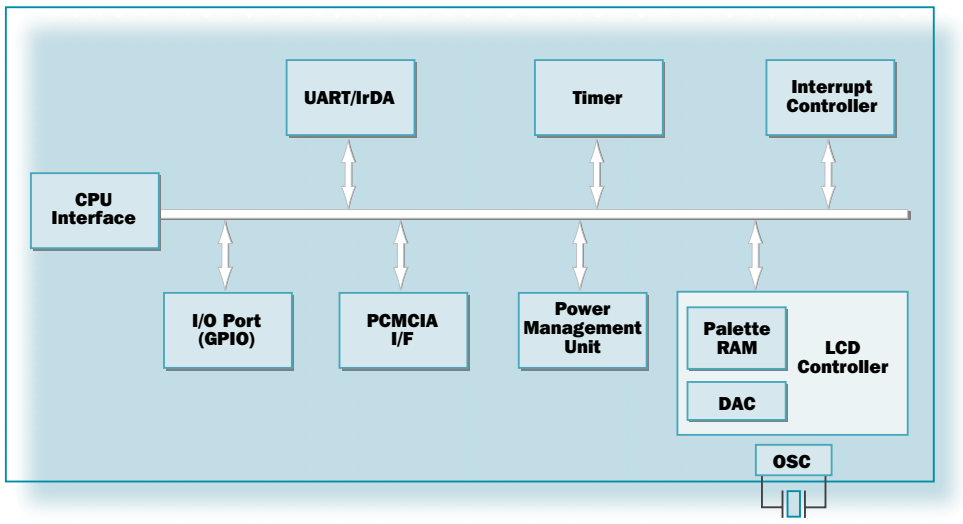


Figure 28: HD64461 Functional Block Diagram

Development Tools

A complete set of development tools for the SH7709 is directly available from Hitachi. Hitachi provides the EBX7709 development board as a hardware platform which is also available as Windows® CE ready-to-go version. The EBX7709 also supports the Hitachi Debugger Interface (HDI). An additional LCD kit is available which interfaces to the EBX7709 board, drivers for Windows® CE are available.
Other Operating System support for the SH7709 is being provided by Accelerated Technologies® (Nucleus™), Wind River Systems® (VxWorks™) and other Integrated Systems® (pSOS™).
High-level language C-compilers are available from Hitachi, Cygnus (Gnu C) and Greenhills. The Visual C/C++ development and debug environment for Windows CE is available from Microsoft.

Derivatives

The SH-3 family includes also some reduced versions such as the SH7708 device which has compared to the SH7709 less I/O ports, no DMAC, a reduced INTC, a single channel SCI, and does not have ADC or DAC. The SH7708 is also capable of running Windows® CE.

SH-3-DSP

Hitachi is also currently developing more enhanced derivatives based on an extended SH-3 architecture. The SH-3-DSP featuring additional instructions and units for Digital Signal Processing (DSP) support. The SH-3 provides instruction set upward compatibility to the SH-3-DSP architecture, also code running on the aforementioned SH-DSP is upward compatible to the SH-3-DSP:
A first member of the enhanced SH-3-DSP family will be widely compatible to the SH7709, thus providing a simple and fast upgrade path.

Application Examples

The SH-3 embedded processor family has been designed for applications such as handheld PC companions, multimedia phones, internet appliances, car information systems, navigation systems, multimedia equipment, and terminals.

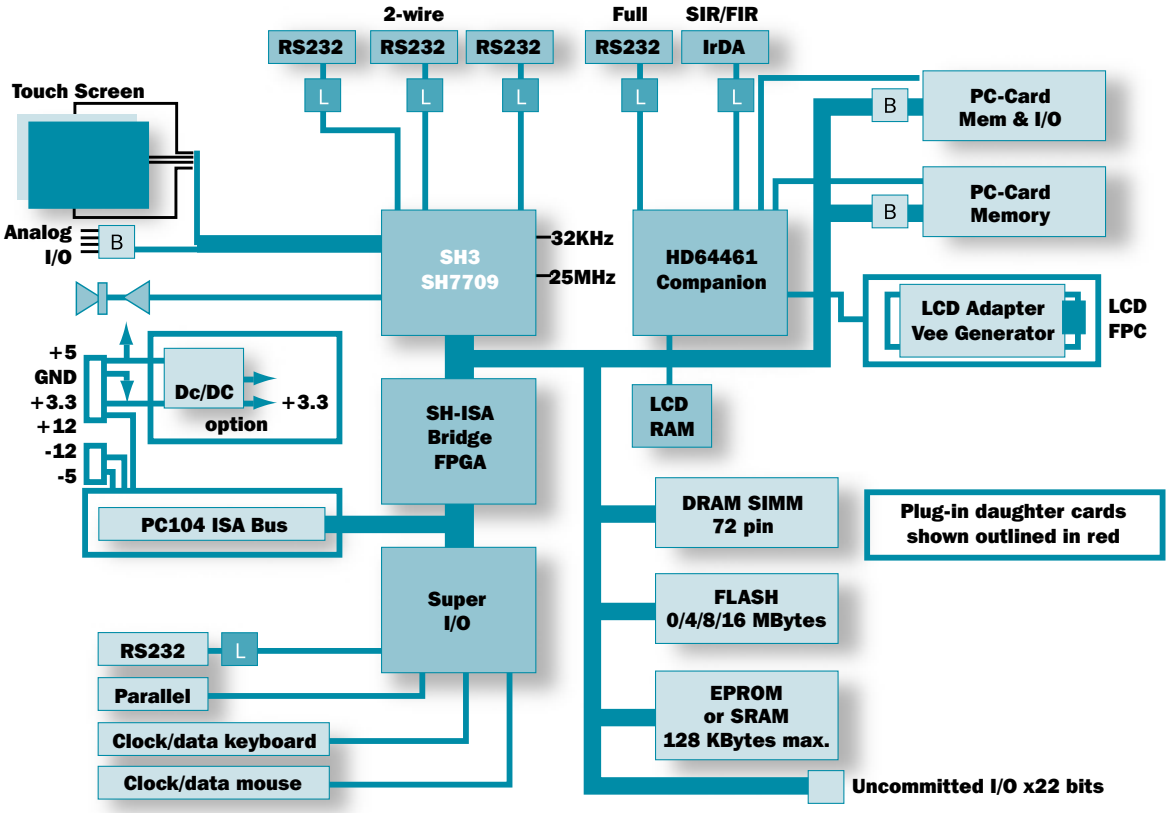


Figure 29: EBX7709 Development Board Functional Block Diagram

Related Documents:
SH7709 Hardware Manual Doument No.19-036
SH7700 Series Programming Manual Document No: 19-027
SH7708 Hardware Manual Document No: 19-029C

SH-4: The Next **Wave of Embedded** Computing

Hitachi's SH-4 architecture introduces the next wave of embedded computing processors. With superscalar features, very high clock frequencies, advanced power saving mechanisms, an integrated floating-point unit and extended high-performance graphics support, SH-4 devices are the basis for next generation multimedia consumer applications.

The SH-4 series will be supported by Windows® CE version 2.1 and higher. The SH-4's instruction set is a superset of the SH-1, SH-2, and SH-3 instruction set, thus still providing upward compatibility. This feature will provide a simple and useful upgrade route for customers using , for example, already SH-3 devices.

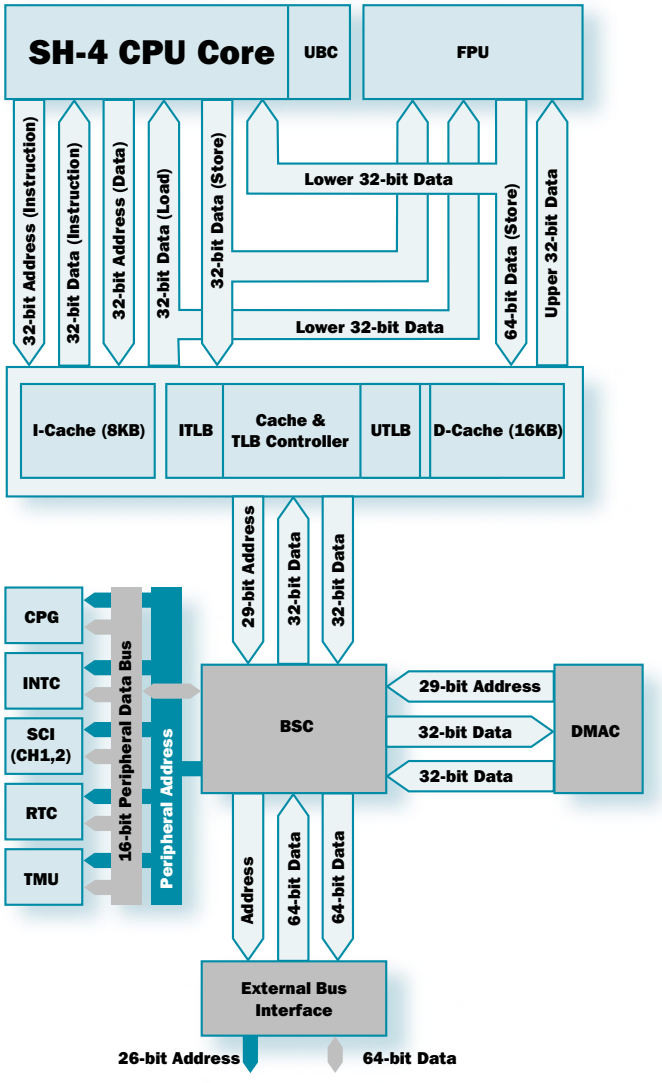


Figure 30: SH7750 Functional Block Diagram

SH-4 Architecture

The SH-4 architecture has the following main features:

- 32-bit internal data path
- 16-bit fixed-length RISC-type instruction set
- Load/Store architecture
- 5-stage pipeline
- 4 Gbyte address space
- 16 x 32-bit general registers
- 8x32-bit shadow registers
- 7 x 32-bit control registers
- 4 x 32-bit system registers
- Integrated Floating-Point co-processor (FPU)
- 3D graphics instructions
- 2-way superscalar instruction execution of Integer Unit with FPU
- 2 instructions/cycle at maximum

SH7750 Series

Based on the SH-4 architecture Hitachi will introduce SH7750 devices running with a clock frequency of up to 200 MHz and a typical power consumption of about 1.5 W at full speed. A seperated instruction and data cache will provide the throughput necessary for optimal utilization of the resources. The SH7750 features an 64-bit external bus interface and will come in a 256-pin BGA package. A further set of peripherals will be integrated simplifying systemdesign. A peak performance of 360 Dhrystone MIPS and 1.4 GFLOPs offers the performance needed for next generation multimedia applications.
Application examples are video game consoles and sub-notebook devices.

Hitachi optimised the SH7750 MMU, cache size, and peripheral mix for Windows® CE applications. Besides Microsoft's Windows® CE operating system a set of other third-party support tools will be available.

SH7750 Companion Chips

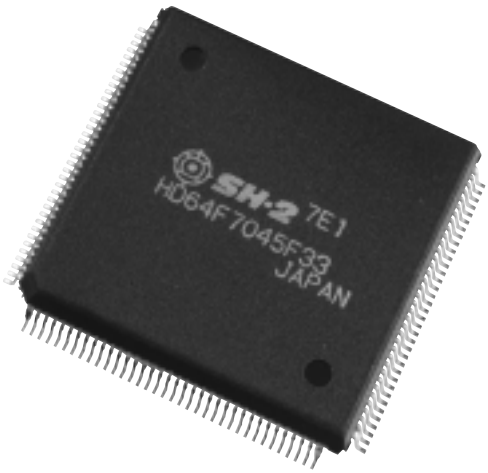
Similar to the SH-3's HD64461 companion chip, Hitachi is developing devices suitable for complete system design based on the SH7750 featuring LCD controller, embedded DRAM, and a set of advanced interfaces and peripherals. Also this set of companion chips will provide efficient power saving mechanisms especially suitable for battery-driven handheld devices.

Hitachi CD-ROM "Hitachi Electronic Components Databook" 16-007

This CD-ROM is available free of charge from Hitachi or our authorised distributors.
Please ring +49-(0)89-99180-245 to order your copy or send a fax to +49-(0)89-99180-265.
It contains approx. 20.000 pages of Hitachi documentation about microcontrollers, memories and packages. This includes the actual hardware manuals for almost all our microcontrollers, as well as application notes, programming manuals and overviews.
A powerful selection tool allows you to run a selection to find out which Hitachi microcontrollers are suitable for your application. The CD-ROM is usable under Windows and Macintosh.

Internet access / WWW

Under Hitachi's Electronic Components Group (ECG) homepage (address URL: http://www.hitachi-eu.com/hel/ecg/index.htm) you have access to detailed technical product information about Hitachi's microcontrollers, memory, displays, ASIC, discretes & power modules and optoelectronic components. For memory and microcontroller products each user can download complete data sheets and application notes in PDF format.
You will also find a complete overview over Hitachi's European Microcontroller development tools with a short description, the package contents and the ordering information (part names).


SH-2 7E1
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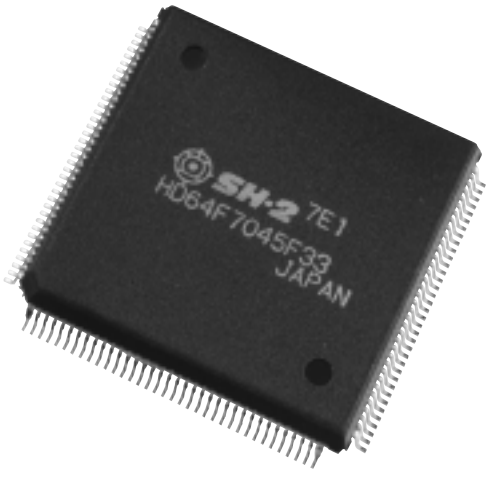
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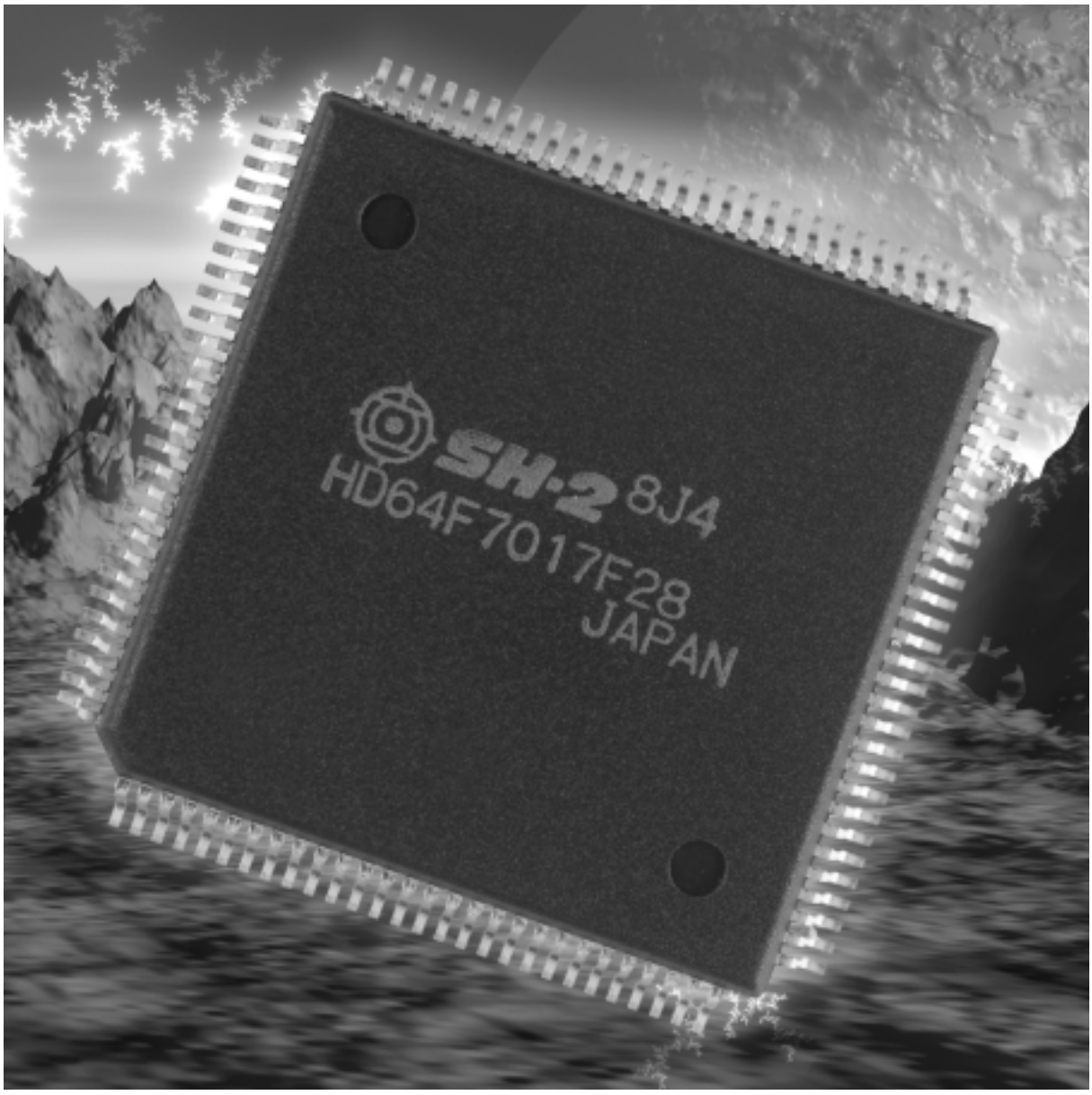
SH-2 8J4
HD64F7017F28
JAPAN

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