S93VP662/S93VP663

4K Serial E^2PROM with a Precision Low-V_{CC} Lockout Circuit

FEATURES

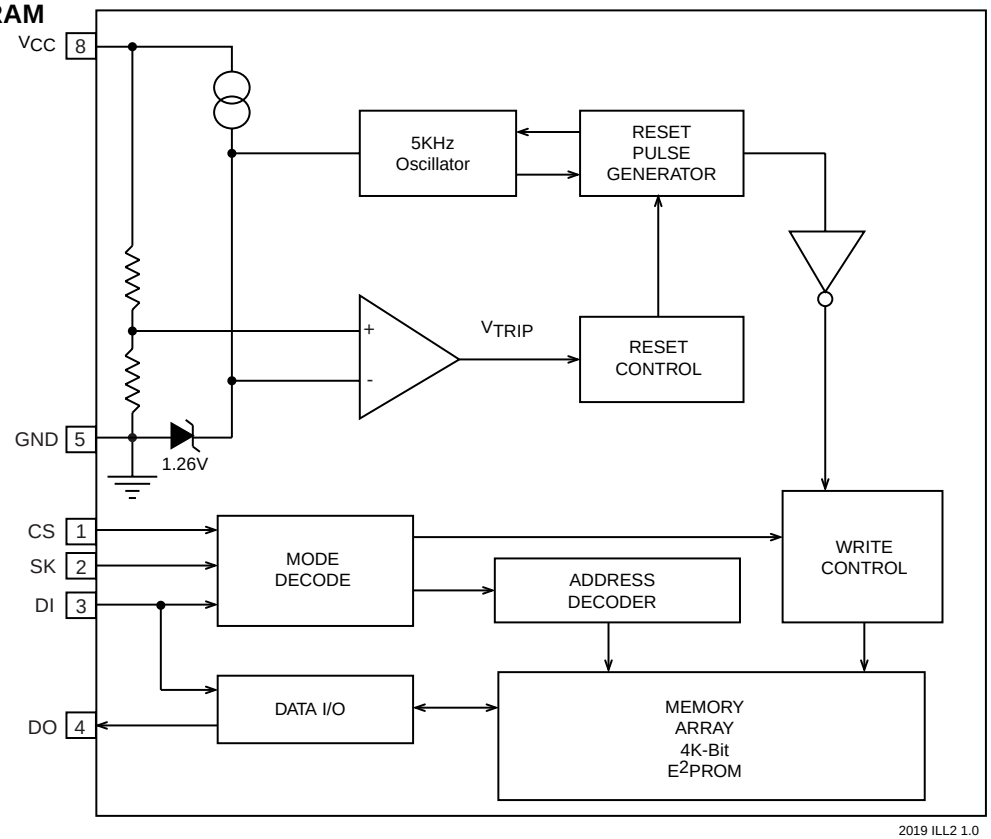
- **Voltage Protection™**
- **Precision Low-V_{CC} Write Lockout**
- **All Write Operations Inhibited When V_{CC} Falls below V_{LOCK}**
- **One 3Volt and Two 5Volt System Versions**
  - **V_{LOCK} = 2.6V+.1V/-.05V**
  - **V_{LOCK} = 4.25V +.25V/-0.0V**
  - **V_{LOCK} = 4.50 +.25V/-0.0V**
- **100% Compatible with Industry Standard Microwire Devices**
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Commercial Industrial Temperature Range**

OVERVIEW

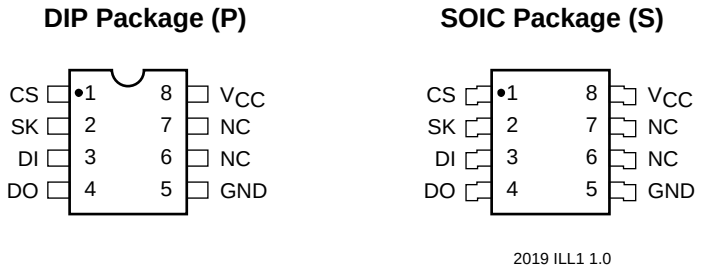
The S93VP662 and S93VP663 are 4K-bit serial E^2PROM memories integrated with a precision V_{CC} sense circuit. The sense circuit will disable write operations whenever V_{CC} falls below the V_{LOCK} voltage. They are fabricated using SUMMIT's advanced CMOS E^2PROM technology and is suitable for both 3 and 5 volt systems.

Both devices have 4k-bits of E^2PROM memory that is accessible via the industry standard microwire bus. The S93VP662 is configured with an internal ORG pin tied low providing an 8-bit byte organization and the S93VP663 is configured with an internal ORG pin tied high providing a 16-bit word organization. Both the S93VP662 and S93VP663 have page write capability. The devices are designed for a minimum 1,000,000 program/erase cycles and have data retention in excess of 100 years.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+2.7 to 6.0V Power Supply
GND	Ground

DEVICE OPERATION

APPLICATIONS

The S93VP662/VP663 was designed specifically for applications where the integrity of the stored data is paramount. In recent years, as the operating voltage range of serial E^2PROMs has widened, most semiconductor manufacturers have arbitrarily eliminated their V_{CC} sense circuits. The S93VP662/VP663 will protect your data by guaranteeing write lockout below the selected V_{CC} Lockout voltage.

V_{CC} Lockout

The S93VP662/VP663 has an on-board precision V_{CC} sense circuit. Whenever V_{CC} is below V_{LOCK}, the S93VP662/VP663 will disable the internal write circuitry. The V_{CC} lockout circuit will ensure a higher level of data integrity than can be expected from industry standard devices that have either a very loose specification or no V_{CC} lockout specification.

During a power-on sequence all writes will be inhibited below the V_{LOCK} level and will continue to be held in a write inhibit state for approximately 200ms after V_{CC} reaches, then stays at or above V_{LOCK}. The 200ms delay provides a buffer space for the microcontroller to complete its power-on initialization routines (reading is OK) while still protecting against inadvertent writes.

During a power-down sequence initiation of writes will be inhibited whenever V_{CC} falls below V_{LOCK}. This will guard against the system's microcontroller performing an inadvertent write within the 'danger zone'. (see AN003)

GENERAL OPERATION

The S93VP662/VP663 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The S93VP663 is organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. The S93VP662 is organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance

state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions is: one start bit; two op code bits and either eight (x16) or nine (x8) address/ instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the S93VP662/ VP663 will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic erase and write cycle to the memory location specified in the instruction. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deslected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

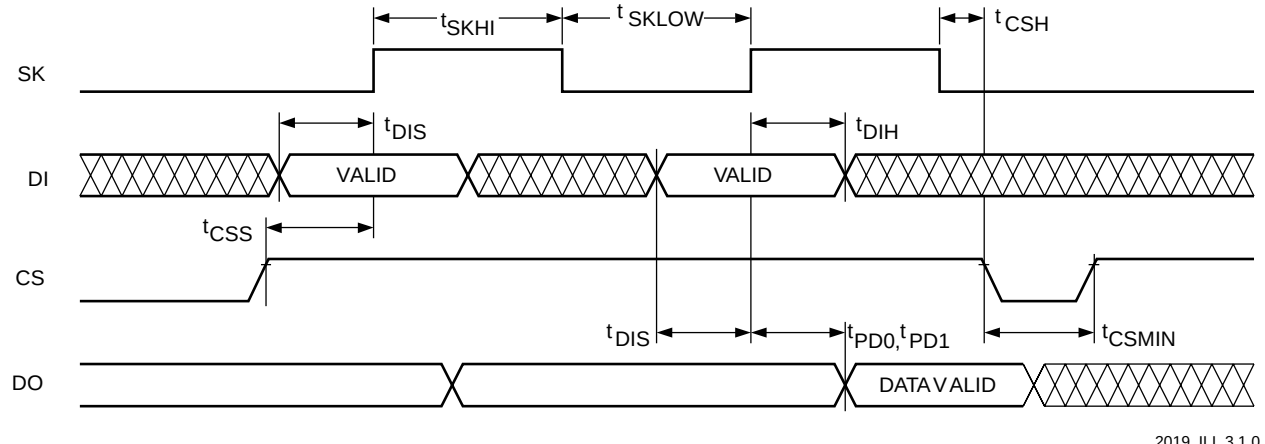


Figure 1. Sychronous Data Timing

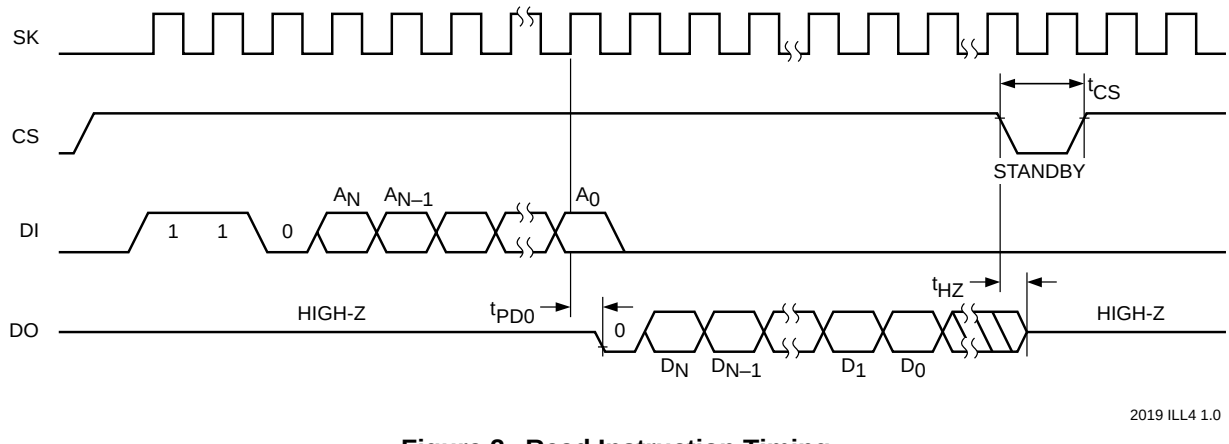


Figure 2. Read Instruction Timing

Erase/Write Enable and Disable

The S93VP662/VP663 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S93VP662/VP663 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

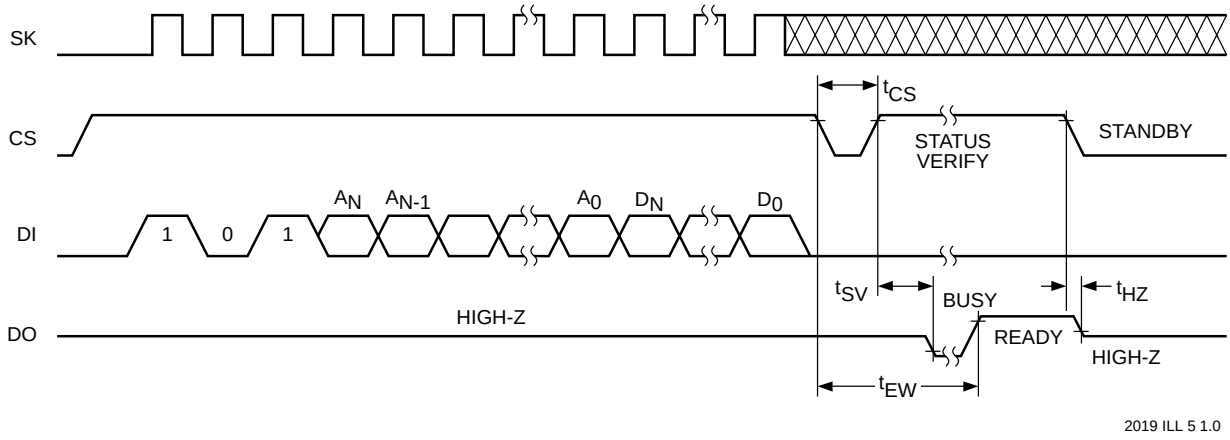


Figure 3. Write Instruction Timing

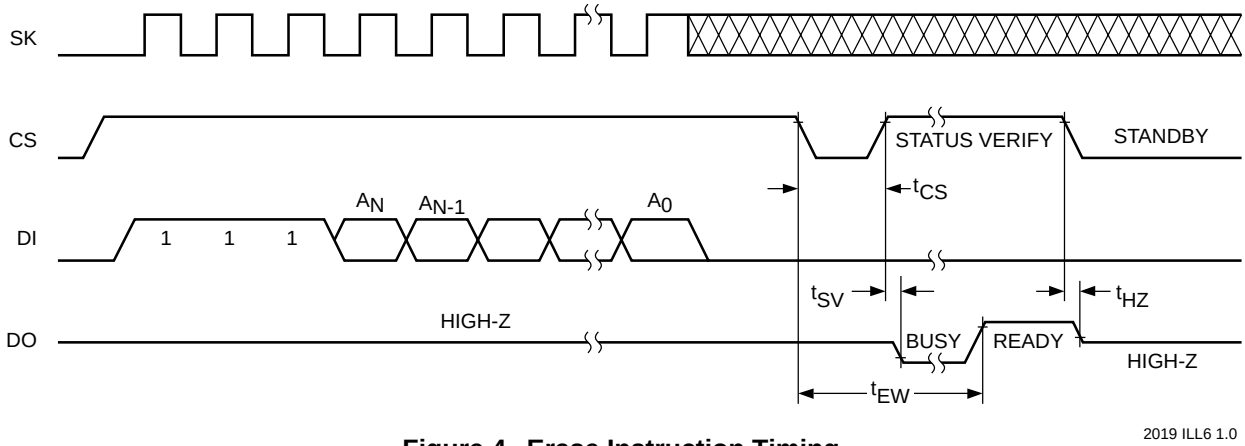


Figure 4. Erase Instruction Timing

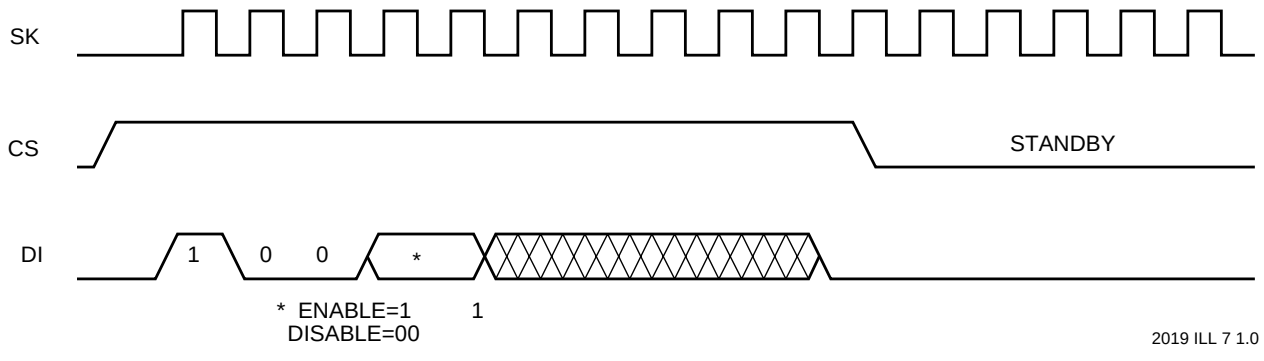


Figure 5. EWEN/EWDS Instruction Timing

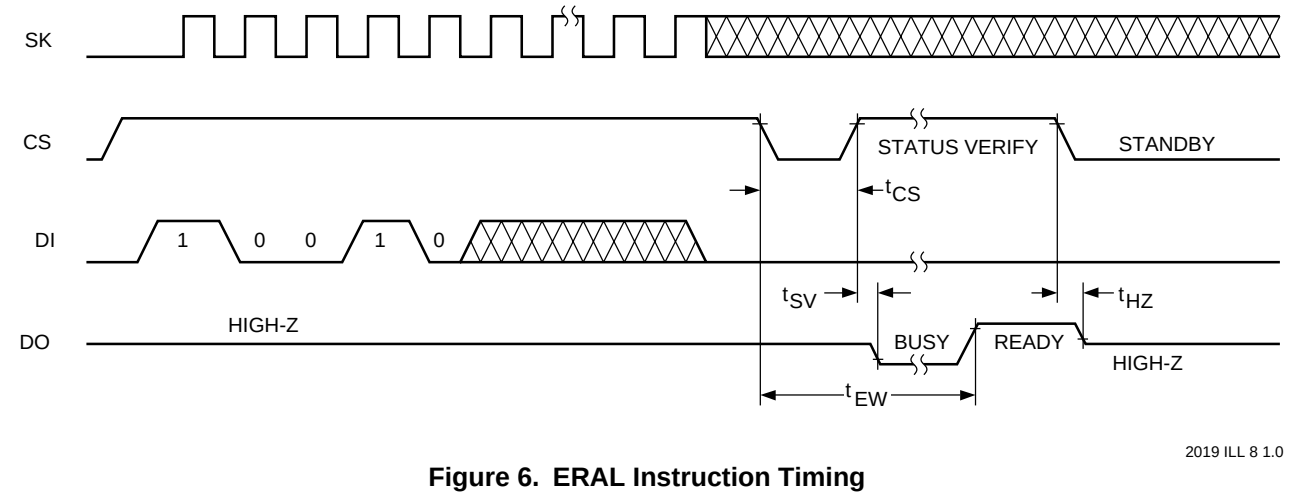


Figure 6. ERAL Instruction Timing

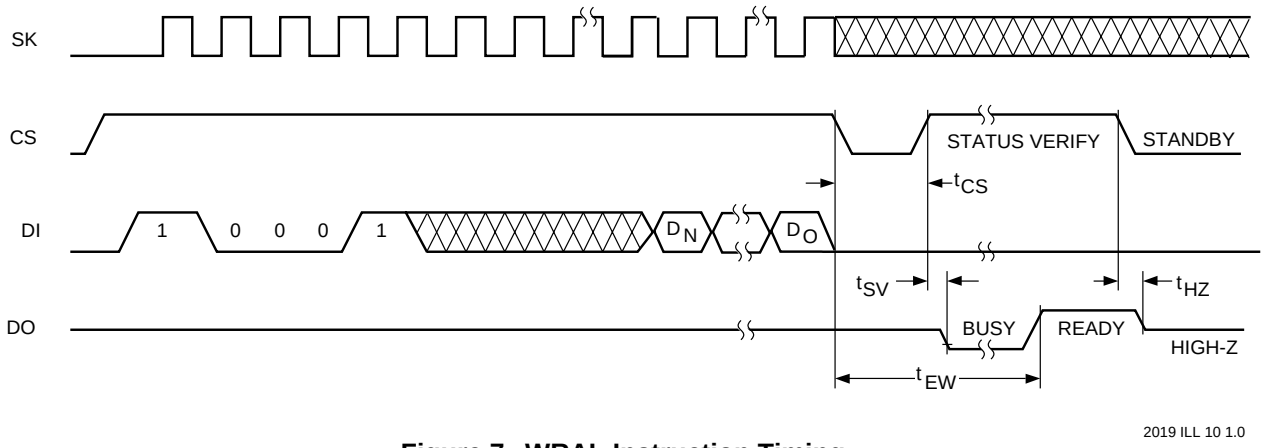


Figure 7. WRAL Instruction Timing

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			S93VP662	S93VP663	S93VP662	S93VP663	
READ	1	10	A8–A0	A7–A0			Read Address AN–A0
ERASE	1	11	A8–A0	A7–A0			Clear Address AN–A0
WRITE	1	01	A8–A0	A7–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	00	11xxx xxxx	11xxx xxx			Write Enable
EWDS	1	00	00xxx xxxx	00xxx xxx			Write Disable
ERAL	1	00	10xxx xxxx	10xxx xxx			Clear All Addresses
WRAL	1	00	11xxx xxxx	01xxx xxx	D7–D0	D15–D0	Write All Addresses

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-Up	100		mA	JEDEC Standard 17

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D.C. OPERATING CHARACTERISTICS

V_{CC} = +2.7V to +6.0V, unless otherwise specified. T_A = -40ºC to +85ºC

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f_{SK} = 1MHz V_{CC} = 5.0V, CS = 5.0V, Output Open
I_{SB}	Power Supply Current (Standby)			50	µA	CS = 0V
I_{LI}	Input Leakage Current			2	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current (Including ORG pin)			10	µA	V_{OUT} = 0V to V_{CC}, CS = 0V
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	-0.1 2		0.8 V_{CC}+1	V V	4.5V≤V_{CC}<5.5V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	0 V_{CC}X0.7		V_{CC}X0.2 V_{CC}+1	V V	1.8V≤V_{CC}<2.7V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	2.4		0.4	V V	4.5V≤V_{CC}<5.5V I_{OL} = 2.1mA I_{OH} = -400µA
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	V_{CC}-0.2		0.2	V V	1.8V≤V_{CC}<2.7V I_{OL} = 1mA I_{OH} = -100µA

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Note:

(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.

(2) Output shorted for no more than one second. No more than one output shorted at a time.

(3) This parameter is tested initially and after a design or process change that affects the parameter.

(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C_{OUT}(1)	OUTPUT CAPACITANCE (DO)	5	pF	V_{OUT}=OV
C_{IN}(1)	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V_{IN}=OV

2019 PGM T4 1.0

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS

		Limits					
		V_{CC}=2.7V-4.5V		V_{CC}=4.5V-5.5V			Test
SYMBOL	PARAMETER	Min.	Max.	Min.	Max.	UNITS	Conditions
t_{CSS}	CS Setup Time	100		50		ns	C_L = 100pF
t_{CSH}	CS Hold Time	0		0		ns	
t_{DIS}	DI Setup Time	200		100		ns	
t_{DIH}	DI Hold Time	200		100		ns	
t_{PD1}	Output Delay to 1		0.5		0.25	µs	
t_{PD0}	Output Delay to 0		0.5		0.25	µs	
t_{HZ}(1)	Output Delay to High-Z		200		100	ns	
t_{EW}	Program/Erase Pulse Width		10		10	ms	
t_{CSMIN}	Minimum CS Low Time	0.5		0.25		µs	
t_{SKHI}	Minimum SK High Time	0.5		0.25		µs	
t_{SKLOW}	Minimum SK Low Time	0.5		0.25		µs	
t_{SV}	Output Delay to Status Valid		0.5		0.25	µs	
SK_{MAX}	Maximum Clock Frequency	DC	500	DC	1000	KHZ	

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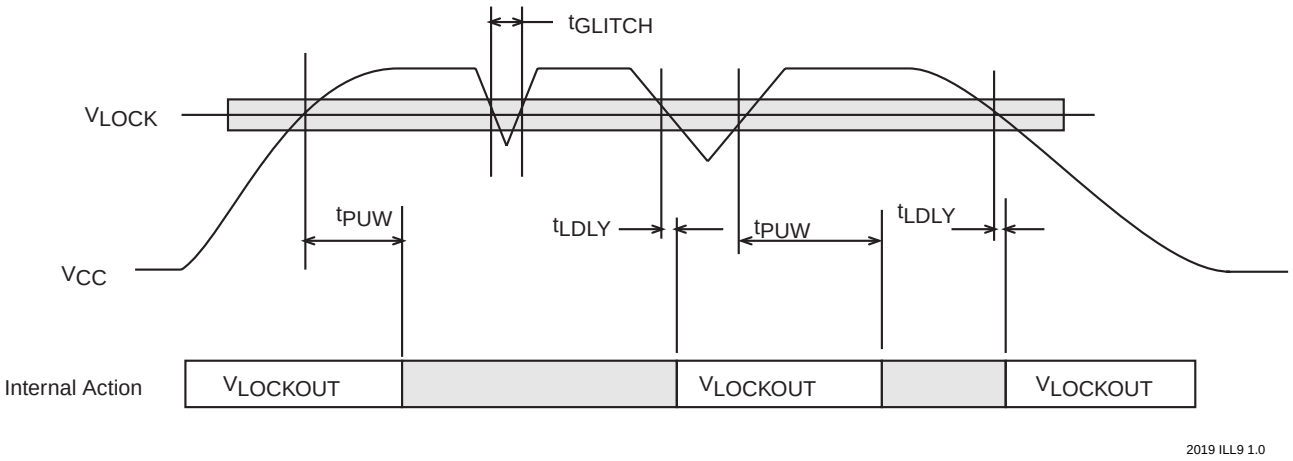
Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

V_{LOCK} CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

		S24VP662/VP663-2.7		S24VP662/VP663–A		S24VP662/VP663–B		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{LOCK}	Write Lockout Voltage Level	2.55	2.70	4.25	4.50	4.50	4.75	V
t_{PUW}	Power-Up Write Delay	130	20	130	270	130	270	ms
t_{LDLY}	Delay to $V_{LOCKOUT}$		5		5		5	µs
t_{GLITCH}	Glitch Filter		30		30		30	ns

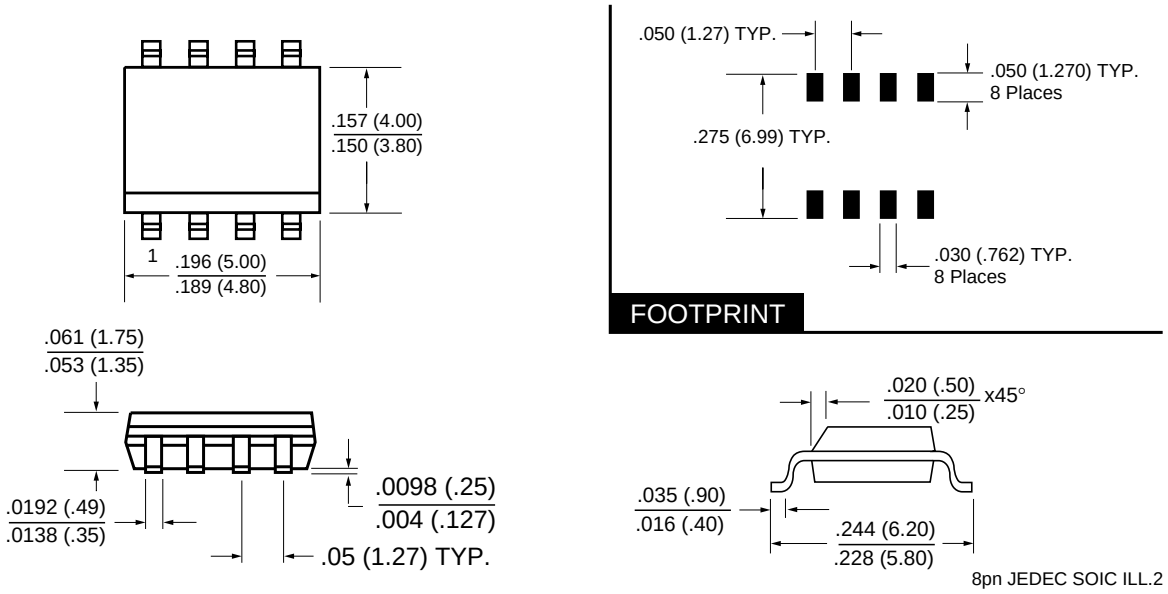
2019 PGM T1 1.3



2019 ILL9 1.0

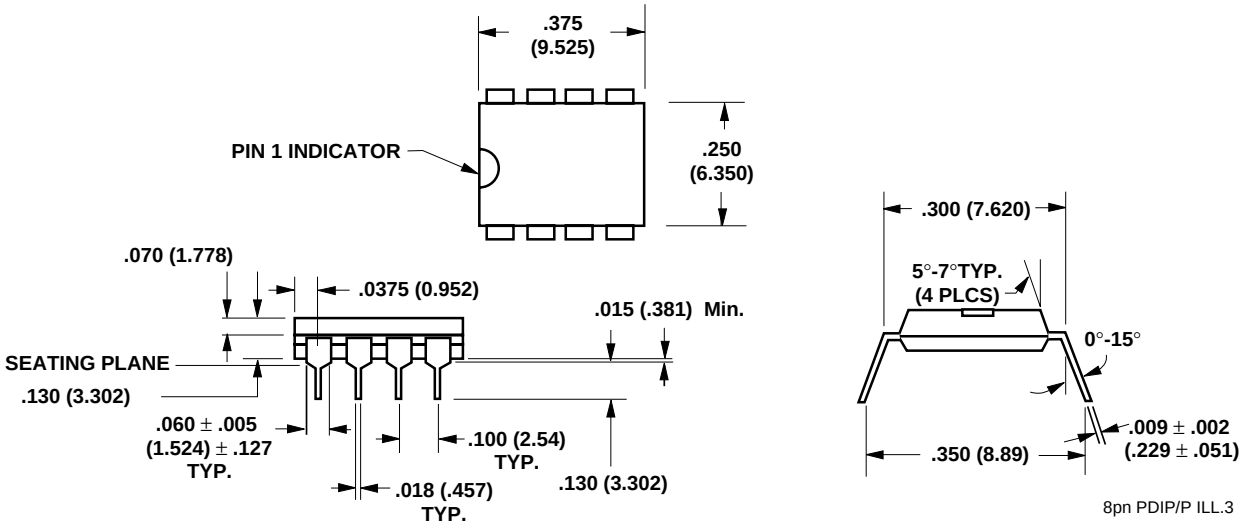
Figure 8. V_{LOCK} Timing Diagram

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



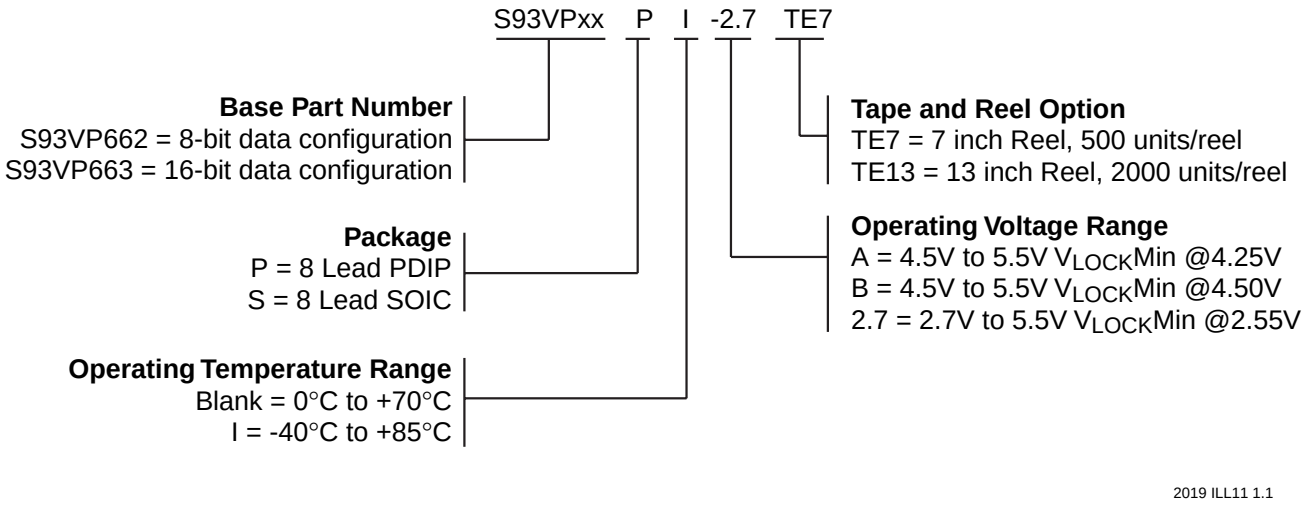
8pn JEDEC SOIC ILL.2

8 Pin PDIP (Type P) Package



8pn PDIP/P ILL.3

ORDERING INFORMATION



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