Contents

CMOS SERIAL E^2PROM

S-29UXX1A Series

The S-29UXX1A Series is low power 1K/2K/4K-bit serial E^2PROM with a low operating voltage range. They are organized as 64-wordX16-bit, 128-wordX16-bit and 256-wordX16-bit, respectively. Each is capable of sequential read, where addresses are automatically incremented in 16-bit blocks. The instruction code is compatible with the NM93CSXX Series.
The S-29UXX1A Series is capable of protecting the memory, 50% of which can be protected starting from address 00.

■ Features

- Low power consumption
  - Standby : 2.0 μA Max. (V_{CC}=3.6 V)
  - Operating : 0.6 mA Max. (V_{CC}=3.6 V)
  - : 0.4 mA Max. (V_{CC}=2.7 V)
- Low operating voltage range
  - Read : 0.9 to 3.6 V
  - Write : 1.8 to 3.6 V
- Sequential read capable
- Memory Protection
- Endurance : 10^5 cycles/word
- Data retention : 10 years
- S-29U131A : 1K bits NM93CS46 instruction code compatible
- S-29U221A : 2K bits NM93CS56 instruction code compatible
- S-29U331A : 4K bits NM93CS66 instruction code compatible

■ Pin Assignment

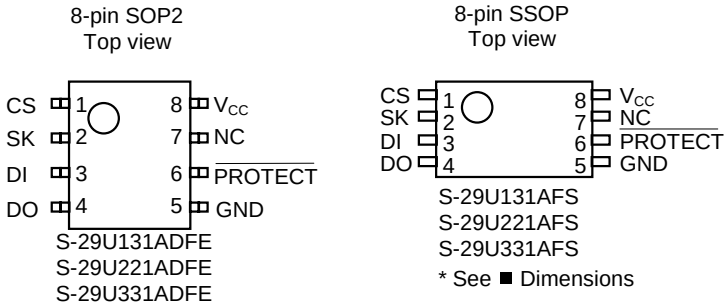


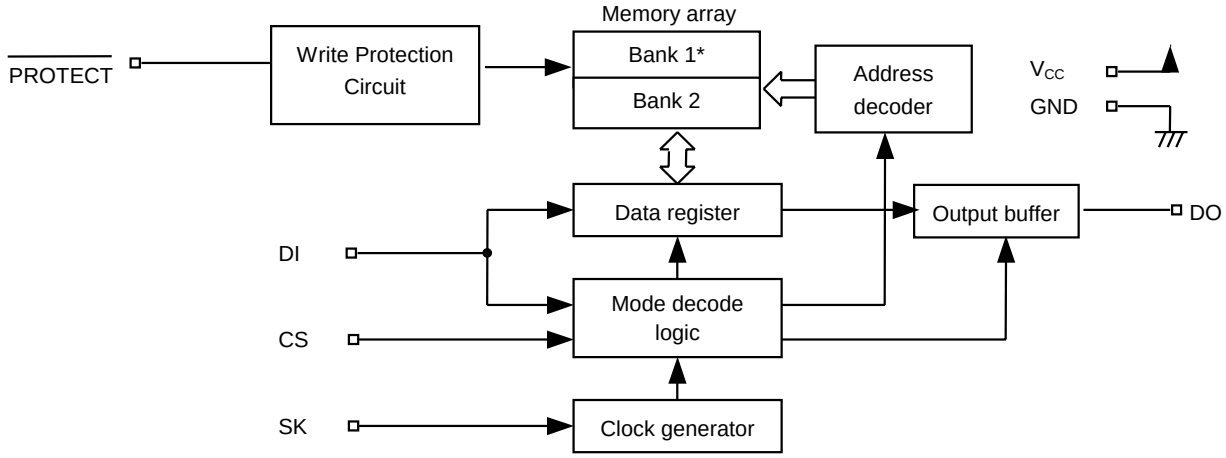
Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	SOP2	SSOP	
CS	1	1	Chip select input
SK	2	2	Serial clock input
DI	3	3	Serial data input
DO	4	4	Serial data output
GND	5	5	Ground
$\overline{\text{PROTECT}}$	6	6	Memory Protection Control Input Connected to GND or Open : Protection Valid Connected to Vcc : Protection Invalid
NC	7	7	No Connection
V_{CC}	8	8	Power supply

■ Block Diagram



* 50% of the memory can be protected starting from address 00

Figure 2

■ Instruction Set

Table 2

Instruction	Start Bit	Ope code	Address			Data
			S-29U131A	S-29U221A	S-29U331A	
READ (Read data)	1	10	A_5 to A_0	XA_6 to A_0	A_7 to A_0	D_{15} to D_0 Output*
WRITE (Write data)	1	01	A_5 to A_0	XA_6 to A_0	A_7 to A_0	D_{15} to D_0 Input
ERASE (Erase data)	1	11	A_5 to A_0	XA_6 to A_0	A_7 to A_0	—
EWEN (Program enable)	1	00	11xxxx	11xxxxxx	11xxxxxx	—
EWDS (Program disable)	1	00	00xxxx	00xxxxxx	00xxxxxx	—

x : Doesn't matter.
* : When 16-bit data of the specified address is output, the data of the next address is output.

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation Write Enable/Disable	0.9	—	3.6	V
		Write Operation	1.8	—	3.6	V
High level input voltage	V_{IH}	V_{CC}=1.8 to 3.6 V	0.8xVcc	—	Vcc	V
		V_{CC}=0.9 to 1.8 V	0.9xVcc	—	Vcc	V
Low level input voltage	V_{IL}	V_{CC}=1.8 to 3.6 V	0.0	—	0.2xVcc	V
		V_{CC}=0.9 to 1.8 V	0.0	—	0.1xVcc	V
Operating temperature	T_{opr}		-40	—	+85	°C

■ Pin Capacitance

Table 5

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN}=0 V	—	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT}=0 V	—	—	10	pF

■ Endurance

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^5	—	—	cycles/word

■ DC Electrical Characteristics

Table 7

Parameter	Smbl	Conditions	V_{CC}=2.7 V to 3.6 V			V_{CC}=1.8 V to 2.7 V			V_{CC}=0.9 to 1.8 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO unloaded	—	—	0.6	—	—	0.4	—	—	0.2	mA
Current consumption (PROGRAM)	I_{CC2}	DO unloaded	—	—	1.5	—	—	1.0				mA

Table 8

Parameter	Smbl	Conditions	V_{CC}=2.7 V to 3.6 V			V_{CC}=1.8 to 2.7 V			V_{CC}=0.9 to 1.8 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	CS=GND DO=Open Other input: Connected to V_{CC} or GND Topr=-10 to +70°C	—	—	1.0	—	—	1.0	—	—	1.0	μA
		CS=GND DO=Open Other input: Connected to V_{CC} or GND Topr=-40 to +85°C	—	—	2.0	—	—	2.0	—	—	2.0	μA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V_{OL}	I_{OL}=100 μA	—	—	0.1	—	—	0.1				V
		I_{OL}=30 μA	—	—	0.1	—	—	0.1				V
		I_{OL}=10 μA	—	—	0.1	—	—	0.1	—	—	0.2	V
High level output voltage	V_{OH}	I_{OH}=-100 μA	V_{CC}-0.7	—	—							V
		I_{OH}=-10 μA	V_{CC}-0.7	—	—	V_{CC}-0.3	—	—				V
		I_{OH}=-5 μA	V_{CC}-0.7	—	—	V_{CC}-0.3	—	—	V_{CC}-0.2	—	—	V
Write enable latch data hold voltage	V_{DH}	Only when write disable mode	0.8	—	—	0.8	—	—	0.8	—	—	V
Pull-Down Current	I_{PD}	$\overline{\text{PROTECT}}$ Terminal=V_{CC}	4	—	30	1	—	15	0.05	—	5	μA

■ AC Electrical Characteristics

Table 9 Measuring conditions

Input pulse voltage	0.1 x V_{CC} to 0.9 x V_{CC}
Output reference voltage	0.5 x V_{CC}
Output load	100pF

Table 10

Parameter	Smbl	Conditions	V_{CC}=2.7 to 3.6V			V_{CC}=1.8 to 2.7 V			V_{CC}=0.9 to 1.8V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	t_{CSS}		0.4	—	—	1.0	—	—	10	—	—	µs
CS hold time	t_{CSH}		0.4	—	—	1.0	—	—	10	—	—	µs
CS deselect time	t_{CDS}		0.2	—	—	0.4	—	—	4	—	—	µs
Data setup time	t_{DS}		0.4	—	—	0.8	—	—	8	—	—	µs
Data hold time	t_{DH}		0.4	—	—	0.8	—	—	8	—	—	µs
Output delay time	t_{PD}	Topr=-10 to +70°C	—	—	1.0	—	—	2.0	—	—	50	µs
		Topr=-40 to +85°C	—	—	1.0	—	—	2.0	—	—	100	µs
Clock frequency	f_{SK}	Topr=-10 to +70°C	0	—	500	0	—	250	—	—	10	kHz
		Topr=-40 to +85°C	0	—	500	0	—	250	—	—	5	kHz
Clock pulse width	t_{SKH}	Topr=-10 to +70°C	1.0	—	—	2.0	—	—	50	—	—	µs
	t_{SKL}	Topr=-40 to +85°C	1.0	—	—	2.0	—	—	100	—	—	µs
Output disable time	t_{HZ1} t_{HZ2}		0	—	0.5	0	—	1.0	0	—	50	µs
Output enable time	t_{SV}		0	—	0.5	0	—	1.0	0	—	50	µs
Programming time	t_{PR}		—	4.0	10.0	—	4.0	10.0				ms

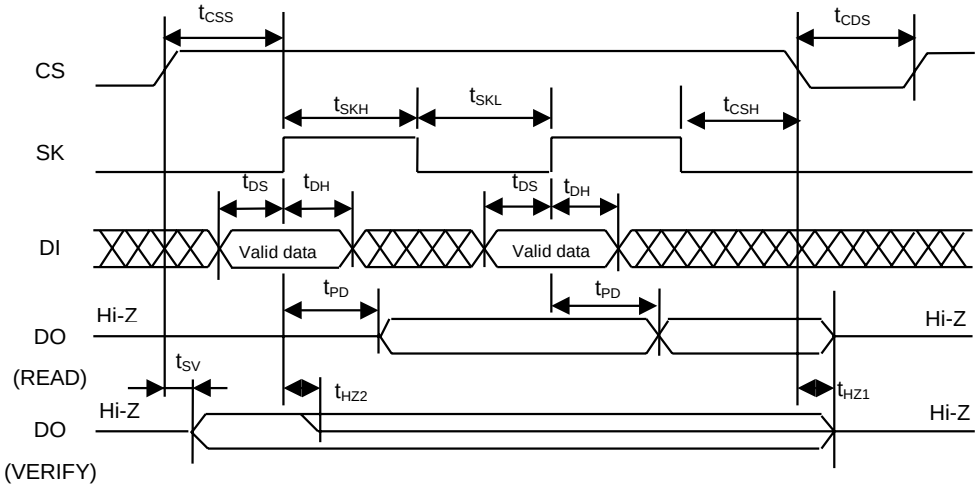


Figure 3 Timing Chart

■ Operation

Instructions (in the order of start-bit, instruction, address, and data) are latched to DI in synchronization with the rising edge of SK after CS goes high. A start-bit can only be recognized when the high of DI is latched at the rising edge of SK after changing CS to high, it is impossible for it to be recognized as long as DI is low, even if there are SK pulses after CS goes high. Any SK pulses input while DI is low before receiving a start-bit are called "dummy clocks." The number of clocks transmitted by the serial interface in a CPU and the number of clocks needed for operation of the serial memory IC can be adjusted by inserting several dummy clocks before a start-bit. Instruction finishes when CS goes low, where it must be low between commands during t_{CDS}.

All input, including DI and SK signals, is ignored while CS is low, which is stand-by mode.

1. Read

The READ instruction reads data from a specified address. After A0 is latched at the rising edge of SK, DO output changes from a high-impedance state (Hi-Z) to low level output. 16-bit data is continuously output in synchronization with the rise of SK.

When all of the data (D_{15} to D_0) in the specified address has been read, the data in the next address can be read with the input of another SK clock. Thus, the data over whole area of the memory can be read by continuously inputting SK clocks as long as CS is high.

The last address (An ⋯ A1 A0 = 1 ⋯ 11) rolls over to the top address (An ⋯ A0 = 0 ⋯ 00).

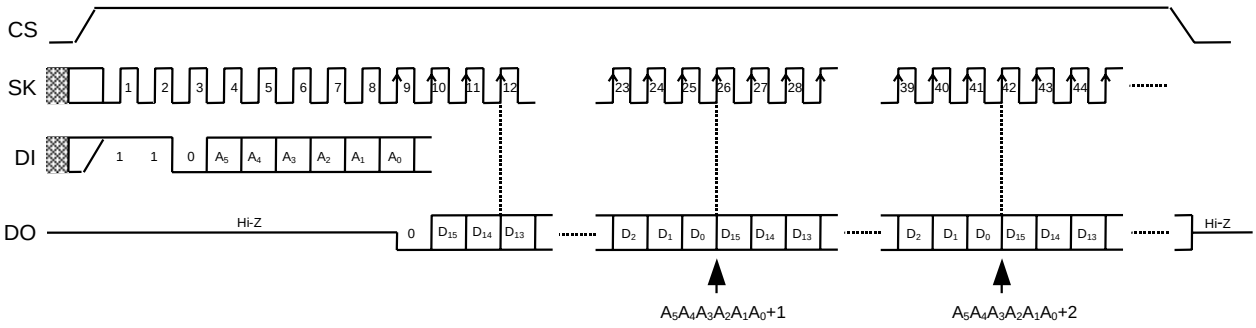


Figure 4 Read Timing (S-29U131A)

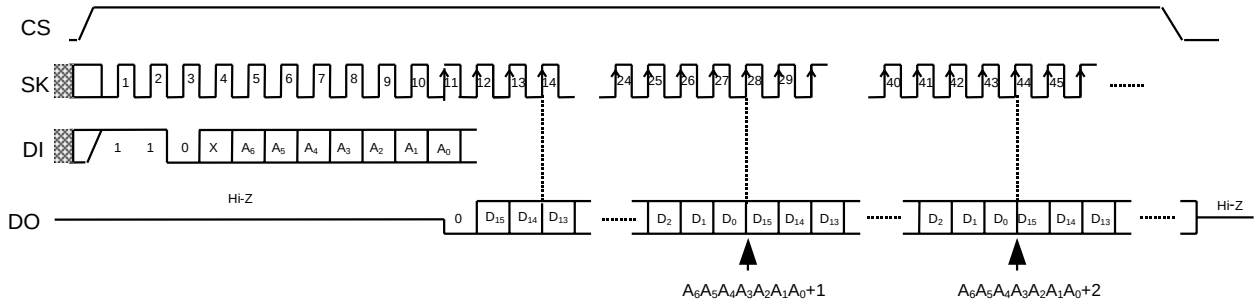


Figure 5 Read Timing (S-29U221A)

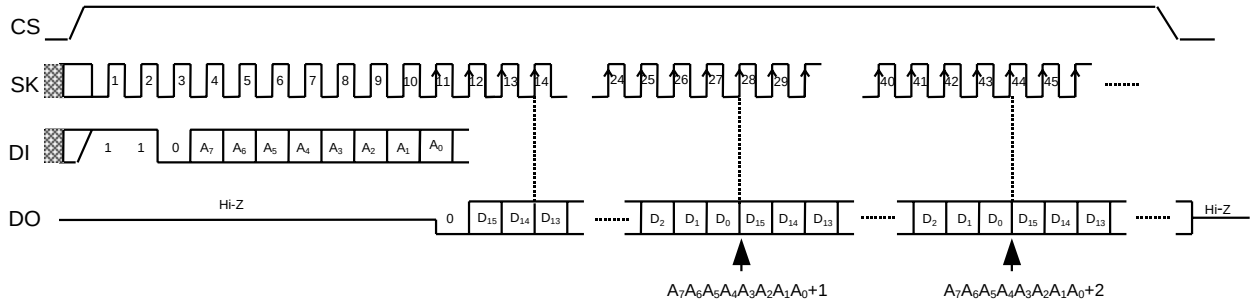


Figure 6 Read Timing (S-29U331A)

2. Write (WRITE, ERASE)

There are two write instructions, WRITE, ERASE. Each automatically begins writing to the non-volatile memory when CS goes low at the completion of the specified clock input.

The write operation is completed in 10 ms (t_{PR} Max.), and the typical write period is less than 5 ms. In the S-29UXX1A Series, it is easy to VERIFY the completion of the write operation in order to minimize the write cycle by setting CS to high and checking the DO pin, which is low during the write operation and high after its completion. This VERIFY procedure can be executed over and over again. There are two methods to detect a change in the DO output. One is to detect a change from low to high setting CS to high, and the other is to detect a change from low to high as a result of repetitous operations of returning the CS to low after setting CS to high and checking the DO output.

Because all SK and DI inputs are ignored during the write operation, any input of instruction will also be disregarded. When DO outputs high after completion of the write operation or if it is in the high-impedence state (Hi-Z), the input of instructions is available. Even if the DO pin remains high, it will enter the high-impedence state upon the recognition of a high of DI (start-bit) attached to the rising edge of an SK pulse.

DI input should be low during the VERIFY procedure.

2.1 WRITE

This instruction writes 16-bit data to a specified address.
After changing CS to high, input a start-bit, op-code (WRITE), address, and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing CS to low will start the WRITE operation. It is not necessary to make the data "1" before initiating the WRITE operation.

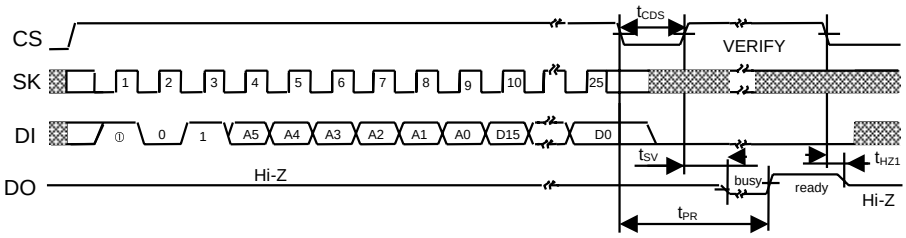


Figure 7 WRITE Timing (S-29U131A)

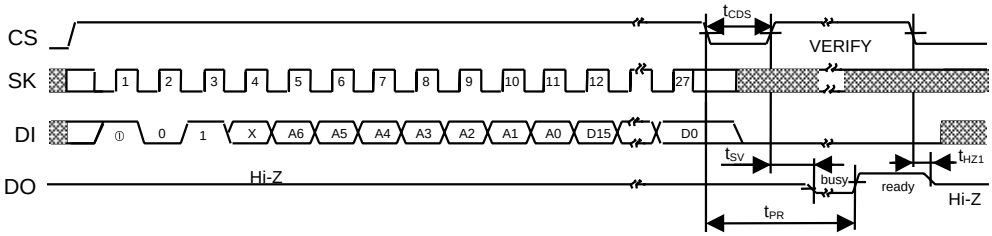


Figure 8 WRITE Timing (S-29U221A)

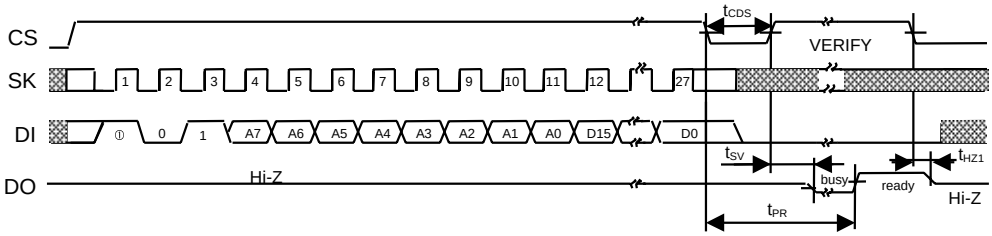


Figure 9 WRITE Timing (S-29U331A)

2.2 ERASE

This command erases 16-bit data in a specified address.
After changing CS to high, input a start-bit, op-code (ERASE), and address. It is not necessary to input data.
Changing CS to low will start the ERASE operation, which changes every bit of the 16 bit data to "1."

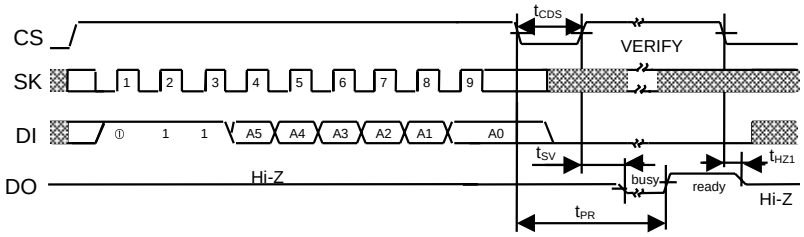


Figure 10 ERASE Timing (S-29U131A)

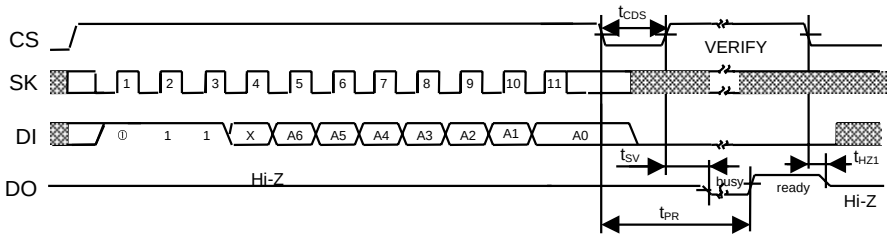


Figure 11 ERASE Timing (S-29U221A)

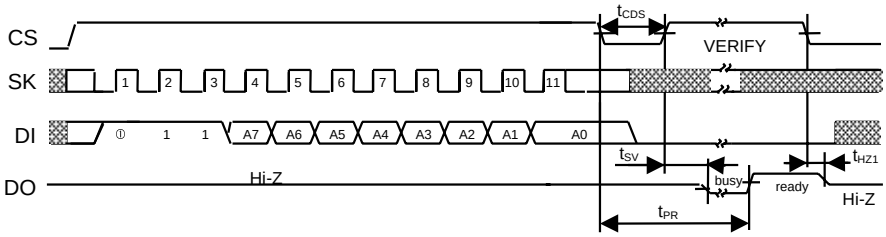


Figure 12 ERASE Timing (S-29U331A)

3. Write enable (EWEN) and Write disable (EWDS)

The EWEN instruction puts the S-29UXX1A Series into write enable mode, which accepts WRITE, ERASE instructions. The EWDS instruction puts the S-29UXX1A Series into write disable mode, which refuses WRITE, ERASE instructions.
The S-29UXX1A Series powers on in write disable mode, which protects data against unexpected, erroneous write operations caused by noise and/or CPU malfunctions. It should be kept in write disable mode except when performing write operations.

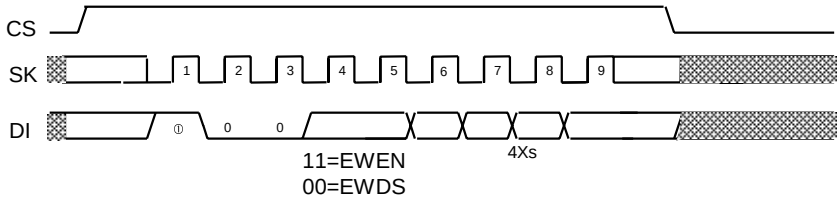


Figure 13 EWEN/EWDS Timing (S-29U131A)

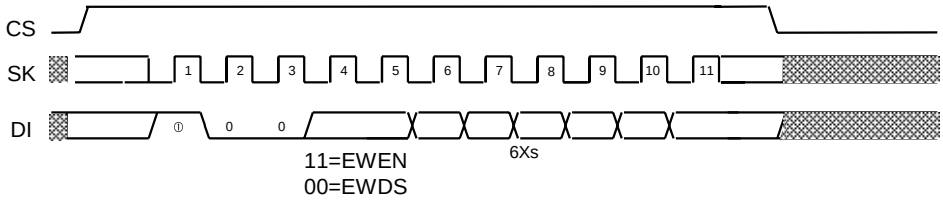


Figure 14 EWEN/EWDS Timing (S-29U221A)

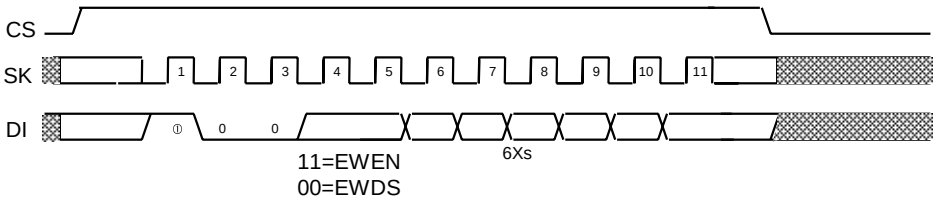


Figure 15 EWEN/EWDS Timing (S-29U331A)

Receiving a Start-Bit

A start-bit can be recognized by latching the high level of DI at the rising edge of SK after changing CS to high (Start-Bit Recognition). The write operation begins by inputting the write instruction and setting CS to low. The DO pin then outputs low during the write operation and high at its completion by setting CS to high (Verify Operation). Therefore, only after a write operation, in order to accept the next command by having CS go high, the DO pin is switched from a state of high-impedance to a state of data output; but if it recognizes a start-bit, the DO pin returns to a state of high-impedance (see Figure 3).

Make sure that data output from the CPU does not interfere with the data output from the serial memory IC when you configure a 3-wire interface by connecting DI input pin and DO output pin. Such interference may cause a start-bit fetch problem.

Three-wire Interface (DI-DO direct connection)

Although the normal configuration of a serial interface is a 4-wire interface to CS, SK, DI, and DO, a 3-wire interface is also a possibility by connecting DI and DO. However, since there is a possibility that the DO output from the serial memory IC will interfere with the data output from the CPU with a 3-wire interface, install a resistor between DI and DO in order to give preference to data output from the CPU to DI (See Figure 16).

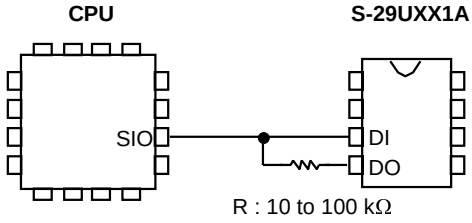


Figure 16

Memory Protection

The S-29UXX1A Series is capable of protecting the memory. So, the contents of the memory will not be miswritten due to error run or malfunction of the CPU. When the $\overline{\text{PROTECT}}$ terminal is connected to GND or OPEN, write to Bank 1 in the memory array is prohibited (50% of the memory can be protected starting from address 00). Because the pull-down resistance is connected to the $\overline{\text{PROTECT}}$ terminal internally, the memory can be automatically protected when the $\overline{\text{PROTECT}}$ terminal is OPEN. When the protection is valid, the data in the memory of Bank 1 will not be rewritten. However, because the write control circuit inside the IC functions, the next instruction cannot be executed during the time period of writing (t_{PR}). While write instruction is being input and write is being executed, always connect the $\overline{\text{PROTECT}}$ terminal to "H," "L" or OPEN, and leave the input signal unchanged (see Figure 17).

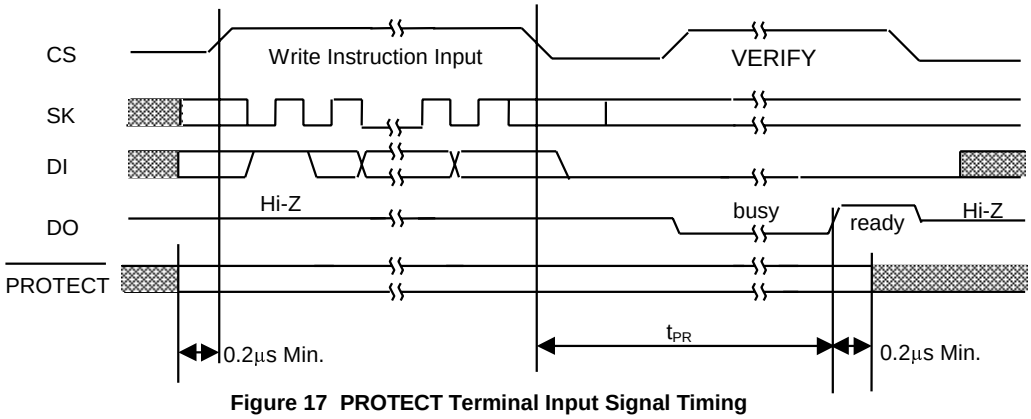


Figure 17 PROTECT Terminal Input Signal Timing

■ Dimensions (Unit : mm)

1. 8-pin SOP

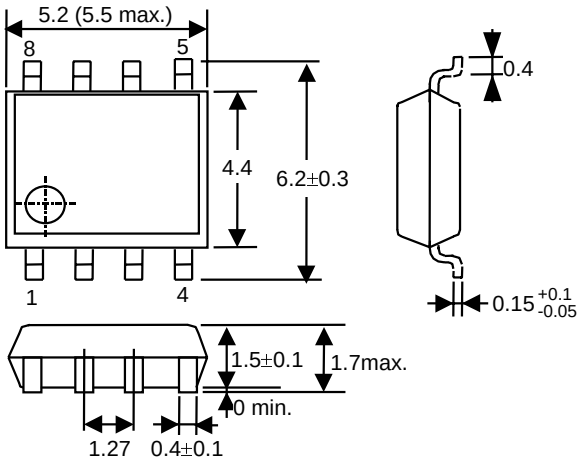


Figure 18

2. 8-pin SSOP

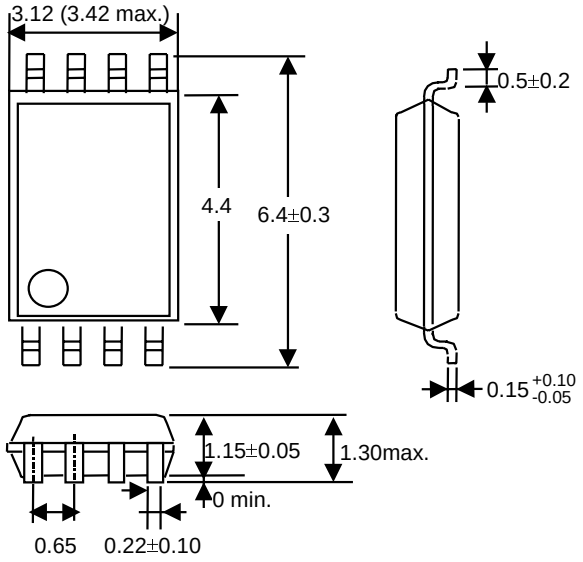


Figure 19

■ Ordering Information

S-29UXX1A XXX

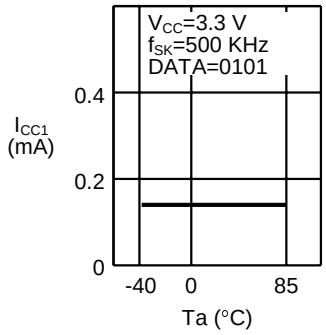
Package DFE : SOP2
FS : SSOP

Product name S-29U131A : 1K-bit
S-29U221A : 2K-bit
S-29U331A : 4K-bit

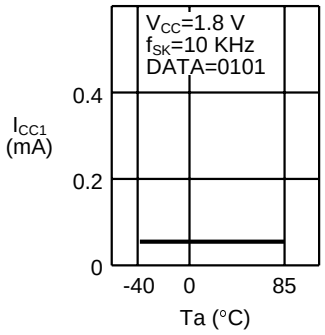
■ Characteristics

1. DC Characteristics

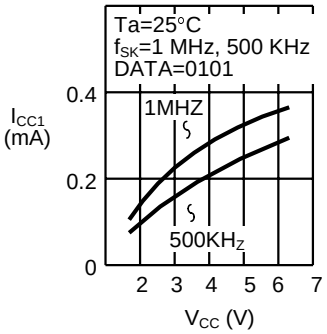
1.1 Current consumption (READ) I_{CC1} — Ambient temperature Ta



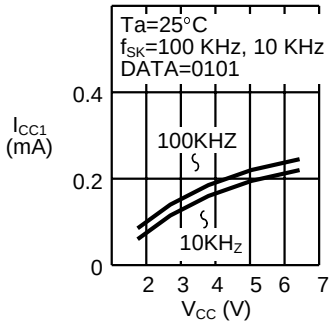
1.2 Current consumption (READ) I_{CC1} — Ambient temperature Ta



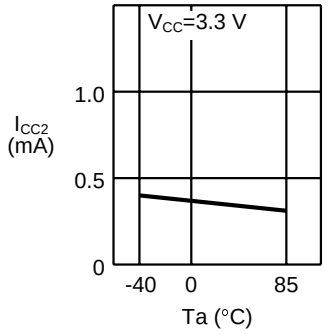
1.3 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



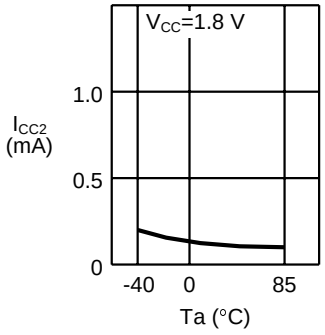
1.4 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



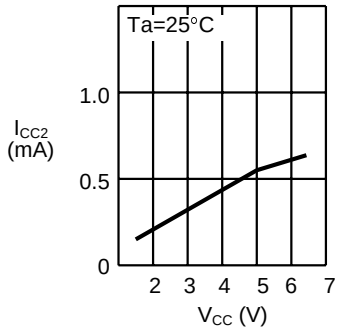
1.5 Current consumption (PROGRAM) I_{CC2} - Ambient temperature Ta



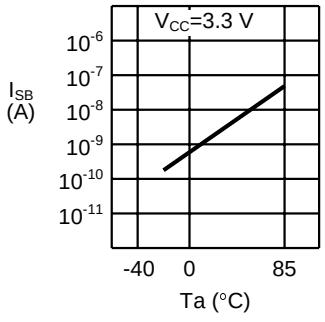
1.6 Current consumption (PROGRAM) I_{CC2} - Ambient temperature Ta



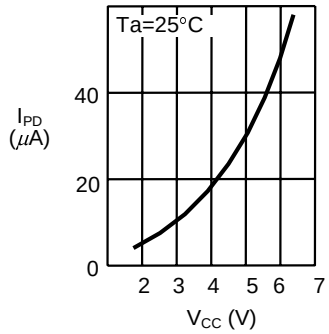
1.7 Current consumption (PROGRAM) I_{CC2} - Power supply voltage V_{CC}



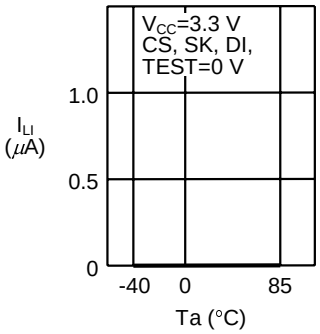
1.8 Standby current consumption I_{SB} — Ambient temperature Ta



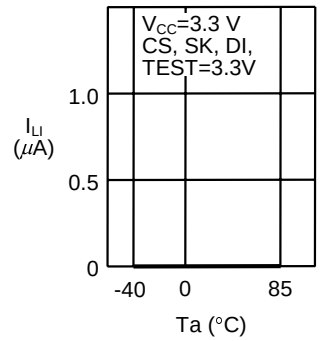
1.9 Pull-Down current I_{PD} — Power supply voltageV_{CC}



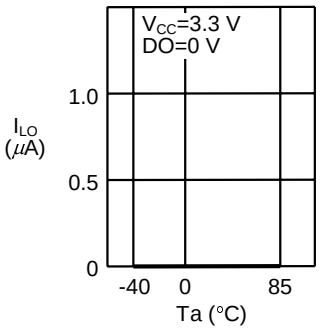
1.10 Input leakage current I_{LI} - Ambient temperature Ta



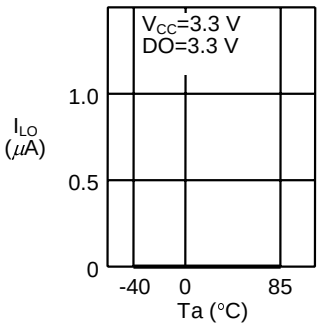
1.11 Input leakage current I_{LI} - Ambient temperature Ta



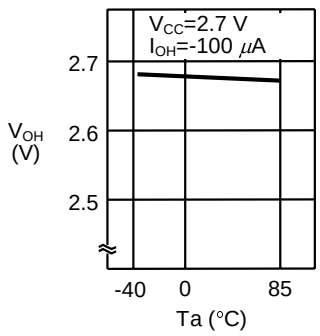
1.12 Output leakage current I_{LO} - Ambient temperature Ta



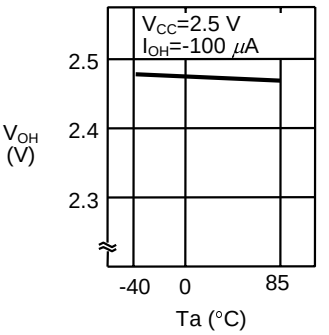
1.13 Output leakage current I_{LO} - Ambient temperature Ta



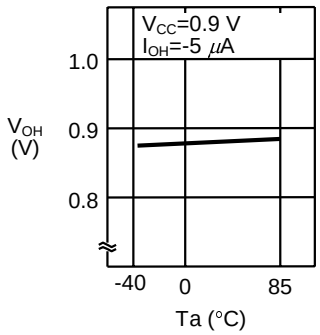
1.14 High level output voltage V_{OH} - Ambient temperature Ta



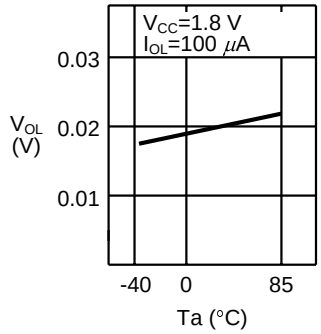
1.15 High level output voltage V_{OH} - Ambient temperature Ta



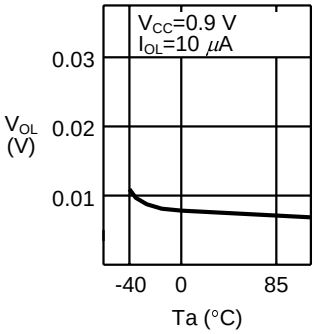
1.16 High level output voltage V_{OH} - Ambient temperature Ta



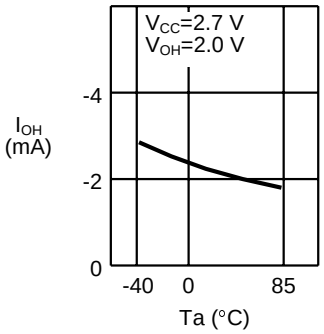
1.17 Low level output voltage V_{OL} - Ambient temperature Ta



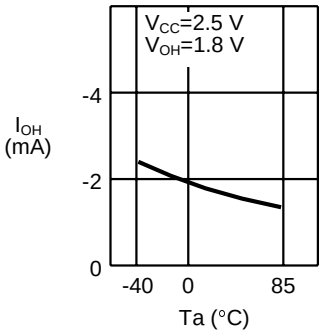
1.18 Low level output voltage V_{OL} - Ambient temperature Ta



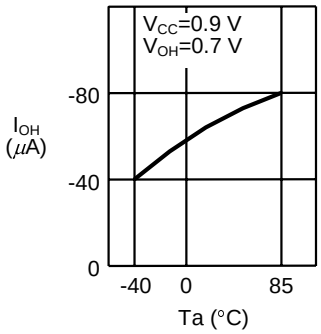
1.19 High level output current I_{OH} - Ambient temperature Ta



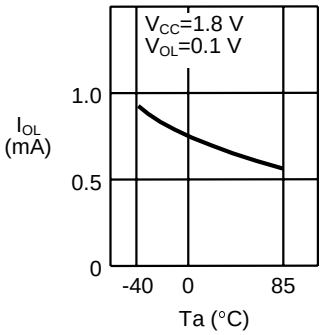
1.20 High level output current I_{OH} - Ambient temperature Ta



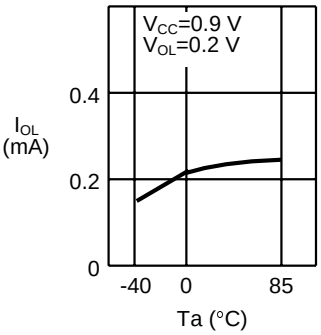
1.21 High level output current I_{OH} - Ambient temperature Ta



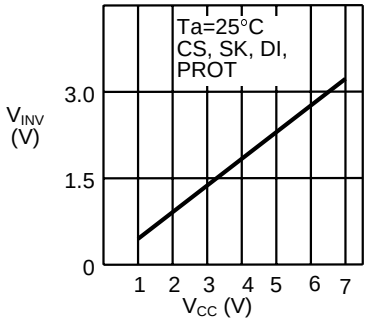
1.22 Low level output current I_{OL} - Ambient temperature Ta



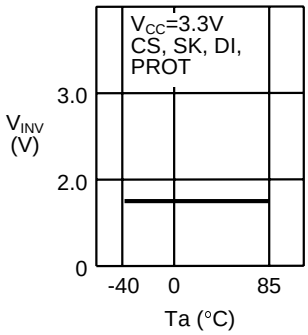
1.23 Low level output current I_{OL} - Ambient temperature Ta



1.24 Input inversion voltage V_{INV} - Power supply voltage V_{CC}

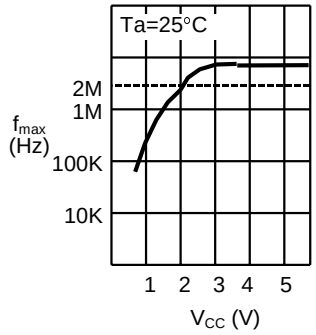


1.25 Input inversion voltage V_{INV} - Ambient temperature Ta

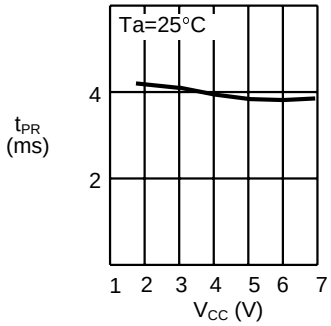


2. AC Characteristics

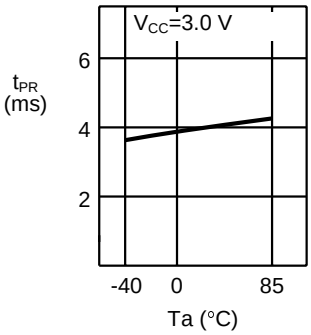
2.1 Maximum operating frequency f_{max} - Power supply voltage V_{CC}



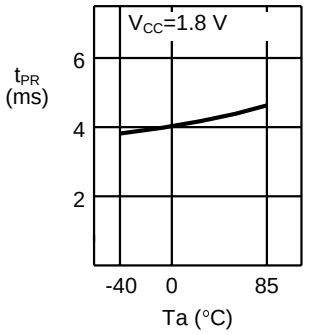
2.2 Program time t_{PR} - Power supply voltage V_{CC}



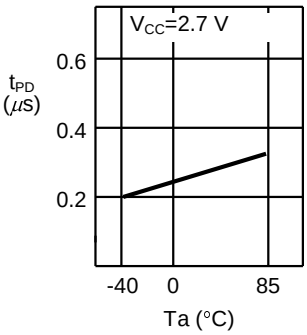
2.3 Program time t_{PR} - Ambient temperature Ta



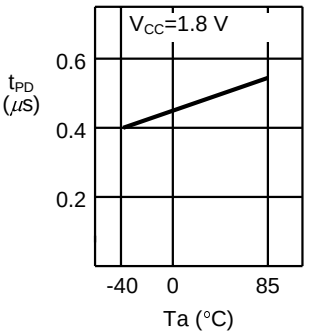
2.4 Program time t_{PR} - Ambient temperature Ta



2.5 Data output delay time t_{PD} - Ambient temperature Ta



2.6 Data output delay time t_{PD} - Ambient temperature Ta



2.7 Data output delay time t_{PD} - Ambient temperature Ta