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CMOS 2-WIRED SERIAL EEPROM

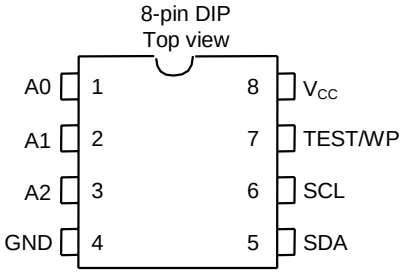
S-24C01A/02A/04A

The S-24C0XA is a series of 2-wired, low power 1K/2K/4K-bit EEPROMs with a wide operating range. They are organized as 128-word × 8-bit, 256-word × 8-bit, and 512-word × 8-bit, respectively. Each is capable of page write, and sequential read.
The time for byte write and page write is the same, i. e., 1 msec. (max.) during operation at 5 V ± 10%.

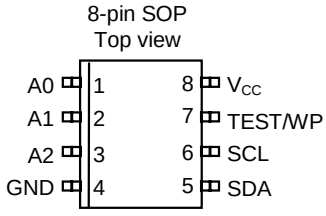
■ Features

- Low power consumption
  Standby: 1.0 μA Max. (V_{CC}=5.5 V)
  Operating: 0.4 mA Max. (V_{CC}=5.5 V)
  0.3 mA Max. (V_{CC}=3.3 V)
- Wide operating voltage range
  Write: 2.5 to 5.5 V
  Read: 1.8 to 5.5 V
- Page write
  8 bytes (S-24C01A, S-24C02A)
  16 bytes (S-24C04A)
- Sequential read capable
- Endurance: 10^5 cycles/word
- Data retention: 10 years
- Write protection: S-24C02A, S-24C04A
- S-24C01A: 1 kbits
- S-24C02A: 2 kbits
- S-24C04A: 4 kbits

■ Pin Assignment



S-24C01ADPX-01
S-24C02ADPX-01
S-24C04ADPX-01



S-24C01AFJX-χχ-01
S-24C02AFJX-χχ-01
S-24C04AFJX-χχ-01

* X differs depending on the package type.
χχ differs depending on the packing form.
See ■ Dimensions and ■ Ordering Information.

Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	DIP	SOP	
A0	1	1	Address input (no connection in the S-24C04A*)
A1	2	2	Address input
A2	3	3	Address input
GND	4	4	Ground
SDA	5	5	Serial data input/output
SCL	6	6	Serial clock input
TEST/WP	7	7	TEST pin (S-24C01A): Connected to GND. WP (Write Protection) pin (S-24C02A, S-24C04A): * Connected to Vcc: Protection valid * Connected to GND: Protection invalid
V_{CC}	8	8	Power supply

* When in use, connect to GND or Vcc.

■ Block Diagram

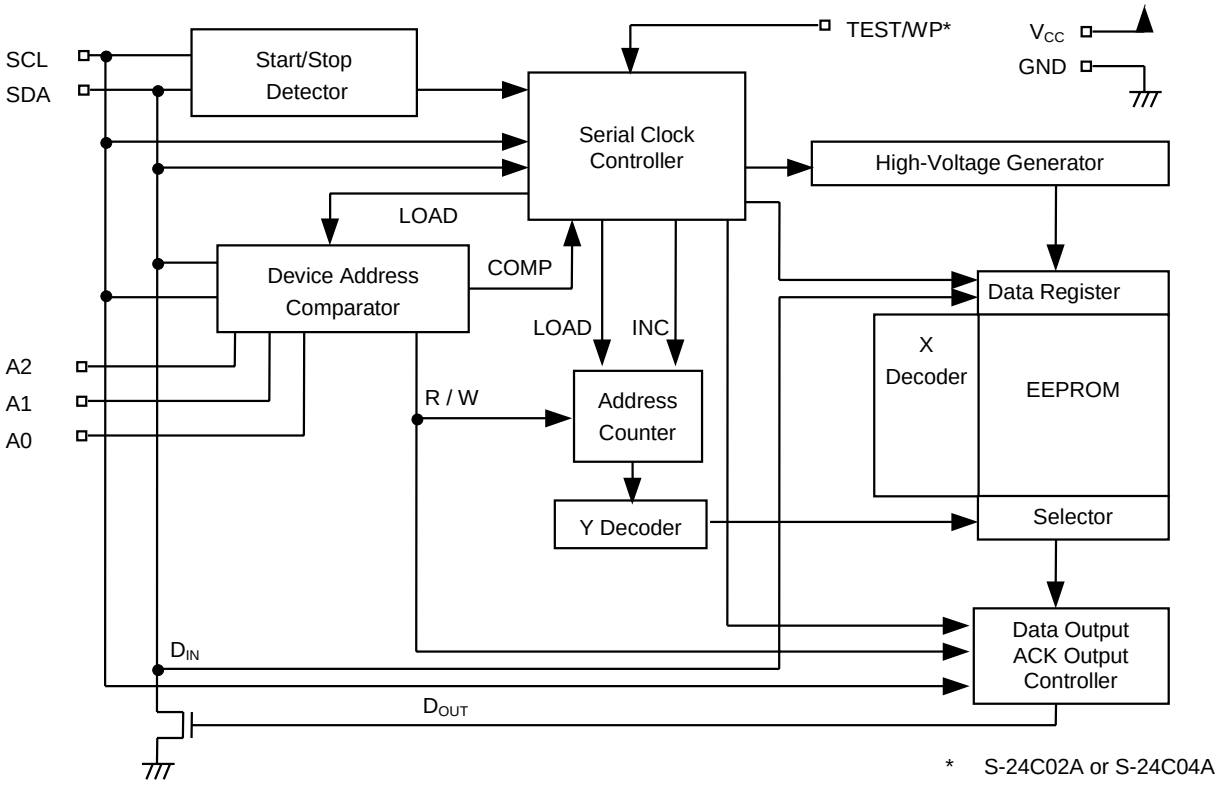


Figure 2

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	-50 to +95	°C
Storage temperature	T_{stg}	-65 to +150	°C

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation	1.8	—	5.5	V
		Write Operation	2.5	—	5.5	V
High level input voltage	V_{IH}	V_{CC}=2.5 to 5.5V	0.7×V_{CC}	—	V_{CC}	V
		V_{CC}=1.8 to 2.5V	0.8×V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC}=2.5 to 5.5V	0.0	—	0.3×V_{CC}	V
		V_{CC}=1.8 to 2.5V	0.0	—	0.2×V_{CC}	V
Operating temperature	T_{opr}	—	-40	—	+85	°C

■ Pin Capacitance

Table 4

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0 V (SCL, A0, A1, A2, WP)	—	—	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0 V (SDA)	—	—	10	pF

■ Endurance

Table 5

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^5	—	—	cycles/word

■ DC Electrical Characteristics

Table 6

Parameter	Symbol	Conditions	V_{CC}=4.5 V to 5.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	f=100 kHz	—	—	0.4	—	—	0.3	—	—	0.2	mA
Current consumption (PROGRAM)	I_{CC2}	f=100 kHz	—	—	2.0	—	—	1.5	—	—	—	mA

Table 7

Parameter	Symbol	Conditions	V_{CC}=4.5 V to 5.5 V			V_{CC}=2.5 to 4.5 V			V_{CC}=1.8 to 2.5 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN}=V_{CC} or GND	—	—	1.0	—	—	0.6	—	—	0.4	μA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V_{OL}	I_{OL}=3.2 mA	—	—	0.4	—	—	0.4	—	—	—	V
		I_{OL}=1.5 mA	—	—	0.3	—	—	0.3	—	—	0.5	V
		I_{OL}=100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
Current address retention voltage	V_{AH}	—	1.5	—	5.5	1.5	—	4.5	1.5	—	2.5	V

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$0.1\times V_{CC}$ to $0.9\times V_{CC}$
Input pulse rising/falling time	20 ns
Output judgment voltage	$0.5\times V_{CC}$
Output load	100 pF+ Pullup resistance 1.0 kΩ

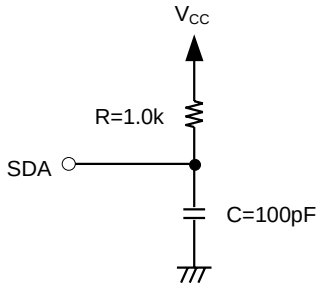


Figure 3 Output Load Circuit

Table 9

Parameter	Symbol	V_{CC}=1.8V to 5.5V			Unit
		Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	—	100	kHz
SCL clock time "L"	t_{LOW}	4.7	—	—	µs
SCL clock time"H"	t_{HIGH}	4.0	—	—	µs
SDA output delay time	t_{AA}	0.3	—	3.5	µs
SDA output hold time	t_{DH}	0.3	—	—	µs
Start condition setup time	$t_{SU.STA}$	4.7	—	—	µs
Start condition hold time	$t_{HD.STA}$	4.0	—	—	µs
Data input setup time	$t_{SU.DAT}$	50	—	—	ns
Data input hold time	$t_{HD.DAT}$	0	—	—	ns
Stop condition setup time	$t_{SU.STO}$	4.7	—	—	µs
SCL · SDA rising time	t_R	—	—	1.0	µs
SCL · SDA falling time	t_F	—	—	0.3	µs
Bus release time	t_{BUF}	4.7	—	—	µs
Noise suppression time	t_I	—	—	100	ns

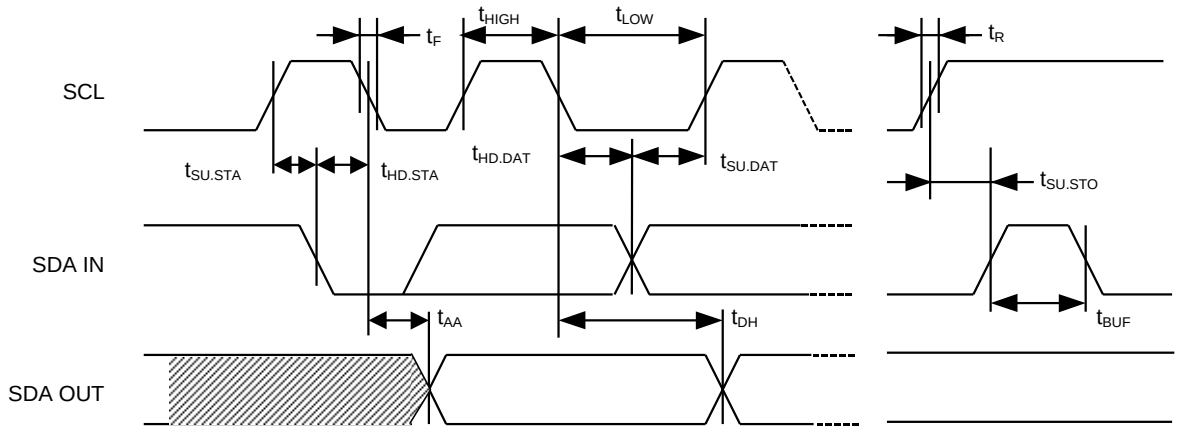


Figure 4 Bus Timing

Table 10

Item	Symbol	V_{CC}=4.5 to 5.5V			V_{CC}=2.5 to 4.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Write time	t_{WR}	—	0.8	1.0	—	4.0	5.0	ms

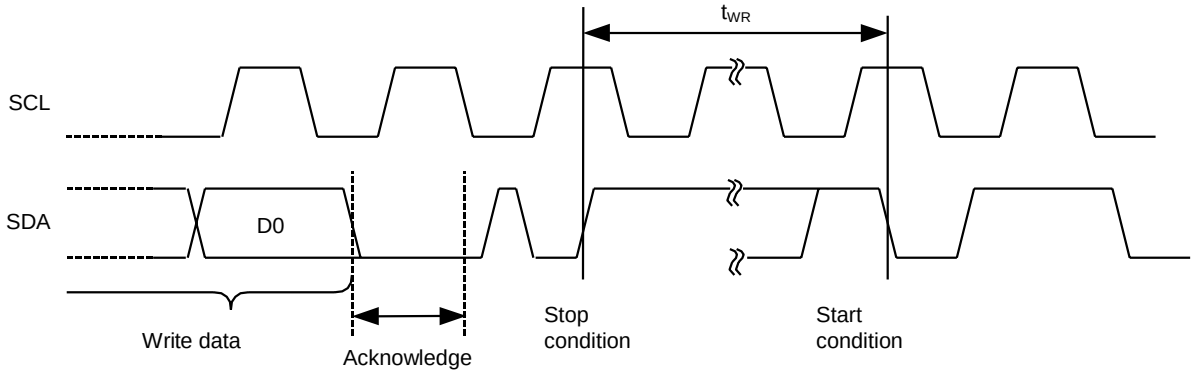


Figure 5 Write Cycle

■ Pin Functions

1. Address Input Pins (A0, A1, and A2)

Connect pins A0, A1, and A2 to the GND or the V_{CC}, respectively, to assign slave addresses. There are 8 different ways to assign slave addresses in the S-24C01A and S-24C02A through a combination of pins A0, A1, and A2, and 4 ways to assign them in the S-24C04A through a combination of pins A1 and A2. When the input slave address coincides with the slave address transmitted from the master device, 1 device can be selected from among multiple devices connected to the bus. Always connect the address input pin to GND or V_{CC} and leave it unchanged.

2. SDA (Serial Data Input/Output) Pin

The SDA pin is used for bilateral transmission of serial data. It consists of a signal input pin and an Nch open-drain transistor output pin.
Usually pull up the SDA line via resistance to the V_{CC}, and use it with other open-drain or open-collector output devices connected in a wired OR configuration.

3. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. It is capable of processing signals at the rising and falling edges of the SCL clock input signal. Make sure the rising time and falling time conform to the specifications.

4. TEST/WP Pin

The S-24C01A is not provided with a write protection (WP) function. The pin serves as the TEST pin. So, always connect the pin to the GND.
In the S-24C02A and S-24C04A, this pin is used for write protection. When there is no need for write protection, connect the pin to the GND; when there is a need for write protection, connect the pin to the Vcc.

■ Operation

1. Start Condition

When the SCL line is "H," the SDA line changes from "H" to "L." This allows the device to go to the start condition.
All operations begin from the start condition.

2. Stop Condition

When the SCL line is "H," the SDA line changes from "L" to "H." This allows the device to go to the stop condition.
When the device receives the stop condition signal during a read sequence, the read operation is interrupted, and the device goes to standby mode.
When the device receives the stop condition signal during write sequence, the retrieval of write data is halted, and the EEPROM initiates rewrite.

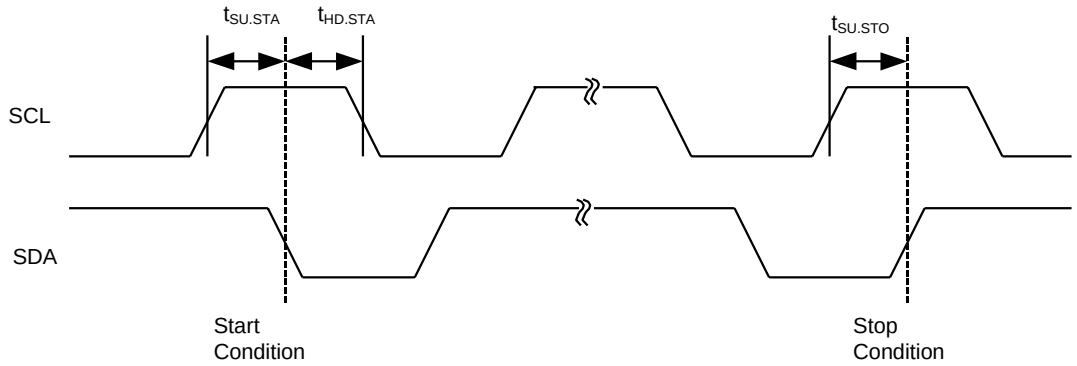


Figure 6 Start/Stop Conditions

3. Data Transmission

Changing the SDA line while the SCL line is "L" allows the data to be transmitted. A start or stop condition is recognized when the SDA line changes while the SCL line is "H."

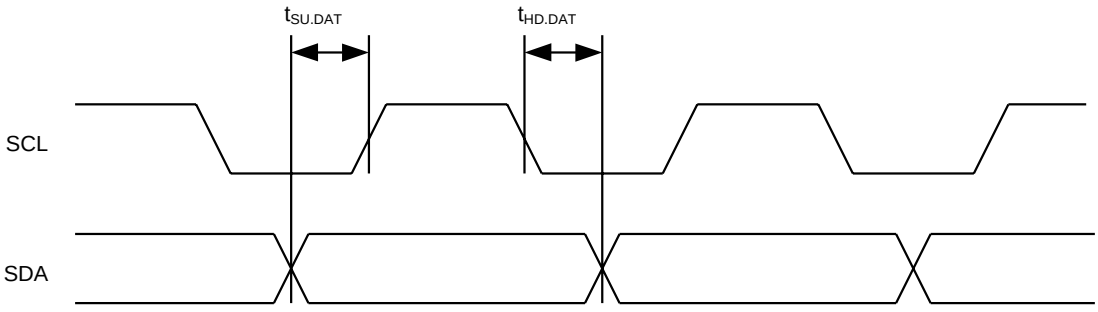


Figure 7 Data Transmission Timing

4. Acknowledgment

The unit of data transmission is 8 bits. By turning the SDA line "L," the slave device mounted on the system bus which receives the data during the 9th clock cycle outputs the acknowledgment signal verifying the data reception.

When the EEPROM is rewriting, the device does not output the acknowledgment signal.

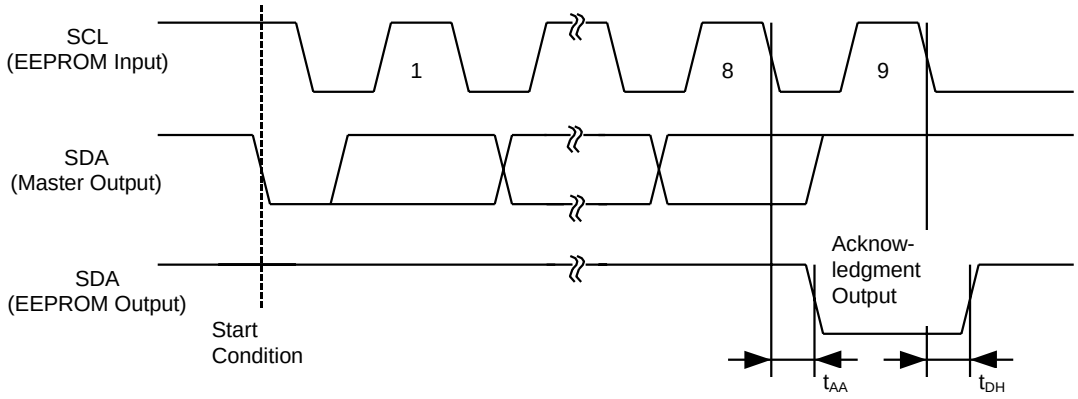


Figure 8 Acknowledgment Output Timing

5. Device Addressing

To perform data communications, the master device mounted on the system outputs the start condition signal to the slave device. Next, the master device outputs 7-bit length device address and a 1-bit length read/write instruction code onto the SDA bus.

Upper 4 bits of the device address are called the "Device Code," and set to "1010." Successive 3 bits are called the "Slave Address." It is used to select a device on the system bus, and compared to the predetermined address value at the address input pin (A2, A1, or A0).

When the comparison results match, the slave device outputs the acknowledgment signal during the 9th clock cycle.

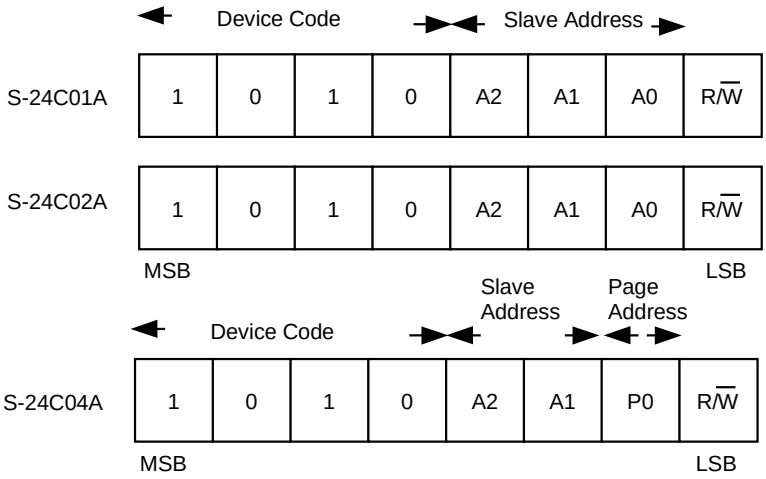


Figure 9 Device Address

In the S-24C04A, "A0" does not exist in the slave addresses. So, "A0" becomes "P0." "P0" is a page address bit and is equivalent to an additional uppermost bit of the word address. Accordingly, when P0="0," the former half area corresponding to 2 kbits (addresses from 000h to 0FFh) in the entire memory are selected; when P0="1," the latter half area corresponding to 2 kbits (addresses from 100h to 1FFh) in all areas of the memory are selected.

6. Write

6.1 Byte Write

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code "0," following the start condition signal, it outputs the acknowledgment signal. Next, when the EEPROM receives an 8-bit length word address, it outputs the acknowledgment signal.
After the EEPROM receives 8-bit write data and outputs the acknowledgment signal, it receives the stop condition signal. Next, the EEPROM at the specified memory address starts to rewrite.

When the EEPROM is rewriting, all operations are prohibited and the acknowledgment signal is not output.

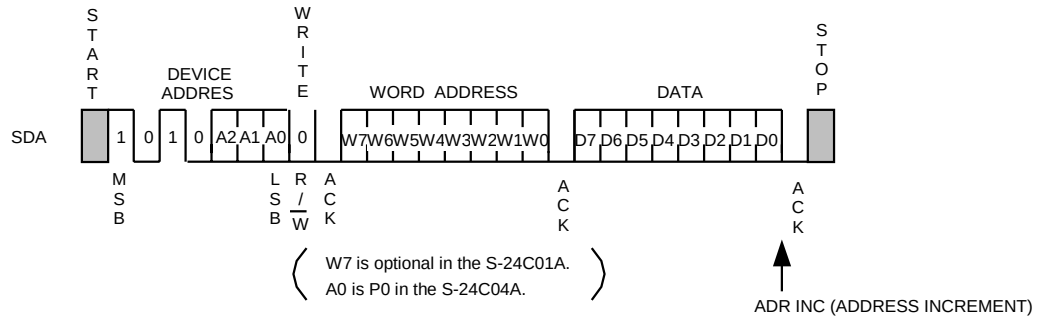


Figure 10 Byte Write

6.2 Page Write

Up to 8 bytes per page can be written in the S-24C01A and S-24C02A.
Up to 16 bytes per page can be written in the S-24C04A.

Basic data transmission procedures are the same as those in the "Byte Write." However, when the EEPROM receives 8-bit write data which corresponds to the page size, the page can be written.

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code "0," following the start condition signal, it outputs the acknowledgment signal. When the EEPROM receives an 8-bit length word address, it outputs the acknowledgment signal.

After the EEPROM receives 8-bit write data and outputs the acknowledgment signal, it receives 8-bit write data corresponding to the next word address, and outputs the acknowledgment signal. The EEPROM repeats reception of 8-bit write data and output of the acknowledgment signal in succession. It is capable of receiving write data corresponding to the maximum page size.

When the EEPROM receives the stop condition signal, it starts to rewrite, corresponding to the size of the page, on which write data, starting from the specified memory address, is received.

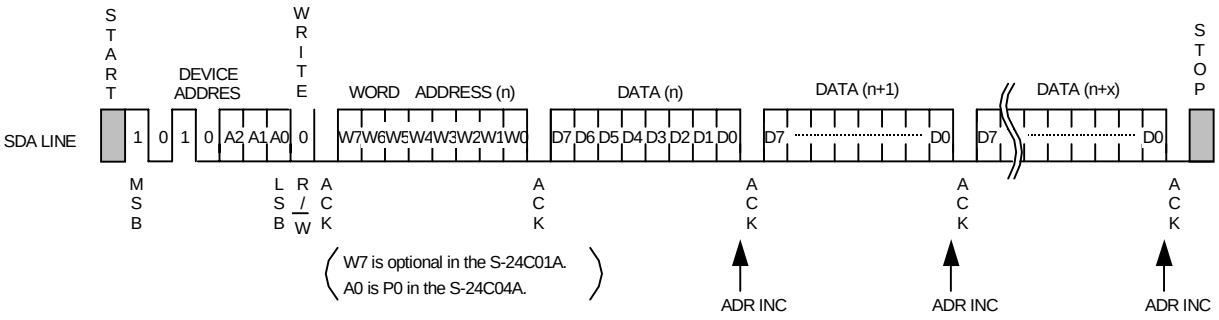


Figure 11 Page Write

In the S-24C01A or S-24C02A, the lower 3 bits of the word address are automatically incremented each when the EEPROM receives 8-bit write data.
Even if the write data exceeds 8 bytes, the upper 5 bits at the word address remain unchanged, the lower 3 bits are rolled over and overwritten.

In the S-24C04A, the lower 4 bits at the word address are automatically incremented each when the EEPROM receives 8 bit write data.
Even when the write data exceeds 16 bytes, the upper 4 bits of the word address and page address P0 remain unchanged, and the lower 4 bits are rolled over and overwritten.

6.3 Acknowledgment Polling

Acknowledgment polling is used to know when the rewriting of the EEPROM is finished.
After the EEPROM receives the stop condition signal and once it starts to rewrite, all operations are prohibited. Also, the EEPROM cannot respond to the signal transmitted by the master device. Accordingly, the master device transmits the start condition signal and the device address read/write instruction code to the EEPROM (namely, the slave device) to detect the response of the slave device. This allows users to know when the rewriting of the EEPROM is finished.

That is, if the slave device does not output the acknowledgment signal, it means that the EEPROM is rewriting; when the slave device outputs the acknowledgment signal, you can know that rewriting has been completed. It is recommended to use read instruction "1" for the read/write instruction code transmitted by the master device.

6.4 Write Protection

The S-24C02A and the S-24C04A are capable of protecting the memory. When the WP pin is connected to V_{CC}, writing to 50% of the latter half of all memory area (080h to 0FFh in the S-24C02A; 100h to 1FFh in the S-24C04A) is prohibited. Even when writing is prohibited, since the controller inside the IC is operating, the response to the signal transmitted by the master device is not available during the time of writing (t_{WR}).
When the WP pin is connected to GND, the write protection becomes invalid, and writing in all memory area becomes available. However, when there is no need for using write protection, always connect the WP pin to GND.

7. Read

7.1 Current Address Read

The EEPROM is capable of storing the last accessed memory address during both writing and reading. The memory address is stored as long as the power voltage is more than the retention voltage V_{AH}.
Accordingly, when the master device recognizes the position of the address pointer inside the EEPROM, data can be read from the memory address of the current address pointer without assigning a word address. This is called "Current Address Read."

"Current Address Read" is explained for when the address counter inside the EEPROM is an "n" address.
When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code "1," following the start condition signal, it outputs the acknowledgment signal. However, in the S-24C04A, page address P0 becomes invalid, and the memory address of the current address pointer becomes valid.
Next, 8-bit length data at an "n" address is output from the EEPROM, in synchronization with the SCL clock.
The address counter is incremented at the falling edge of the SCL clock by which the 8th bit of data is output, and the address counter goes to address n+1.

The master device does not output the acknowledgment signal and transmits the stop condition signal to finish reading.

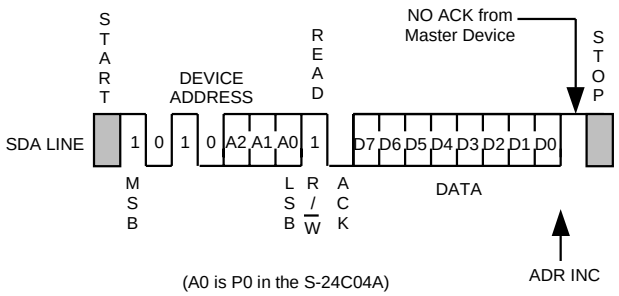


Figure 12 Current Address Read

For recognition of the address pointer inside the EEPROM, take into consideration the following:
The memory address counter inside the EEPROM is automatically incremented for every falling edge of the SCL clock by which the 8th bit of data is output during the time of reading. During the time of writing, upper bits of the memory address (upper 5 bits of the word address in the S-24C01A and S-24C02A; upper 4 bits of the word address and page address P0 in the S-24C04A) are left unchanged and are not incremented.

7.2 Random Read

Random read is a mode used when the data is read from arbitrary memory addresses. To load a memory address into the address counter inside the EEPROM, first perform a dummy write according to the following procedures:

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code "0," following the start condition signal, it outputs the acknowledgment signal.

Next, the EEPROM receives an 8-bit length word address and outputs the acknowledgment signal. Last, the memory address is loaded into the address counter of the EEPROM.
the EEPROM receives the write data during byte or page writing. However, data reception is not performed during dummy write.

The memory address is loaded into the memory address counter inside the EEPROM during dummy write. After that, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition signal and performing the same operation as that in the "Current Read."

That is, when the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code "1," following the start condition signal, it outputs the acknowledgment signal.
Next, 8-bit length data is output from the EEPROM, in synchronization with the SCL clock. The master device does not output an acknowledgment signal and transmits the stop condition signal to finish reading.

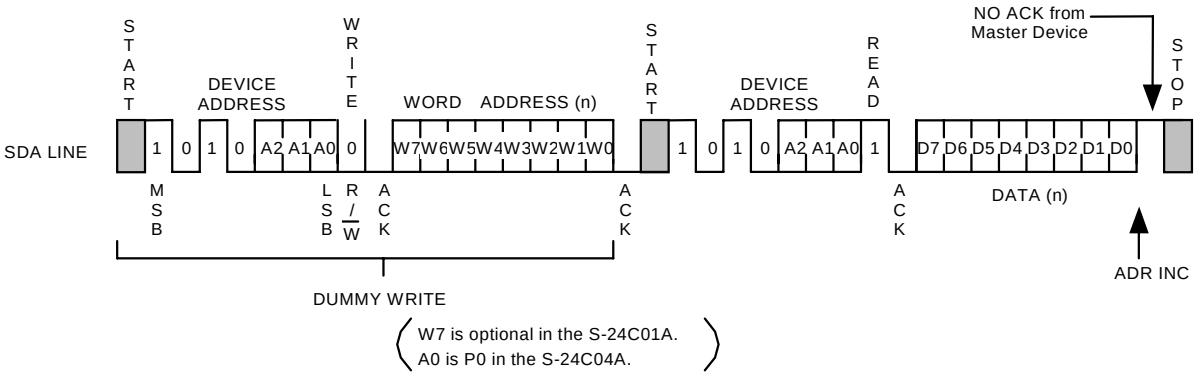


Figure 13 Random Read

7.3 Sequential Read

When the EEPROM receives a 7-bit length device address and a 1-bit read/write instruction code "1" in both current and random read operations, following the start condition signal, it outputs the acknowledgment signal

When 8-bit length data is output from the EEPROM, in synchronization with the SCL clock, the memory address counter inside the EEPROM is automatically incremented at the falling edge of the SCL clock, by which the 8th data is output.

When the master device transmits the acknowledgment signal, the next memory address data is output.

When the master device transmits the acknowledgment signal, the memory address counter inside the EEPROM is incremented and read data in succession. This is called "Sequential Read."

When the master device does not output an acknowledgement signal and transmits the stop condition signal, the read operation is finished.

Data can be read in the "Sequential Read" mode in succession. When the memory address counter reaches the last word address, it rolls over to the first memory address.

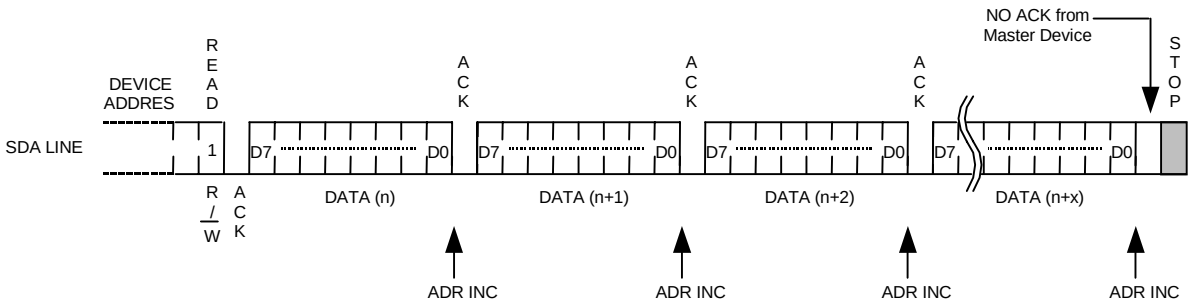


Figure 14 Sequential Read

8. Address Increment Timing

The address increment timing is as follows. See Figures 15 and 16. During reading operation, the memory address counter is automatically incremented at the falling edge of the SCL clock (the 8th read data is output).

During writing operation, the memory address counter is also automatically incremented at the falling edge of the SCL clock when the 8th bit write data is fetched.

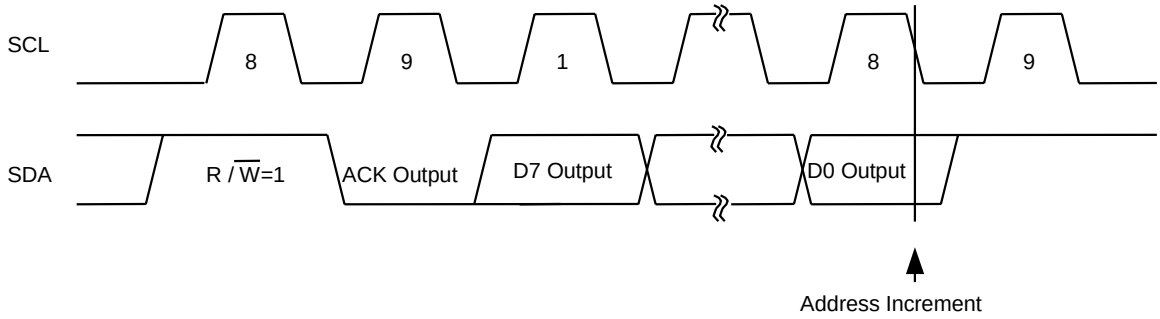


Figure 15 Address Increment Timing During Reading

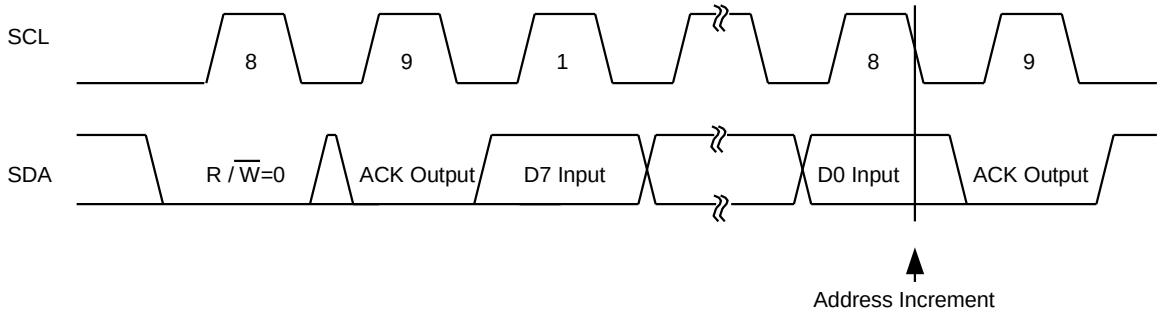


Figure 16 Address Increment Timing During Writing

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Please note that any product or system incorporating this IC may infringe upon the Philips I^2C Bus Patent Rights depending upon its configuration.
In the event that such product or system incorporating the I^2C Bus infringes upon the Philips Patent Rights, Seiko Instruments Inc. shall not bear any responsibility for any matters with regard to and arising from such patent infringement.

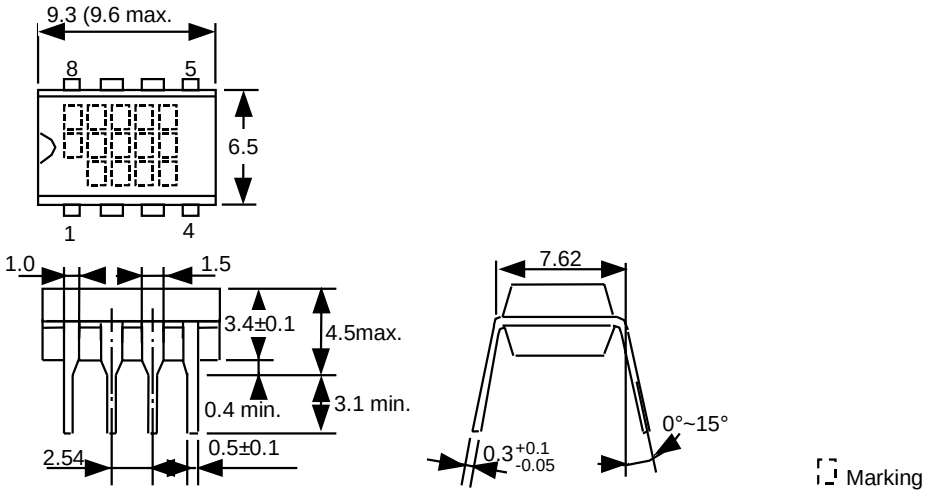
■ Physical Dimensions (Unit: mm)

1. 8-pin DIP

There are two types of packages : A or B.

A type

S-24C01ADPA-01
S-24C02ADPA-01
S-24C04ADPA-01



B type

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S-24C02ADP-01
S-24C04ADP-01

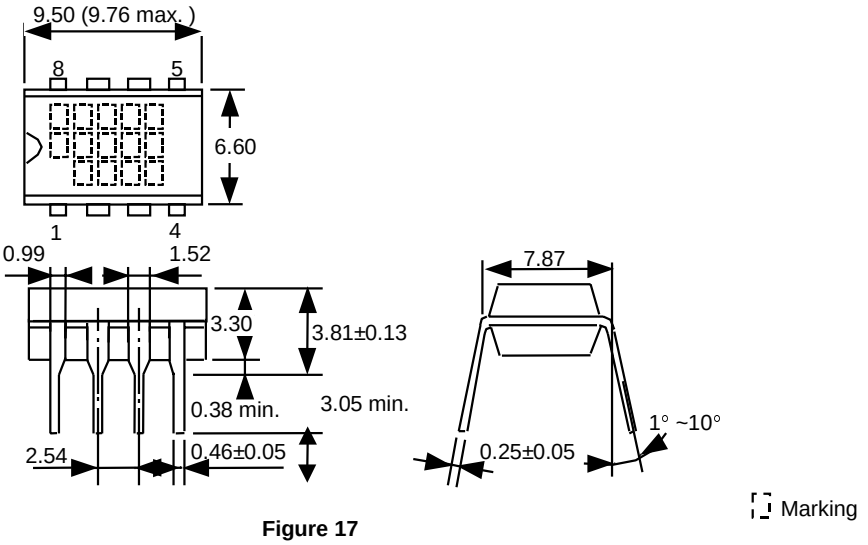


Figure 17

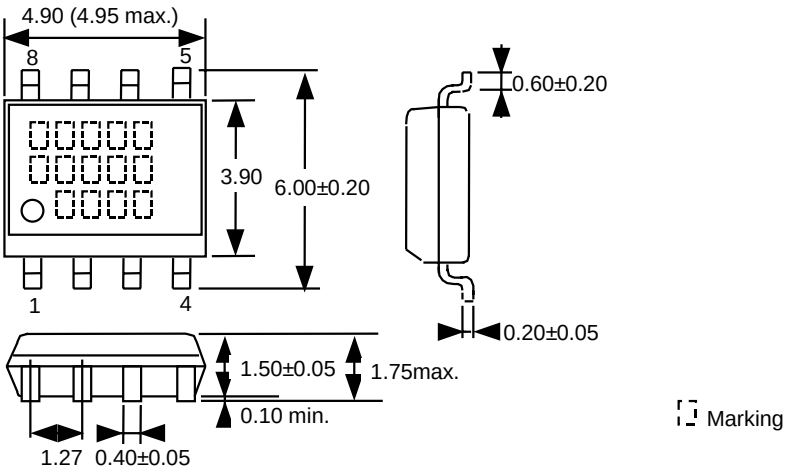
2. 8-pin SOP

There are two types of packages : A or B.

A type

S-24C01AFJA-χχ-01
S-24C02AFJA-χχ-01
S-24C04AFJA-χχ-01

* χχ differs depending on the packing form.
TB : Tape
(blank) : Magazine



B type

S-24C01AFJ-χχ-01
S-24C02AFJ-χχ-01
S-24C04AFJ-χχ-01

* χχ differs depending on the packing form.
TB : Tape
(blank) : Magazine

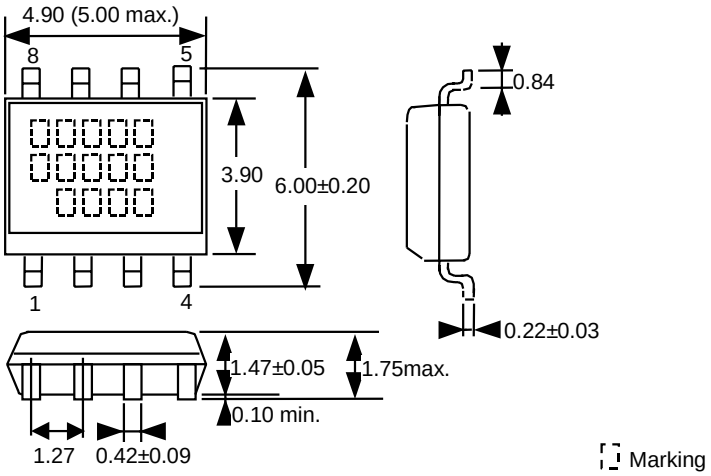


Figure 18

■ Ordering Information

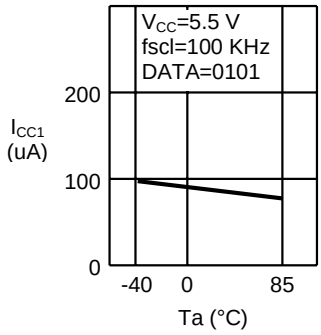
S-24C0XA XX X-χχ-01

Packing form	TB	:	Tape (SOP only)
	(blank)	:	Magazine
Package type	A	:	A type
	(blank)	:	B type
Package	DP	:	DIP
	FJ	:	SOP
Name of Product	S-24C01A	:	1 kbits
	S-24C02A	:	2 kbits
	S-24C04A	:	4 kbits

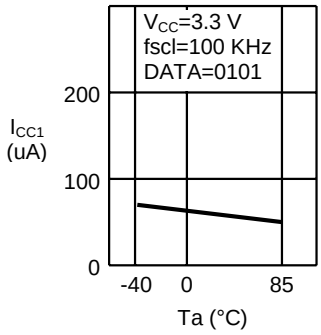
■ Characteristics

1. DC Characteristics

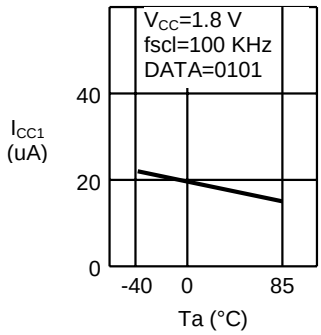
1.1 Current consumption (READ) I_{CC1} — Ambient temperature Ta



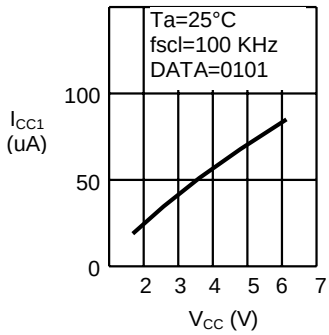
1.2 Current consumption (READ) I_{CC1} — Ambient temperature Ta



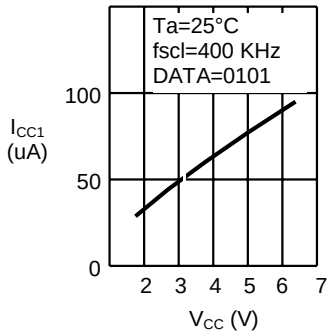
1.3 Current consumption (READ) I_{CC1} — Ambient temperature Ta



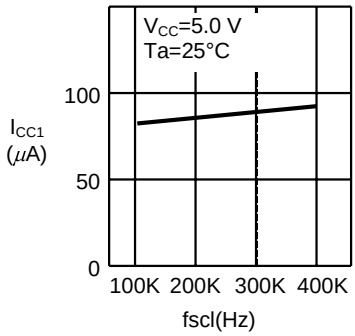
1.4 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



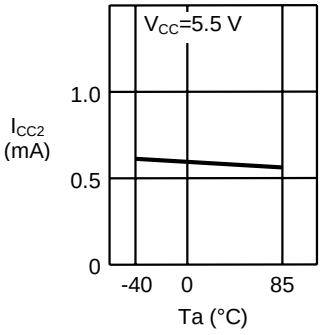
1.5 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



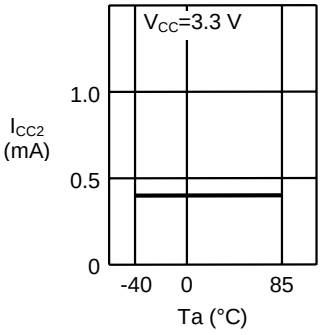
1.6 Current consumption (READ) I_{CC1} – Clock frequency fscl



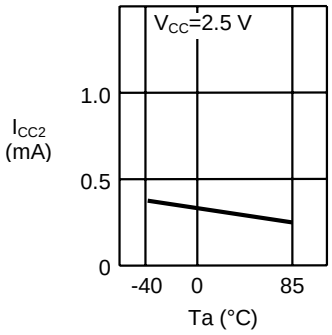
1.7 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



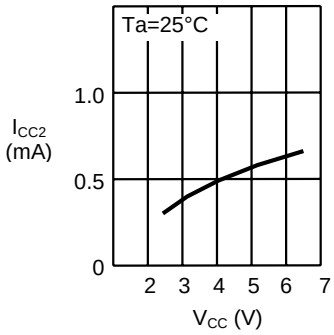
1.8 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



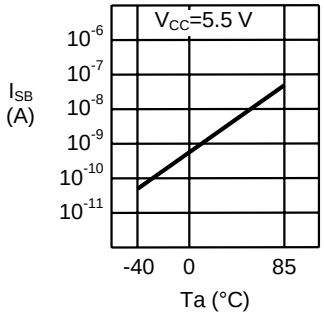
1.9 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



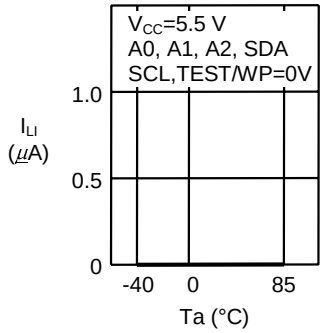
1.10 Current consumption (PROGRAM) I_{CC2} – Power supply voltage V_{CC}



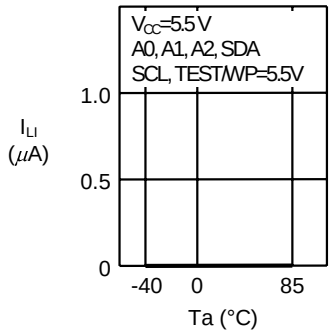
1.11 Standby current consumption I_{SB} — Ambient temperature Ta



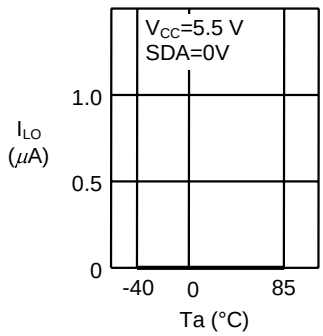
1.12 Input leakage current I_{LI} – Ambient temperature Ta



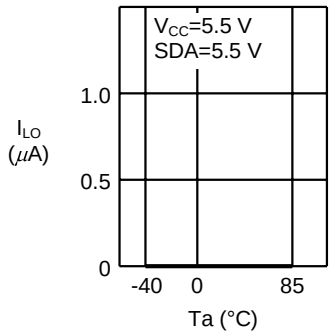
1.13 Input leakage current I_{LI} – Ambient temperature Ta



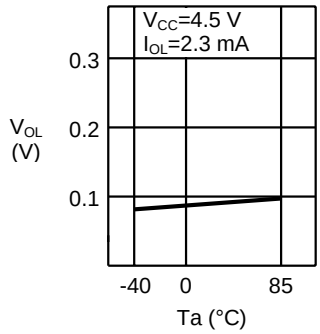
1.14 Output leakage current I_{LO} – Ambient temperature Ta



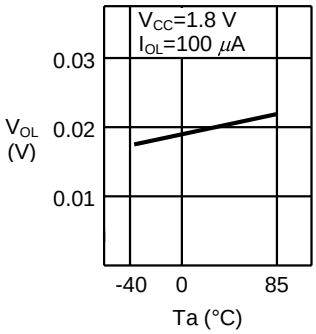
1.15 Output leakage current I_{LO} – Ambient temperature Ta



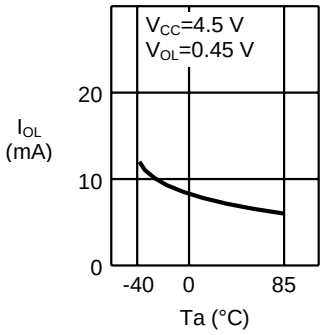
1.16 Low level output voltage V_{OL} – Ambient temperature Ta



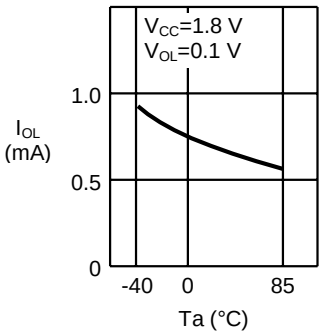
1.17 Low level output voltage V_{OL} – Ambient temperature Ta



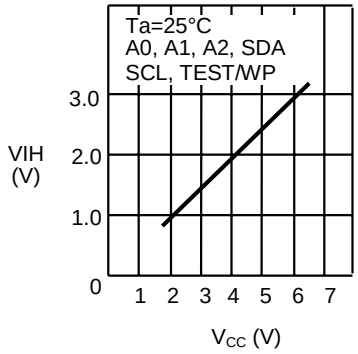
1.18 Low level output current I_{OL} – Ambient temperature Ta



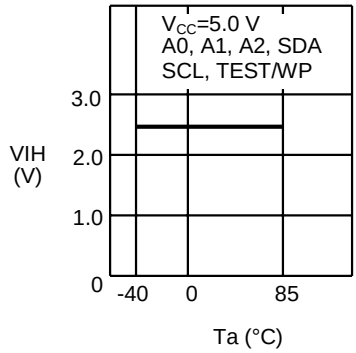
1.19 Low level output current I_{OL} – Ambient temperature Ta



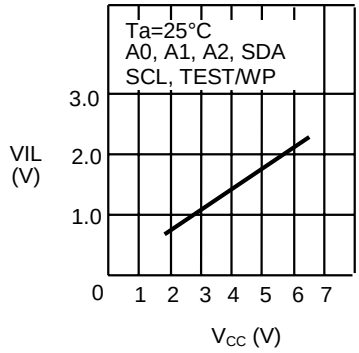
1.20 High input inversion voltage VIH – Power supply voltageV_{CC}



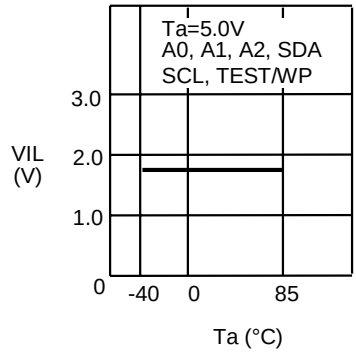
1.21 High input inversion voltage VIH – Ambient temperature Ta



1.22 Low input inversion voltage VIL – Power supply voltageV_{CC}

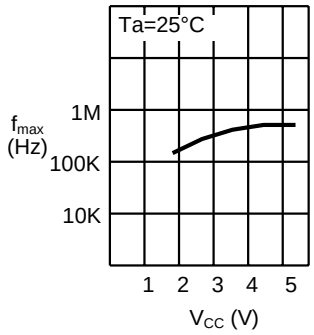


1.23 Low input inversion voltage VIL – Ambient temperature Ta

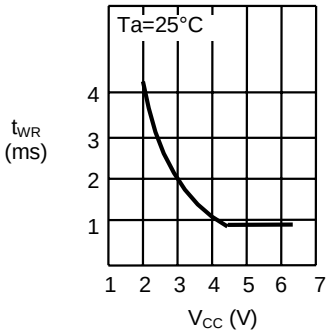


2. AC Characteristics

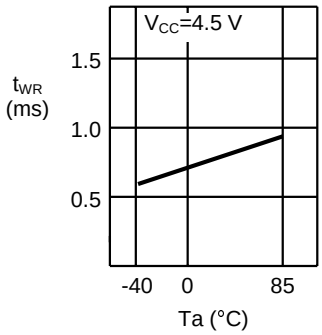
2.1 Maximum operating frequency fmax – Power supply voltage V_{CC}



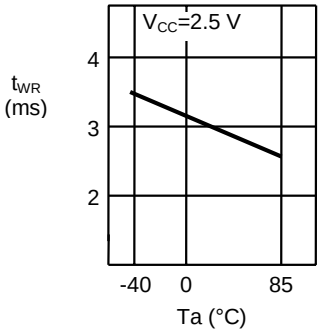
2.2 Write time t_{WR} – Power supply voltage V_{CC}



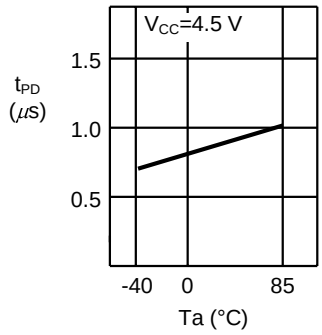
2.3 Write time t_{WR} – Ambient temperature Ta



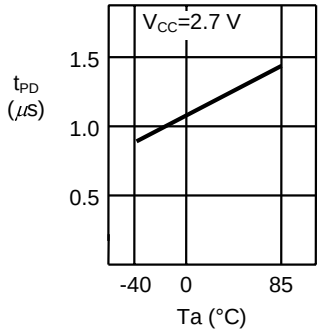
2.4 Write time t_{WR} – Ambient temperature Ta



2.5 SDA output delay time t_{PD} – Ambient temperature Ta



2.6 SDA output delay time t_{PD} – Ambient temperature Ta



2.7 Data output delay time t_{PD} – Ambient temperature Ta