ICs for Communications

PMB 2408 V1.1
Wideband-Receiver

Data Sheet 5.99

Contents

0	Revision History		3
1	General Overview		4
	1.1	Features	4
	1.2	Applications	4
	1.3	Functional Description	4
2	Pinning		5
	2.1	Pin Description	5
	2.2	Pin Configuration	6
	2.3	Package Outline	6
3	Functional Block Diagram		7
4	Circuit Description		8
5	Internal Input/Output circuits		12
6	Electrical Characteristics		14
	6.1	Absolut Maximum Ratings	14
	6.2	Operational Range	15
	6.3	AC/DC Characteristics	16
7	Test Circuits		25
	7.1	Test Circuit 1	25
	7.2	Test Circuit 1.1	26
	7.3	Test Circuit 1.2	26
	7.4	Test Circuit 2	27
	7.5	Test Board	28
8	Design Hints		
	8.1	LNA Matching for 925 MHz	35
	8.2	VCO: Possibility of I/Q phase error correction	36
	8.3	Sample and Hold: Offset compensation diagram for smallband applications	37
	8.4	Sample and Hold: Offset compensation diagram for wideband applications	38
9	Diagrams		39

0 Revision History

#	Subjekt	Data sheet 5/99		Data sheet		Change
		Page	Item	Page	Item	

1 General Overview

1.1 Features

- Heterodyne receiver with demodulator
- On-chip low noise amplifier (LNA), gain switchable
- Switchable (on / off) reference voltage for biasing either the internal LNA or an external LNA
- Demodulation and generation of I/Q components
- Low mixer noise 9dB (SSB)
- High input intercept point +2dB
- Integrated phase shifter
- IF amplifier with 80dB programmable gain control (PGC) in steps of 2dB
- Active part of a local-oscillator (LO2) with external tuning circuit or possibility to use it as amplifier
- Two differential operational amplifiers for use as base-band amplifier in smallband applications
- Low power consumption due to highly flexible power down capability
- Wide input frequency range up to 2.5 GHz
- Wide IF range from 40 MHz to 460 MHz
- Channel bandwidth (baseband bandwidth) up to 5 MHz (VS = 2.7V)
- Low Supply Voltage down to 2.7V
- P-TQFP-48 package
- Temperature range -40° to 85°C

1.2 Applications

- Vector modulated digital mobile cellular systems as WLAN etc.
- Various demodulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK
- Space and power saving optimisations of existing discrete demodulator circuits

1.3 Functional Description

The PMB 2408 is a single-chip double-conversion heterodyne receiver with LO-phase shifting circuitry for the I/Q-Phase demodulation on chip. It also includes a low noise amplifier with switchable gain, a switchable reference voltage for biasing either the internal or an external LNA, the second local oscillator with a VCO output buffer, a programmable gain controlled IF amplifier, two differential operational amplifiers for base band purposes in smallband applications, and a power down circuitry.

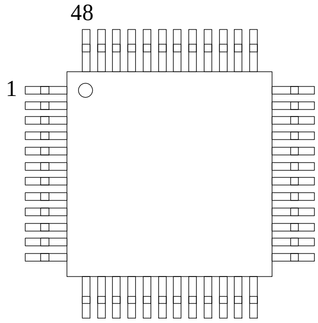
The PMB 2408 is designed for vector modulated digital systems like WLAN with larger channel bandwidth.

2 Pinning

2.1 Pin Description

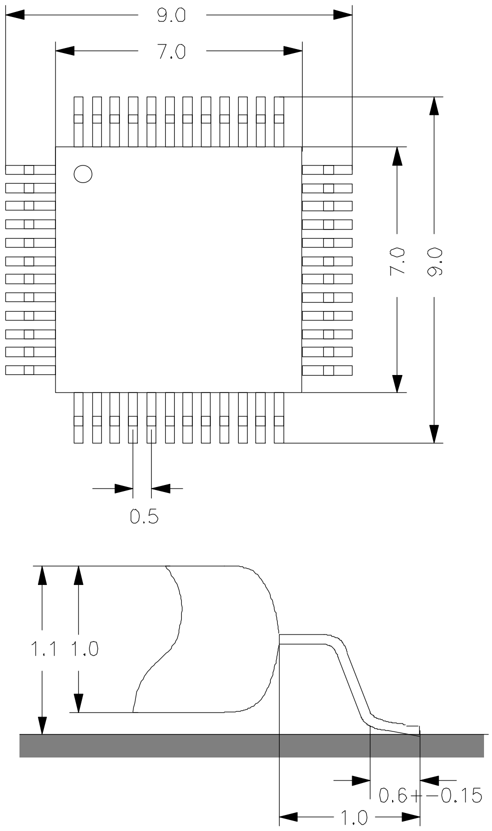
Pin No.	Symbol	Function
1	VS2	Supply voltage 2 (IF circuit part, Op. Amp, 3-wire bus, offset compensation)
2	DIV1/3	Divider-logic input
3, 6, 16, 22, 30	GND	Ground
4	CSH1	Sample and hold capacitance 1
5	CSH2	Sample and hold capacitance 2
7	OCE	Sample and hold input
8	IFI	Non-inverting IF input
9	IFIX	Inverting IF input
10	SYGCDT	Data input (3 wire bus of PGC)
11	SYGCCL	Clock input (3 wire bus of PGC)
12	PGCSTR	Enable input (3 wire bus of PGC)
13	SIX	Inverted signal input of first mixer
14	SI	Non-inverted signal input of first mixer
15	RXON1	Power down input 1 (RF)
17	LO1X	Inverting input for first local oscillator
18	LO1	Non-inverting input for first local oscillator
19	VS1	Supply voltage 1 (First mixer, bias for LNA)
20	MO	Non-inverted output of first mixer
21	MOX	Inverted output of first mixer
23	LO2OX	Inverted VCO output buffer
24	LO2O	Non-inverted VCO output buffer
25	GND3	Ground3 (LNA ground)
26	AO	LNA output
27	VS3	Supply voltage 3 (LNA)
28	AREF	LNA reference input
29	AI	LNA input
31	PUPLO2	Power up input for VCO and VCO output buffer
32	LO2X	Base inverting input for second local oscillator
33	LO2EX	Emitter inverting input for second local oscillator
34	LO2E	Emitter non-inverting input for second local oscillator
35	LO2	Base non-inverting input for second local oscillator
36	RXON2	Power down input 2 for the IF-part and Op. Amp.'s
37	SOQX	Inverting quadratur demodulator signal output
38	FBQ	Feedback tap for “fixed-gain” Op.-Amp.’s (Q)
39	QRX	Inverting op. amp. signal output (Q)
40	QR	Non-inverting op. amp. signal output (Q)
41	FBQX	Feedback tap for “fixed-gain” Op.-Amp.’s (Q)
42	SOQ	Non-inverting quadratur demodulator signal output
43	SOIX	Inverting in-phase demodulator signal output
44	FBI	Feedback tap for “fixed-gain” Op.-Amp.’s (I)
45	IRX	Inverting op. amp. signal output (I)
46	IR	Non-inverting op. amp. signal output (I)
47	FBIX	Feedback tap for “fixed-gain” Op.-Amp.’s (I)
48	SOI	Non-inverting in-phase demodulator signal output

2.2 **Pin Configuration** (top view)

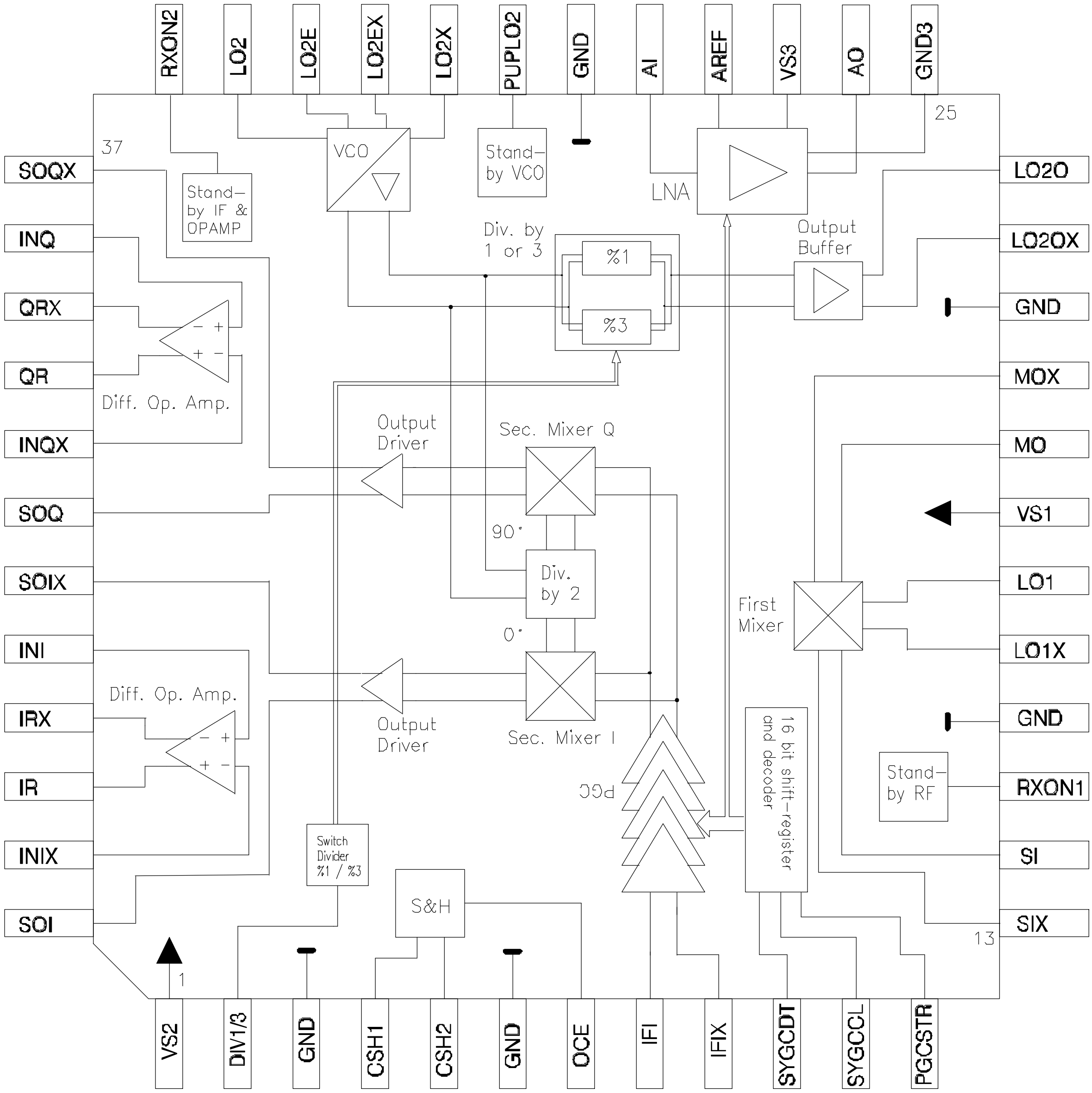


2.3 Package Outline

Quad Flat package
P-TQFP-48



3 Functional Block Diagram



4 Circuit Description

The input signal is amplified by the internal or an external LNA and filtered in an external Filter (LNA programming see table3). The filtered signal SI/SIX and the first local oscillator signal LO1/LO1X are mixed down to an intermediate frequency (IF). The open collector output of the mixer generates a differential current at pins MO/MOX which is filtered by an external LC tank circuit. An external SAW filter following this LC circuit is used for channel selection.
The amplification of the IF signal is performed by a digitally programmable gain-controlled amplifier. Gain programming is done by loading a 16 bit control word into a register via the 3 - wire bus (see Fig. 1 and 3 and also table 3 and 4). Serial data is clocked out from MSB to LSB. After power-down the information in the register is lost.
The second local oscillator signal LO2 is generated either by the active part of an on-chip oscillator (with external tuning circuit) or by an external VCO.
Depending on the logic level at pin DIV1/3 (see table 2), the internal LO2 signal is fed directly to the buffered output **(DIV1/3: L)** or to a divider by 3 **(DIV1/3: H)** and then to a buffered output and also to a divider, which generates orthogonal signals at half the VCO frequency. The filtered IF signal re-enters the chip at the IFI/IFIX input, where it is amplified and converted to the final output frequency with each of the orthogonal signals. The resulting in-phase and quadrature signals pass through differential output drivers and appear at SOI/SOIX and SOQ/SOQX outputs, respectively.
Two differential operational amplifiers with the input signals INI/INIX (INQ/INQX) and the output signals IR/IRX (QR/QRX) can be used as baseband amplifiers or active baseband filters in smallband applications (see design hint 8.3 page 37). At both outputs IR/IRX (QR/QRX) the differential offset is sensed via the sample and hold circuitry. A feedback loop corrects the remaining offset error below the tolerable input value of the baseband A/D converter. For wideband applications please refer to design hint 8.4 page 38.
Differential signals and symmetrical circuitry are used throughout. Bias drivers generate internal temperature- and supply voltage compensated reference voltages required by various circuit blocks. Switching the power down inputs RXON1,RXON2 and PUPLO2 from HIGH to LOW (see table 1 and Fig. 2.1) sets the circuit from its normal operating mode into a mode with reduced supply current. Fig. 2.2 shows the supply function.

There are three supply voltages: VS1 supplies the first mixer and the standby RF circuit, VS2 supplies the complete IF part and VS3 supplies the LNA. The LNA has an own ground pin GND3, the rest of the circuits are grounded by GND.

Figure 1: Block Diagram of PGC and 3 - wire bus

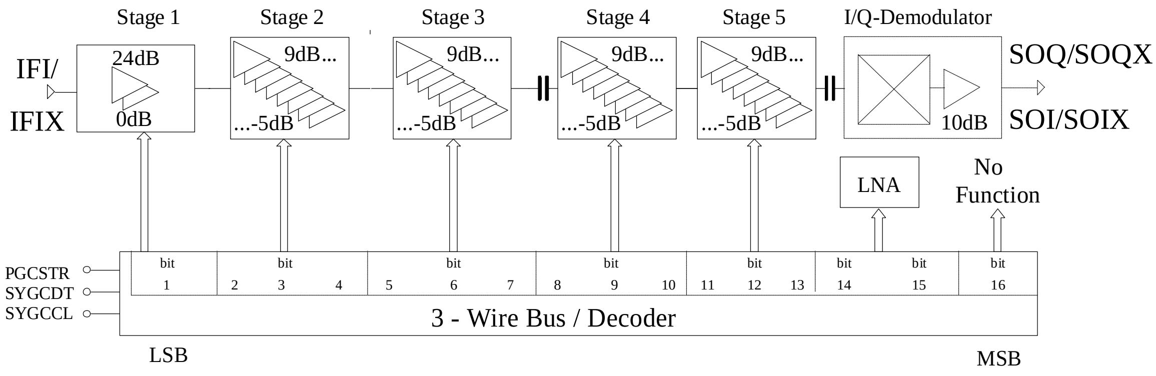


Figure 2: Power Down- and Supply-Function

Figure 2.1: Power Down Function

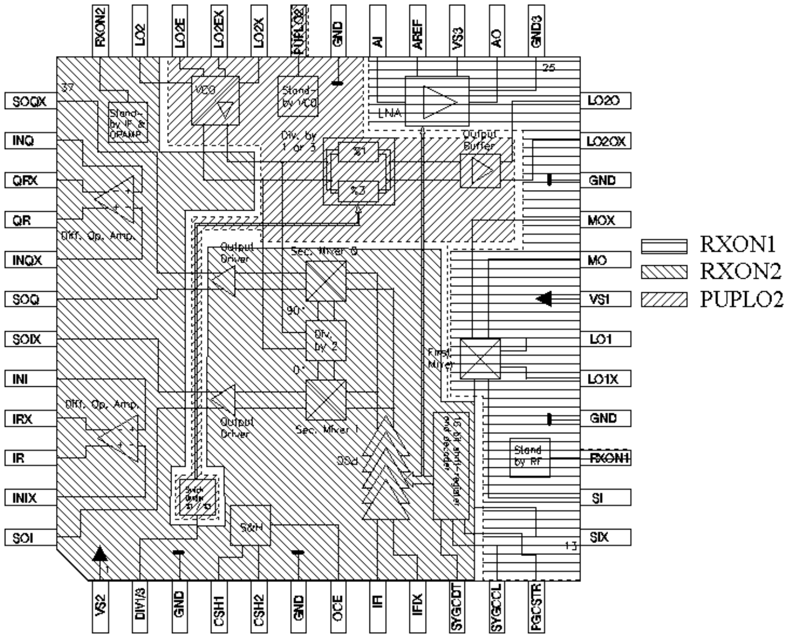


Figure 2.2: Supply Function

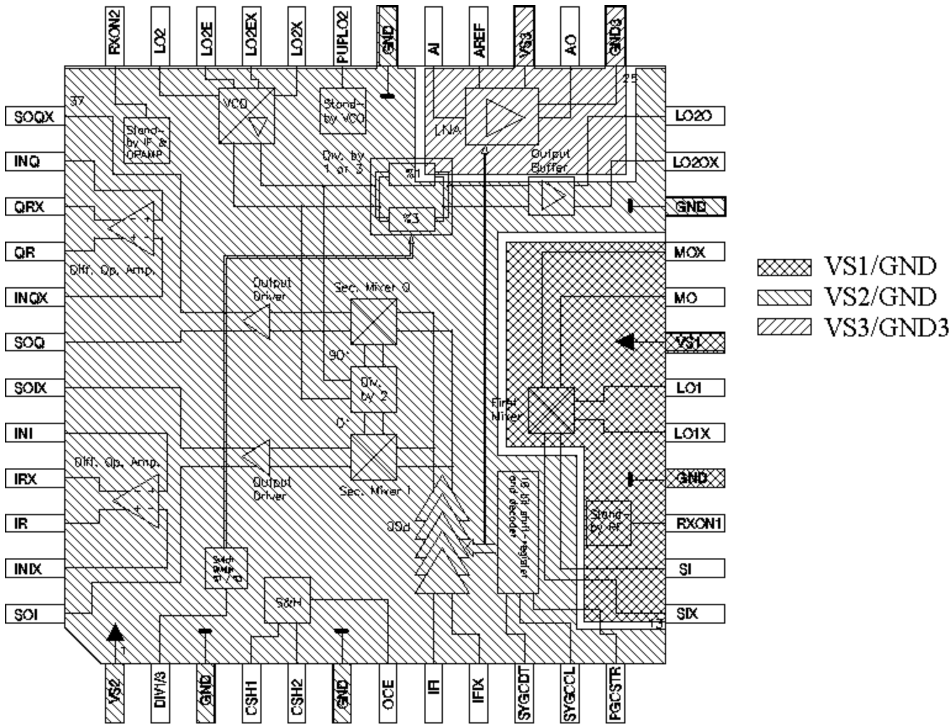


Figure 3: Three-wire bus timing diagram

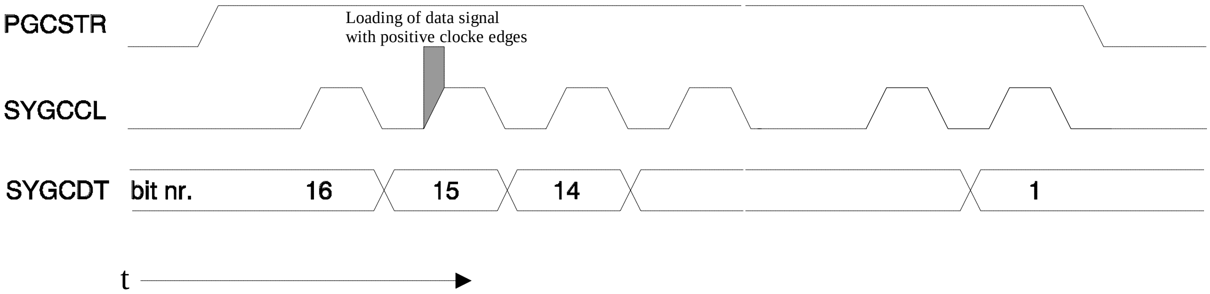


Table 1: Power Down Function

RXON1	RF Part
L	Off
H	On

RXON2	IF Part & Op.Amp.'s
L	Off
H	On

PUPLO2	VCO/Buffer Div. by 1 or 3
L	Off
H	On

The PGC adjustment is not stored during power down of RXON2.

Table 2: Divider DIV1/3: switch logic

DIV 1/3	Divider
L	%1
H	%3

Table 3: LNA gain control:

general			
Reference Voltage	Gain Control	bit 14 reference switch	bit 15 gain switch
Aref = on	H-gain	1	1
Aref = on	L-gain	1	0
Aref = off		0	X

	as LNA	
	bit 14	bit15
H-gain	1	1
L-gain	1	0

	as switch	
	bit 14	bit 15
Aref=on	1	1
Aref=off	0	1

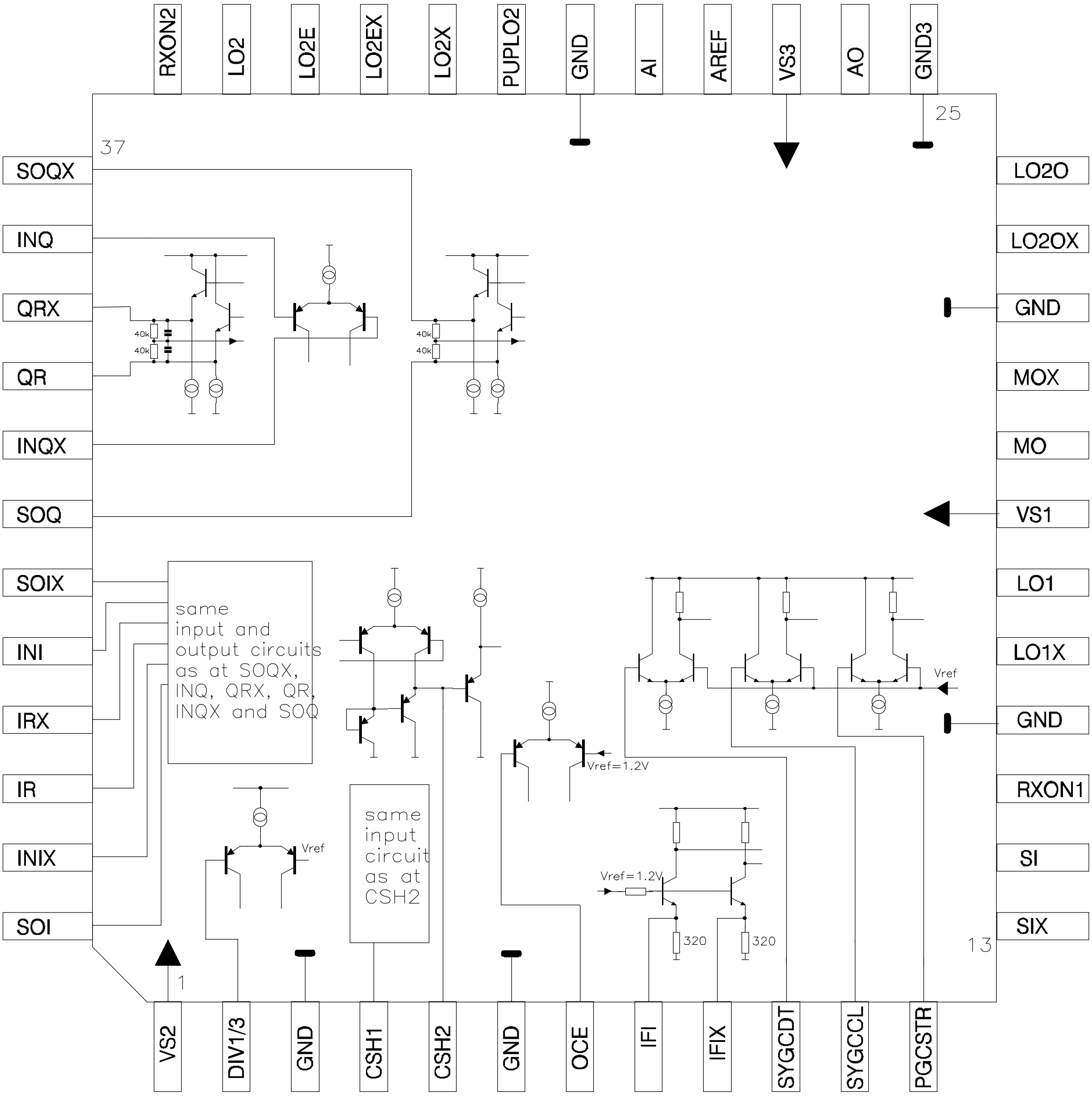
Table 4: Table of PGC-, LNA-Gain Control

G/dB	bit															
	PGC													LNA		no
	st. 1	stage 2			stage 3			stage 4			stage 5			Aref	gain	func-tion
PGC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
70	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X
68	1	1	1	0	1	1	1	1	1	1	1	1	1	X	X	X
66	1	1	0	1	1	1	1	1	1	1	1	1	1	X	X	X
64	1	1	0	0	1	1	1	1	1	1	1	1	1	X	X	X
62	1	0	1	1	1	1	1	1	1	1	1	1	1	X	X	X
60	1	0	1	0	1	1	1	1	1	1	1	1	1	X	X	X
58	1	0	0	1	1	1	1	1	1	1	1	1	1	X	X	X
56	1	0	0	0	1	1	1	1	1	1	1	1	1	X	X	X
54	1	0	0	0	1	1	0	1	1	1	1	1	1	X	X	X
52	1	0	0	0	1	0	1	1	1	1	1	1	1	X	X	X
50	1	0	0	0	1	0	0	1	1	1	1	1	1	X	X	X
48	1	0	0	0	0	1	1	1	1	1	1	1	1	X	X	X
46	1	0	0	0	0	1	0	1	1	1	1	1	1	X	X	X
44	1	0	0	0	0	0	1	1	1	1	1	1	1	X	X	X
42	1	0	0	0	0	0	0	1	1	1	1	1	1	X	X	X
40	0	1	0	0	1	1	1	1	1	1	1	1	1	X	X	X
38	0	0	1	1	1	1	1	1	1	1	1	1	1	X	X	X
36	0	0	1	0	1	1	1	1	1	1	1	1	1	X	X	X
34	0	0	0	1	1	1	1	1	1	1	1	1	1	X	X	X
32	0	0	0	0	1	1	1	1	1	1	1	1	1	X	X	X
30	0	0	0	0	1	1	0	1	1	1	1	1	1	X	X	X
28	0	0	0	0	1	0	1	1	1	1	1	1	1	X	X	X
26	0	0	0	0	1	0	0	1	1	1	1	1	1	X	X	X
24	0	0	0	0	0	1	1	1	1	1	1	1	1	X	X	X
22	0	0	0	0	0	1	0	1	1	1	1	1	1	X	X	X
20	0	0	0	0	0	0	1	1	1	1	1	1	1	X	X	X
18	0	0	0	0	0	0	0	1	1	1	1	1	1	X	X	X
16	0	0	0	0	0	0	0	1	1	0	1	1	1	X	X	X
14	0	0	0	0	0	0	0	1	0	1	1	1	1	X	X	X
12	0	0	0	0	0	0	0	1	0	0	1	1	1	X	X	X
10	0	0	0	0	0	0	0	0	1	1	1	1	1	X	X	X
8	0	0	0	0	0	0	0	0	1	0	1	1	1	X	X	X
6	0	0	0	0	0	0	0	0	0	1	1	1	1	X	X	X
4	0	0	0	0	0	0	0	0	0	0	1	1	1	X	X	X
2	0	0	0	0	0	0	0	0	0	0	1	1	0	X	X	X
0	0	0	0	0	0	0	0	0	0	0	1	0	1	X	X	X
-2	0	0	0	0	0	0	0	0	0	0	1	0	0	X	X	X
-4	0	0	0	0	0	0	0	0	0	0	0	1	1	X	X	X
-6	0	0	0	0	0	0	0	0	0	0	0	1	0	X	X	X
-8	0	0	0	0	0	0	0	0	0	0	0	0	1	X	X	X
-10	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X
G/dB	bit															
LNA	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
15	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X
-5	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X

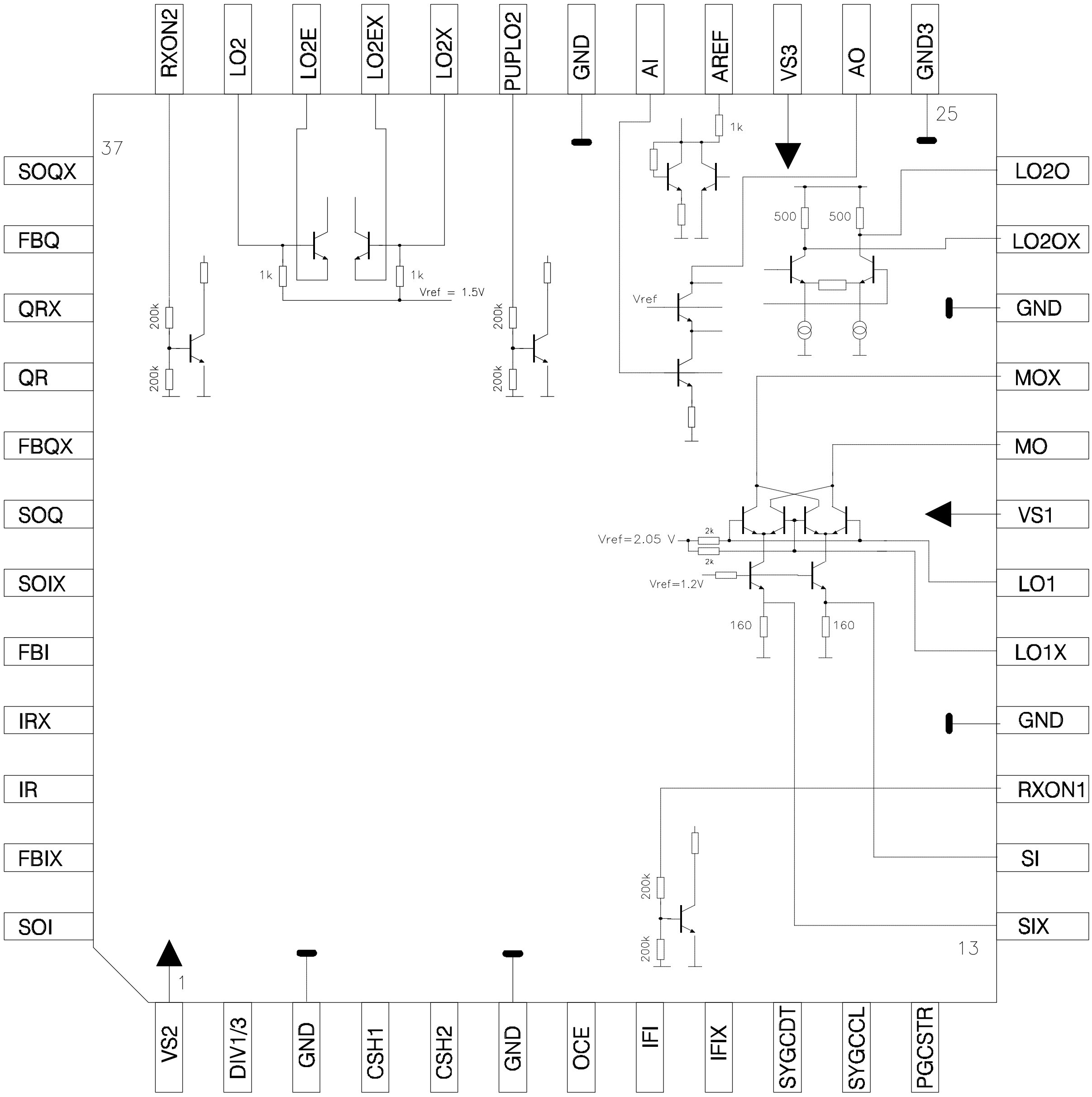
1 = High, 0 = Low, X = don't care

5 Internal Input/Output Circuits

Internal I/O Circuits from Pin 1 to 12 and 37 to 48



Internal I/O Circuits from Pin 13 to 36



6 Electrical Characteristics

6.1 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Ambient temperature T_A = -40° to 85°C

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
1	Supply Voltage	V_S	-0.3	5.5	V	
2	Input/Output Voltage Output Voltage Aref	V_{IO}	-0.3 0	VS + 0.3 2.5	V	Except LNA
3	Open Collector Output Voltage MO,MOX AO	V_{OC}	 1.7 1.0	 VS + 0.3 VS + 0.3	V	
4	LNA Input Voltage	V_{AI}	-3		V	RXON1=L
5	LNA Input Current	I_{AI}		10	mA	RXON1=L
6	Differential Input Voltage (any differential Input)	V_I		2	Vpp	

7	Junction Temperature	T_j		125	°C	
8	Storage Temperature	T_S	-55	125	°C	
9	Thermal Resistance (junction to ambient)	R_{thJA}		165	K/W	

10	ESD-integrity	V_{ESD}	1000	1000	V	according MIL-Std 883D, method 3015.7
The RF pins 20, 21, 26, 29, 32, 33, 34 and 35 are not protected against voltage stress > 300V (versus VS or GND). The high frequency performance prohibits the use of adequate protective structures.						

6.2 Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC characteristics limits are not guaranteed.

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = -40 to 85°C; refer to test circuit 1.

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
LNA						
1	AI Input Frequency	f_{SI}		2500	MHz	
First mixer						
2	SI/SIX Input Level	P_{SI}		-11	dBm	
3	SI/SIX Input Frequency	f_{SI}		2500	MHz	
4	LO1/LO1X Input Level	P_{LO1}	-11	3	dBm	
5	LO1/LO1X Input Frequency	f_{LO1}		2500	MHz	
IF amplifier (PGC)						
6	Intermediate Frequency	IF	40	460	MHz	
7	IFI/IFIX Input Level	P_{IFI}		-12	dBm	
8	IFI/IFIX Input Frequency	f_{IFI}	40	460	MHz	
VCO (second local oscillator)						
9	LO2 Input Level	P_{LO2}	-35	0	dBm	
10	LO2 Input Frequency	f_{LO2}	80	920	MHz	VCO as Amplifier
11	VCO Frequency Range	f_{VCO}	80	920	MHz	
12	LO2O Output Level	P_{LO2O}		4	dBm	tuned for reso-nance, measured with high impedance probe
13	LO2O Output Frequency	f_{LO2O}	80 26.7	920 307	MHz MHz	**DIV1/3: L** **DIV1/3: H**
Demodulator outputs						
14	IR/X,QR/X Outp. Bandw.	B_{Out}	0	9.5	MHz	3dB roll off, see AC/DC characteristics page 21
Power down and logic inputs						
15	SYGCDT/SYGCCL/PGCSTR/ RXON1/RXON2/PUPLO2/OCE Input Voltage-L	V_L	0	0.5	V	
16	SYGCDT/SYGCCL/PGCSTR/ RXON1/RXON2/PUPLO2/OCE Input Voltage-H	V_H	2.0	VS	V	
17	Input Capacitance	C_I		2	pF	

Note:
Power levels are referred to impedance of 50 Ohms

6.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
	Supply currents							
1	Supply current	I_S	 7.8 8.4 16 32.5	 10.5 11.3 20 42	10 13.13 14.1 24 51.3	µA mA mA mA mA	RXON1/RXON2/PUPLO2 L / L / L H / L / L L / L / H L / H / L H / H / H	
	LNA **Input signal AI**							
2	Input Impedance		see diagrams 9.1 and 9.2, pages 42-44					2b
3	Max. Input Level	P_{AI}	 -23 -16	 -20 -13		dBm	1dB Compr. at AO, H, L gain 900MHz H, L gain 1.8/1.9GHz	1
4	Input Intercept Point	IPIP3	-7/-5/-5 -7/-5/-5	-4/-2/-2 -4/-2/-2	-1/+1/+1 -1/+1/+1	dBm	H gain, 0.9/1.8/1.9GHz L gain, 0.9/1.8/1.9GHz	1
5	Noise Figure (Values with matching for 900 MHz see design hints 9.1, page 39)	N_{AI} N_{AI} N_{AI} N_{AI}		1.5 3 8 9	2.5 3.5 9 10	dB dB dB dB	f_{RF}=900MHz;H gain f_{RF}=1.8/1.9GHz;H gain f_{RF}=900MHz;L gain f_{RF}=1.8/1.9GHz;L gain	1
5.1	Temp. coefficient	T_C		0.006		dB/K	see appl. circuit page 35	
	Output signal AO							
6	Output Impedance		see diagrams 9.1 and 9.2, pages 42-44					2b
7	Output collector current	I_{AO}		5 0.5		mA mA	H gain L gain	
8	Gain from Signal Input Without matching.	G_{LNA}	 15 -5 10.5 -9.5	 17 -3 13.5 -6.5	 19 -1 16.5 -3.5	 dB dB dB dB	f_{RF}=900MHz, H gain L gain f_{RF}=1.8/1.9GHz, H gain L gain	1
8.1	Temp. coefficient	T_C		-0.01		dB/K	see appl. circuit page 35	
9	Gain step	ΔG	19	20	21	dB		

AC/DC Characteristics (cont'd)

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
	First mixer **Input SI/SIX**							
10	Input Impedance		see diagram 9.3, page 45					2a
11	Max. Input Level	P_{SI}	 -14 -10	 -11 -7		dBm	1dB Compr. at MO/X f_{SI}=900MHz f_{SI}=1.8/1.9GHz	1
12	Input Intercept Point 3rd order	P_{IPI3}	2 -3			dBm	f_{SI}=900MHz f_{SI}=1.8/1.9GHz	1
13	Blocking Level Δf = 3 MHz	P_B	 -11 -7	 -8 -4		dBm	3dB Attenuation of wanted Signal at MO/MOX f_{SI}=900MHz f_{SI}=1.8/1.9GHz	1
14	Input Frequency	f_{SI}			2500	MHz		1
15	Noise Figure	 N_{SI} N_{SI}			 6/6.5 10/10.5 9/9.5 13/13.5	 dB dB dB dB	IF = 246/336 MHz DSB Noise, f_c=900MHz DSB Noise, f_c=1.8/1.9GHz SSB Noise, f_c=900MHz SSB Noise, f_c=1.8/1.9GHz see diagrams 2, 4, page 39	1
15.1	Temp. coefficient	T_C		0.01		dB/K		
	Output MO/MOX (open collector)							
16	Output Impedance		see diagram 9.5, page 47					2c
17	Total Output Collector Current	I_{MO+MOX}		4		mA		1
18	Power Gain from Signal Input	G_{MO}	11 7 5 2	14 10 8 4	17 13 11 6	dB dB dB dB	f_{MO}=40MHz, f_{RF}=900MHz f_{MO}=40MHz, f_{RF}=1.8/1.9GHz f_{MO}=246MHz, f_{SI}=900MHz, * f_{MO}=246MHz, f_{SI}=1.8/1.9GHz, * see diagram 3, page 39	1 1
18.1	Temp. coefficient	T_C		-0.015		dB/K		
19	Output Frequency IF	f_{IF}	40	246	460	MHz		1

* tank circuit at MO/MOX matched to output / tuned for resonance

AC/DC Characteristics (cont'd)

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
Input LO1/LO1X (first mixer local oscillator)								
20	Input Impedance		see diagram 9.4, page 46					2a
21	Input Level	P_{LO1} V_{LO1}	-11 177		3 890	dBm mVpp	see diagram 1, page 39	1 1
22	Input Frequency	f_{LO1}			2500	MHz		1
Isolation of first mixer								
23	From SI to MO	A_{SI-MO}		30		dB	f_{SI}=945MHz; f_{LO1}=900MHz	1
24	SI to LO1	A_{SI-LO1}		60		dB	"	1
25	LO1 to MO	A_{LO1-MO}		50		dB	"	1
26	LO1 to SI	A_{LO1-SI}		60		dB	"	1
27	MO to SI	A_{MO-SI}		50		dB	"	1
28	MO to LO1	A_{MO-LO1}		65		dB	"	1
29	From SI to MO	A_{SI-MO}		24		dB	f_{SI}=1.845GHz; f_{LO1}=1.8GHz	1
30	SI to LO1	A_{SI-LO1}		54		dB	"	1
31	LO1 to MO	A_{LO1-MO}		44		dB	"	1
32	LO1 to SI	A_{LO1-SI}		54		dB	"	1
33	MO to SI	A_{MO-SI}		44		dB	"	1
34	MO to LO1	A_{MO-LO1}		59		dB	"	1
Isolation between first Mixer Output to IF Input								
35	From MO to IFI	A_{MO-IFI}	60			dB	IF = 40 .... 460 MHz	1
Isolation between LNA Output to first Mixer Input								
36	From AO to SI	A_{AO-SI}		45		dB	f_{RF}=900 MHz	1
37	From AO to SI	A_{AO-SI}		45		dB	f_{RF}=1.8/1.9GHz	1

AC/DC Characteristics (cont'd)

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
IF amplifier (PGC) input IFI/IFIX								
38	Input Impedance		see diagram 9.6, page 48					2a
39	Max. Input Level	P_{IFI} V_{IFI}		-12 155		dBm mVpp	1dB Compr. PGC Gain: -10dB see diagram 5.1, page 39	1 1
40	Input Intercept Point	P_{IPI}	see diagram 5.1, page 39					1
41	Input Frequency	f_{SI}	40	246	460	MHz		1
42	Noise Figure	N_{SI}		6	7	dB	PGC Gain: 70dB see diagram 5.1, page 39	1

VCO (second local oscillator LO2)
Input LO2/LO2X (when used as amplifier for an external VCO)

#	Parameter	Symbol	min.	typ.	max.	Unit	Test Condition	Test Circuit
43	Input Impedance		see diagram 9.7, page 49					2b
44	Input Level	P_{LO2} V_{LO2}	-20 63		0 630	dBm mVpp	into 50 Ohms application hint	1 1
45	Input Frequency	f_{LO2}	80		920	MHz		1
Voltage controlled oscillator VCO (LO2)								
46	VCO Frequency range	f_{VCO}	80	492	920	MHz	*	1.1
47	VCO tuning range	Δf_{VCO}		32		MHz	Vt = 0.6 ... 2.3V **	1.1

* depending on external tuning circuit
** Test circuit 1.1 (f_{VCO}= 492MHz), page 26 and page 36

AC/DC Characteristics (cont'd)

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
	Output LO2O/LO2OX							
48	Output Resistance (diff.)	R_{LO2O}		1		kOhms		
49	Output Capacitance (diff.)	C_{LO2O}		1		pF	Parallel to R_{LO2O}	
50	Output Level	P_{LO2O}		-15		dBm	tuned for resonance	1
51	Output Level	P_{LO2O}		4		dBm	tuned for resonance, measured with high impedance probe (differential)	
52	Output Frequency	f_{LO2O}	80	492	920	MHz	**DIV1/3: L**	
53	Output Frequency	f_{LO2O}	26.7	164	307	MHz	**DIV1/3: H**	
54	SSB noise referenced	L(fm)			-121 -126 -131	dBc/Hz	fm=600 kHz fm=1.8 MHz fm=6 MHz; using high Q coil, Q=60-70 for oscillator tank circuit. **	1.1
55	power on delay	t_{po}		0.3		µs		

** Test circuit 1.1 (f_{VCO}= 492MHz), page 26 and page 36

AC/DC Characteristics (cont'd)

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
IF and BB chain: PGC==>Demodulator Outputs SOI/SOIX, SOQ/SOQX								
56	Output Resistance (diff.)	R_{OUT}		75		Ohms		
57	Output Capacitance (diff.)	C_{OUT}		1		pF		
58	Frequency roll off	f_{OUT}	3.0 3.6 4.1	5.0 6.0 6.8	7.0 8.4 9.5	MHz MHz MHz	VCC = 2.7V VCC = 3.6V VCC = 4.5V see diagram 6 page 41 and design hint 9.4 page 38	
59	DC Output Level	V_{OUTDC}		0.95		V		1
60	Diff. Output Offset Voltage	$V_{SO/X}$		±30	±100	mV	without offset comp. OCE = Low	1
61	AC Voltage Swing (diff.)	V_{OUTAC}			2.5	Vpp	differential	1
62	Voltage Gain from IF to I/Q-BB Output (IF: 225 / 246MHz) $g_{PGC+Demodulator}$	G_{OUT}	67 64 59 -13 -16 -21	70 67 62 -10 -13 -18	73 70 65 -7 -10 -15	dB dB dB dB dB dB	Gmax; IF = 246MHz Gmax; IF = 336MHz Gmax; IF = 435MHz Gmin; IF = 246MHz Gmin; IF = 336MHz Gmin; IF = 435MHz PGC: see table 4 page 11 and diagram 5.1, page 39 PGC controlled via 3 wire bus	1 1
63	PGC Gain step	Gstep		2		dB		1
64	I - Q Phase deviation	ΔφIQ			±3	deg	see design hint 8.2, page 36 design hint 8.4, page 38	1
65	Amplitude mismatch ΔV(I/Q)	ΔVI/Q			1.7	dB		1

AC/DC Characteristics (cont'd)

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
3 Wire bus inputs SYGCDT/SYGCCL/PGCSTR								
66	Input Voltage L	V_L	0		0.5	V		1
67	Input Voltage H	V_H	2.0		VS	V		1
68	Reference Voltage	Vcomp		1.75		V		1/1.2
69	Input Current	$-I_{in}$			5	µA	0v<=V_{in}<=VS	1
70	Clock frequency	fSYGCCL		3.25	13	MHz		1/1.2
71	Set - up time (start)	TSUSTA	30			ns		1/1.2
72	H pulse width (clock)	THIGH	20			ns		1/1.2
73	L pulse width (clock)	TLOW	20			ns		1/1.2
74	Set - up time (data transfer)	TSUDAT	20			ns		1/1.2
75	Hold time (data transfer)	THDDAT	20			ns		1/1.2
76	Rise time	TR		20	40	ns		1/1.2
77	Fall time	TF		20	35	ns		1/1.2
78	Set - up time (stop)	TSUSTO	30			ns		1/1.2
79	Setting Time	t_{set}		200		ns	Setting of gain after programming	1
80	Start time	t_{start}		200		ns	Programming start time after power up	1
Power-down and control inputs RXON1, RXON2, PUPLO2,OCE								
81	Input Voltage L	V_L	0		0.5	V		1
82	Input Voltage H	V_H	2.0		VS	V		1
83	Input Current L	I_L			2.5	µA	0<=V_{PDL}<=0.5V	1
84	Input Current H	I_H			25	µA	2.0V<=V_{PDH}<=VS	1
85	Input capacitance	C_{in}			2	pF		

AC/DC Characteristics (cont'd)

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
	Differential Operational Amplifier (open loop)							
86	Slew Rate	SR		2.6		V/µs		
87	Gain-Bandwidth Prod.	GBW		12		MHz		
88	Voltage Gain	A_{Vo}		60		dB		
89	Phase margin			60		degr.		
90	Gain margin	A_R		14		dB		
91	Common-Mode Rejection	CMR		70		dB		
92	Offset Voltage	V_{OFF}		1		mV	at input INQ/X,INI/X	
93	Output Voltage (IR/X,QR/X)	V_{OUT}			2.5	Vpp	differential	
94	Diff. Output Offset Volt.(IR/X,QR/X)	$V_{OUT/X}$			1	mV/ms	with offset compensation (S&H) over the whole temperature range	1
95	DC Output Level (IR/X,QR/X)	V_{outDC}		0.95		V	depends on SO-DC output level	1
96	Output Resistor	$R_{(out/outx)}$		250		Ω	differential	

Note: The operational amplifiers do not offer wideband capability (see also design hint 8.3 page 37 and design hint 8.4 page 38).

AC/DC Characteristics (cont'd)

Supply voltage V_S = 2.7V to 4.5V; ambient temperature T_A = 25°C

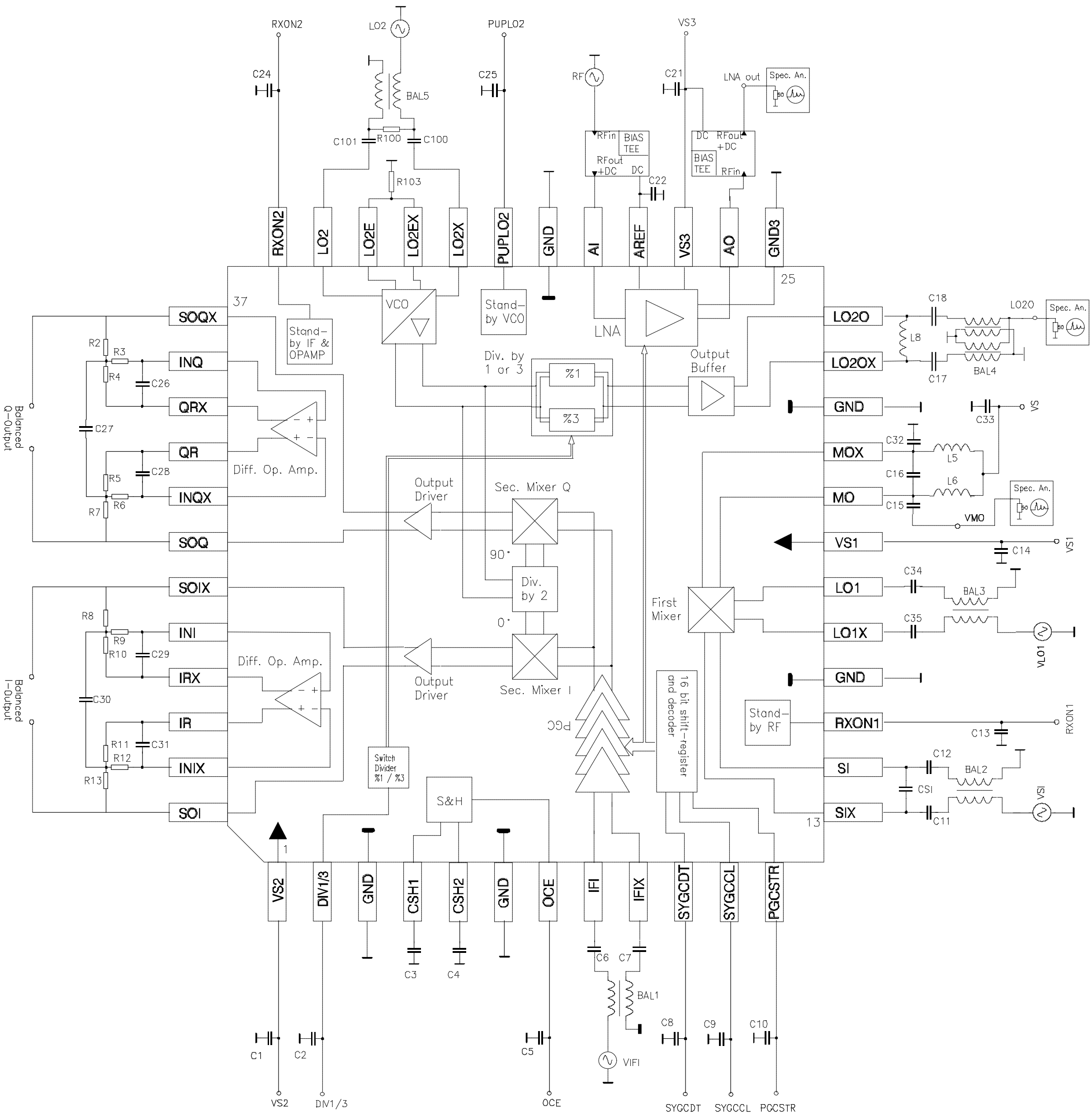
#	Parameter	Symbol	Limit Values			Unit	Test Condition	Test
			min.	typ.	max.			Circuit
	Sample and Hold							
97	Voltage drift at output IR/X, QR/X	V_{dritt}			1	mV/ms	(CSH1/2 = 47nF) during hold time, dep. of capac. C, for the whole temperature range, see diagram 7, page 41	1
98	Min. Sample time	t_{sample}			50 350	µs µs	CSH1/2 ≤ 120nF t PD2 off ≤ 10ms CSH1/2 ≤ 120nF t PD2 off ≥ 10ms see diagram 8, page 41	1
99	Diff. Output Offset Volt. at OP-output	V_{OPdiff}			5	mV	during sample time and the beginning of hold time	1
100	Diff. load at Op-out Single ended load to GND Single ended load to V_{ref}	Rl_{diff} Rl_{se} Rl_{se}	10 50 50			kΩ MΩ kΩ	 0.8V ≤ V_{ref} ≤ 1.3V	see diagram 8, page 41

Note: The operational amplifiers do not offer wideband capability. In wideband applications,the Sample and Hold therefore must be deactivated by setting the OCE input to L (see also design hint 8.4 page 38).

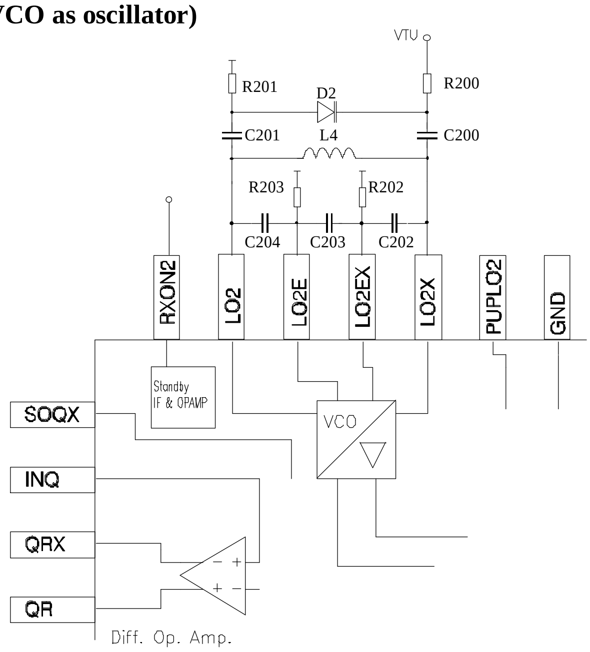
7 Test Circuits

7.1 Test Circuit 1

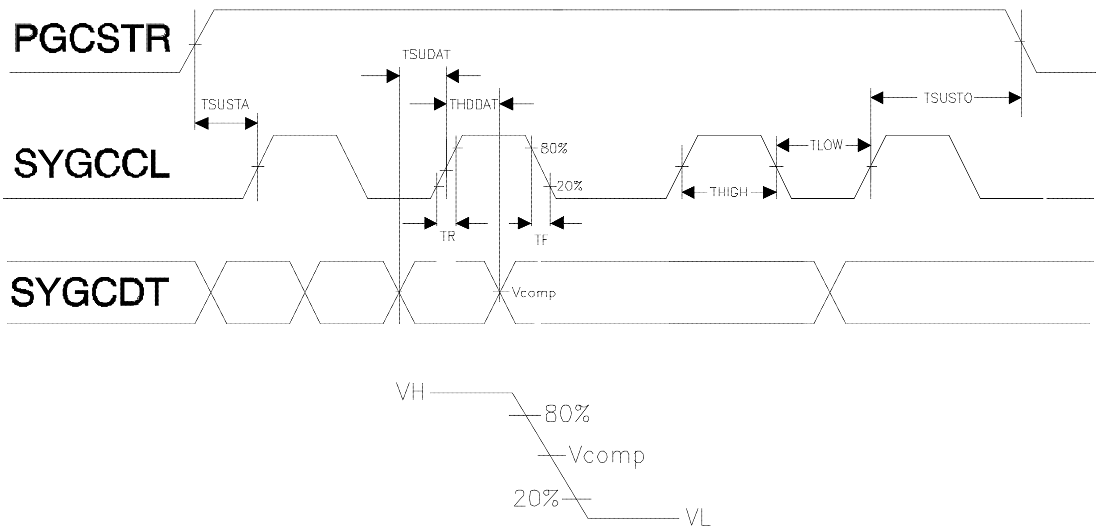
Note:
Resistors R2 - R7, R8 - R13 and capacitors C27 - C31 are not necessary in a wideband application (see also design hint 8.4).
However, the test board offers the possibility to mount these components (e.g. for a low pass filter in small band applications).



7.2 Test Circuit 1.1 (VCO as oscillator)



7.3 Test Circuit 1.2 (3-wire-bus timing)

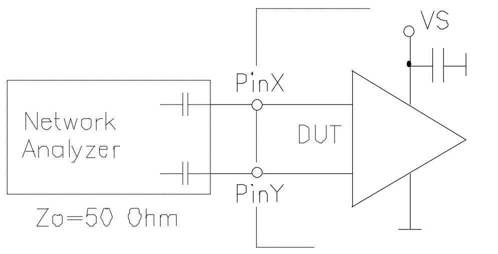


TSUSTA Set - up time (start)
THIGH H pulse width (clock)
TLOW L pulse width (clock)
TSUDAT Set - up time (data transfer)
THDDAT Hold time (data transfer)
TR Rise time
TF Fall time
TSUSTO Set - up time (stop)

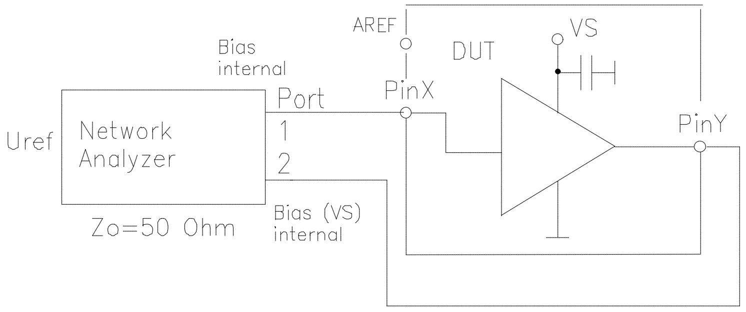
Rise and Fall time to 20% and 80% values
All other times referenced to Vcomp

7.4 Test Circuit 2

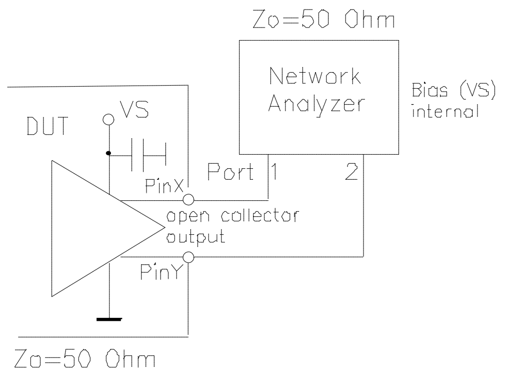
7.4.1 Test Circuit 2a



7.4.2 Test circuit 2b



7.4.3 Test Circuit 2c

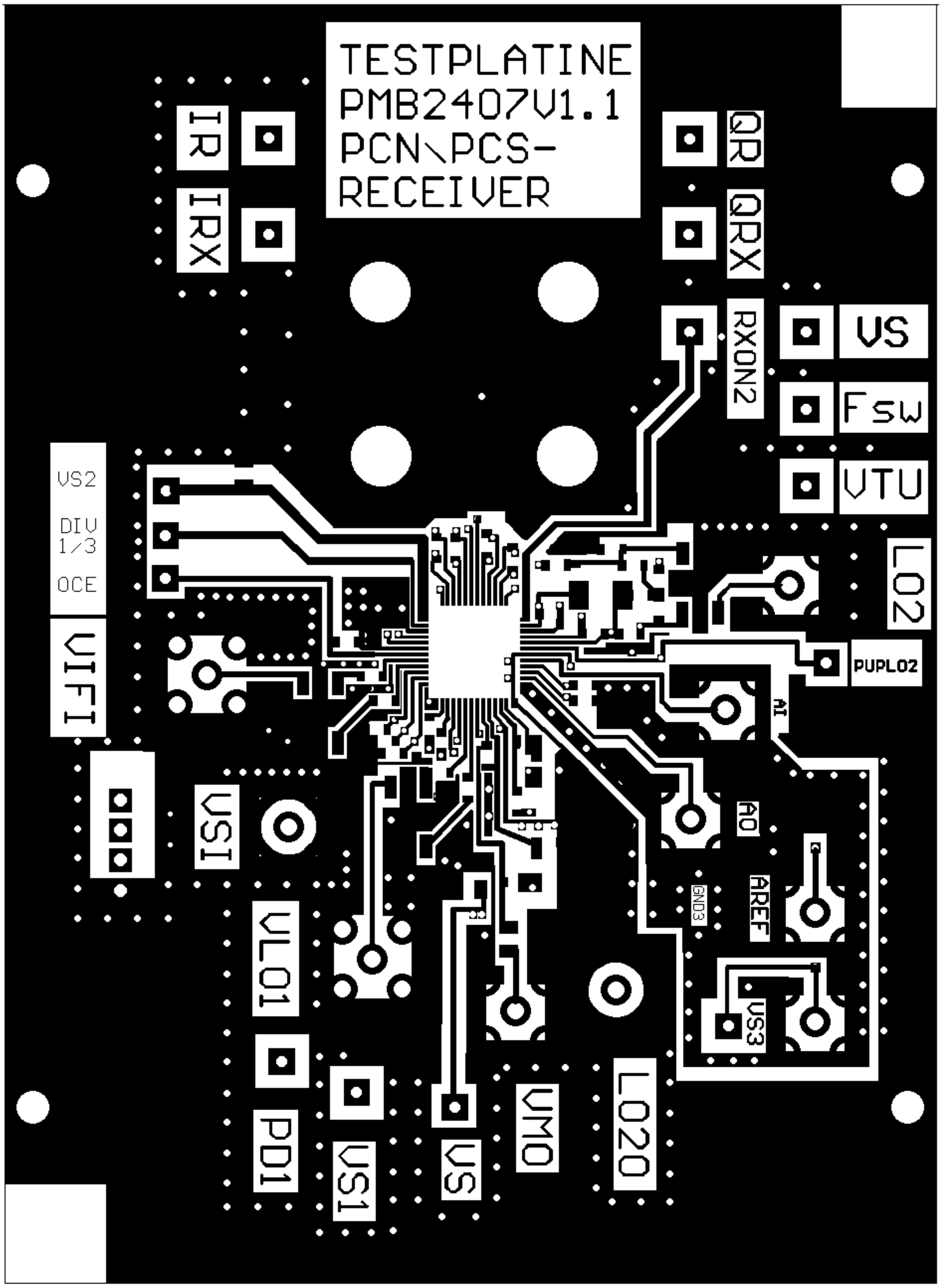


The S parameters are tested at the indicated frequency and the equivalent parallel or series circuit can be calculated on this base.

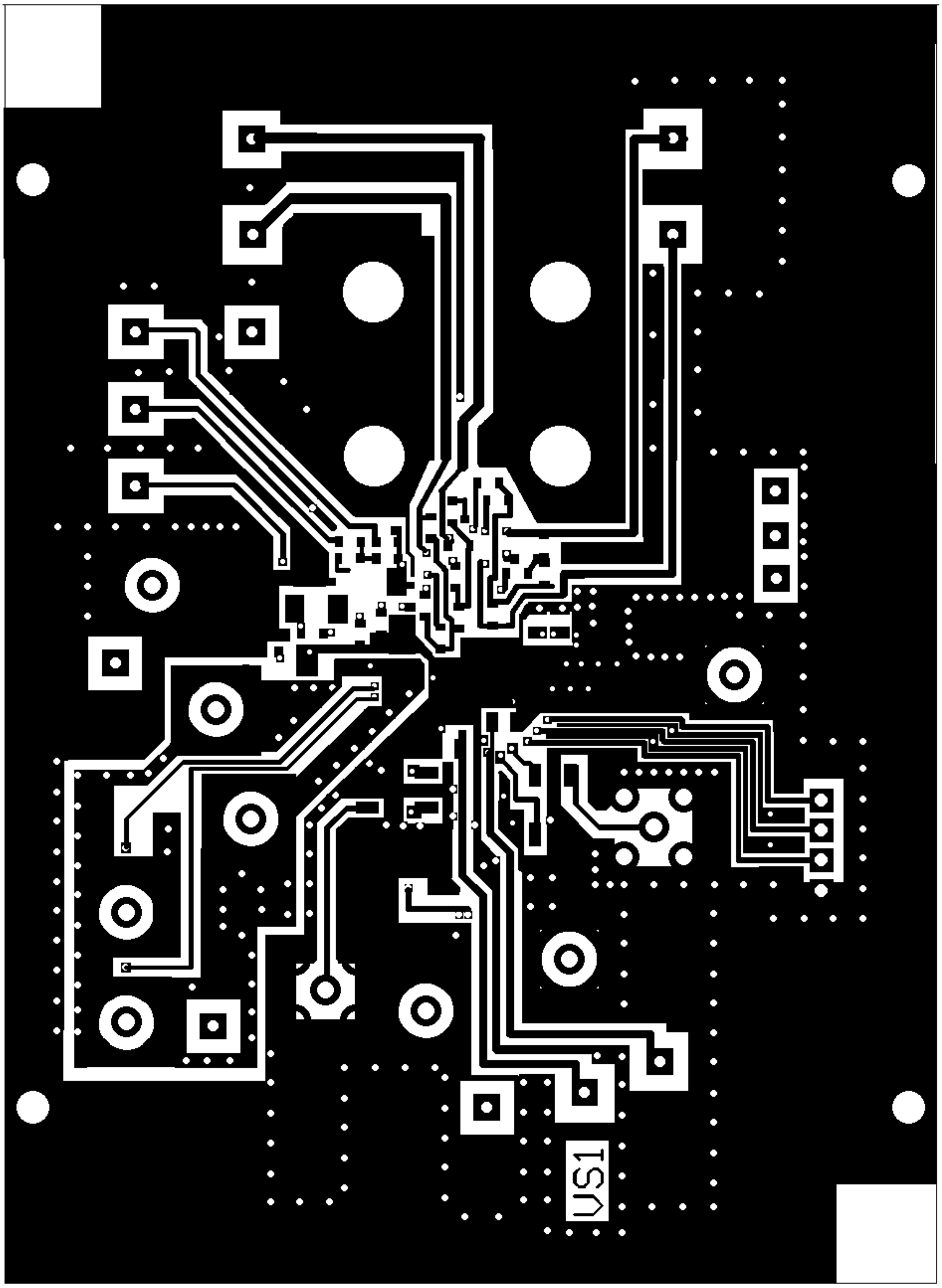
Test point	Test Circuit	Test Frequency / MHz	Pin X	Pin Y
LO1-Input Impedance	2a	200....2000	17	18
SI-Input Impedance	2a	200....2000	13	14
MO-Output Impedance	2c	10.....600	20	21
IFI-Input Impedance	2a	10....600	8	9
LO2-Input impedance	2a	10... 1000	32	35
LNA-I/O impedance	2b	200 2000	29	26

7.5 Test Board (Test boards PMB2407 V1.1 are available on request, also usable for PMB2408 V1.1)

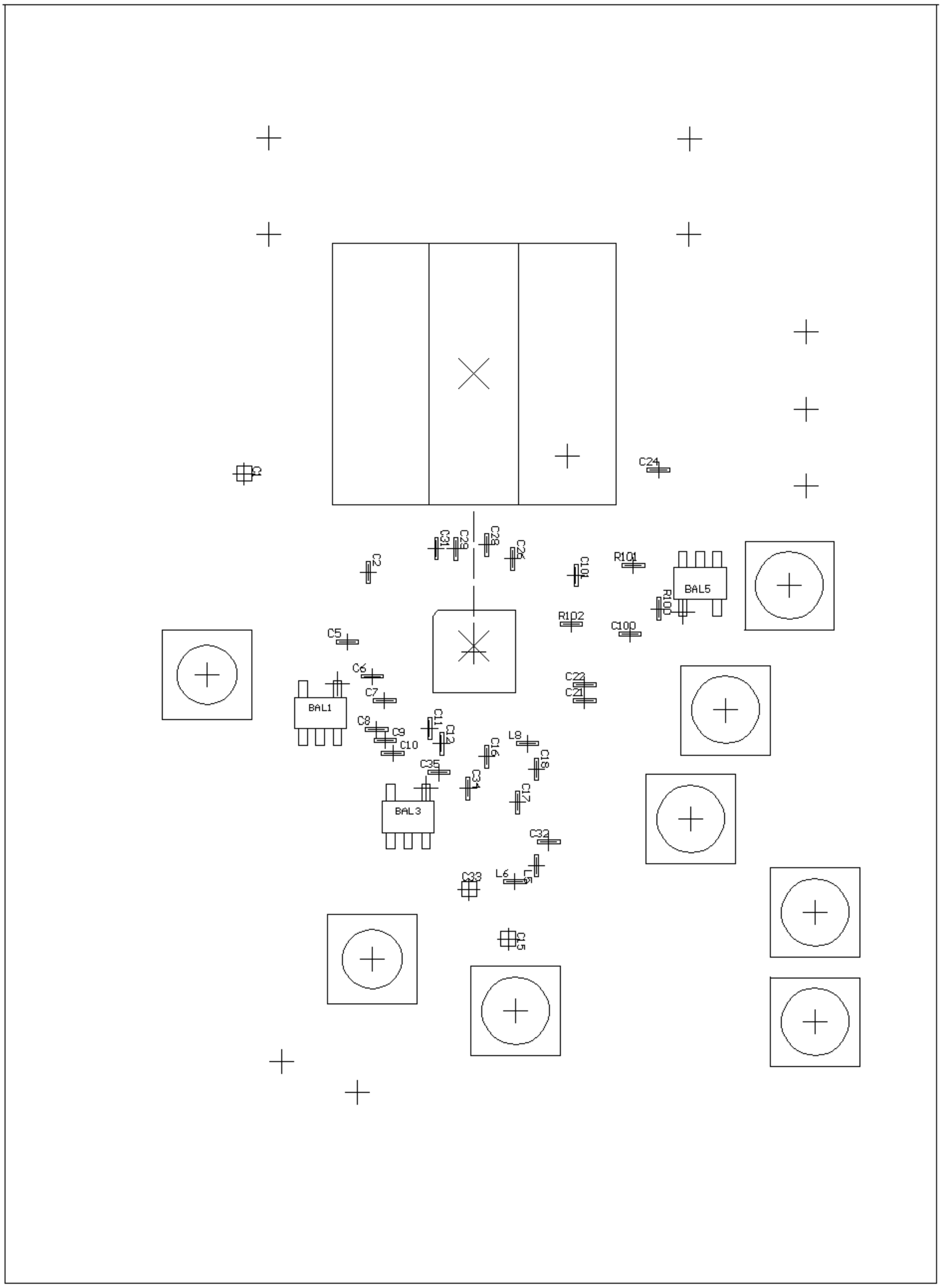
7.5.1 Test Board: Layout Top



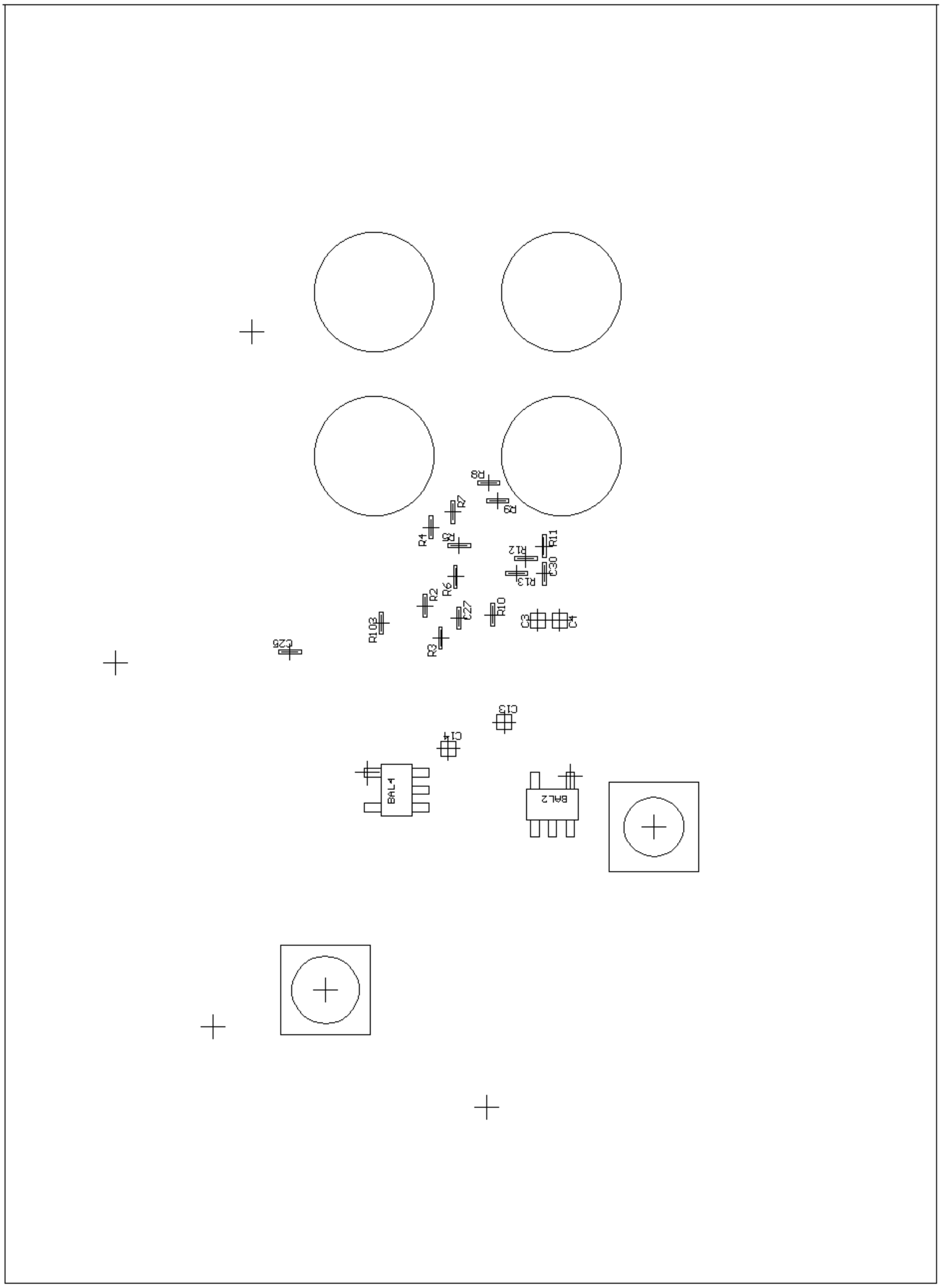
7.5.2 Test Board: Layout Bottom



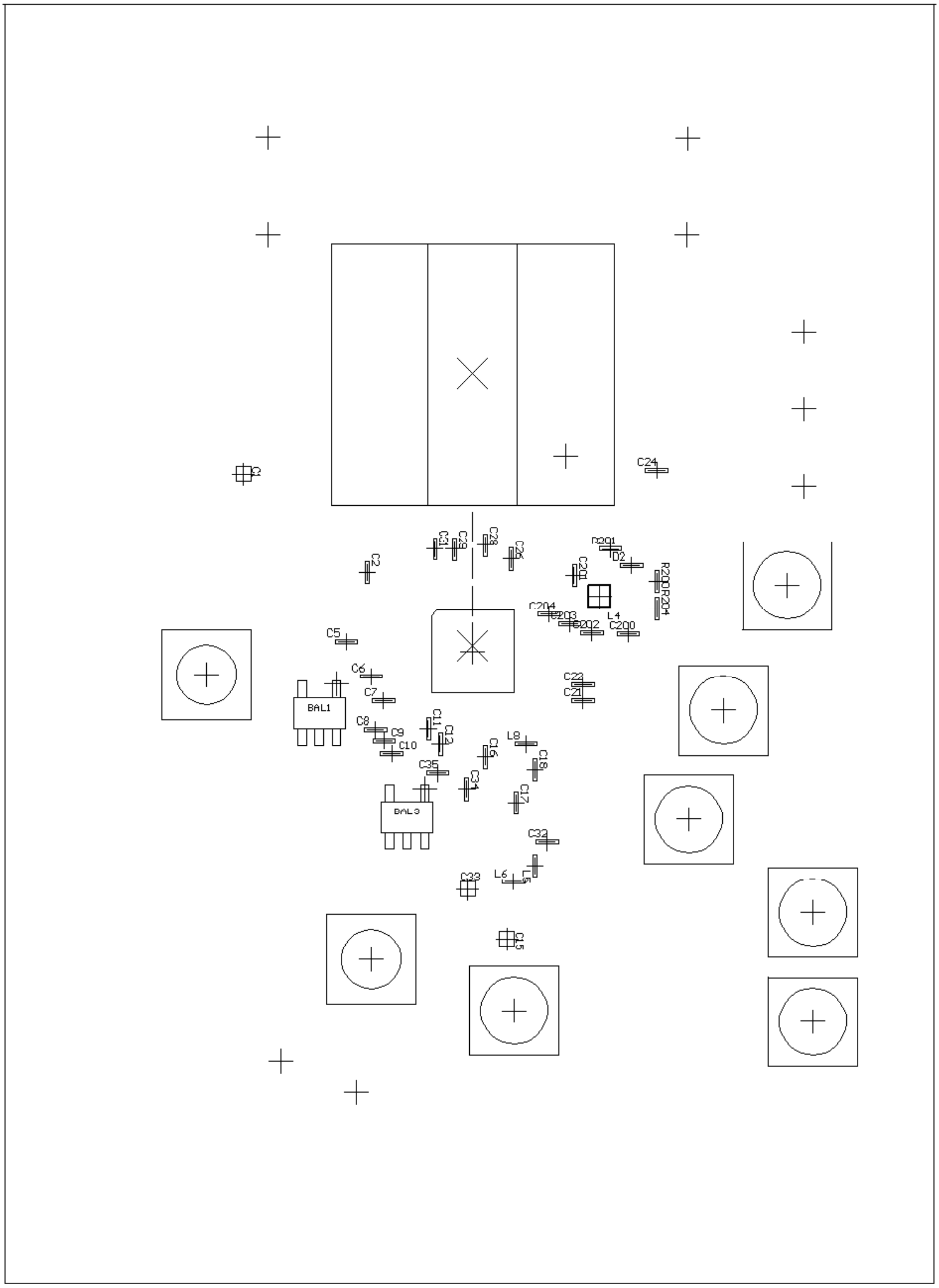
7.5.3 Test Board: Top Place for Test Circuit 1



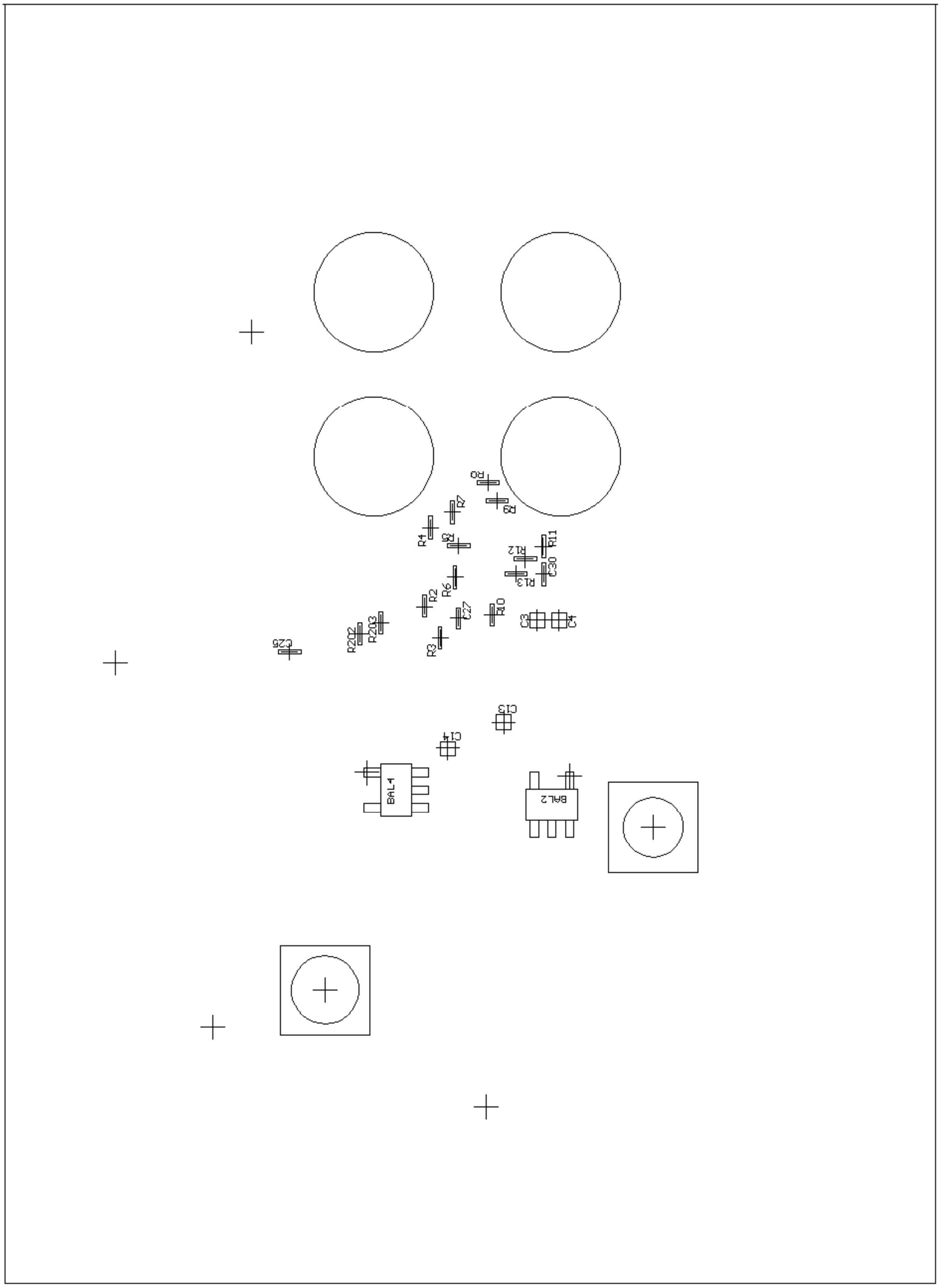
7.5.4 Test Board: Bottom Place for Test Circuit 1



7.5.5 Test Board: Top Place for Test Circuit 1.1



7.5.6 Test Board: Bottom Place for Test Circuit 1.1



7.5.7 List of Components: Test Circuit 1

Component values

C1, C14	10nF
C3, C4	47nF
C2, C5, C8, C9, C10, C13, C24, C25	10pF
C6, C7, C11, C12, C17, C18, C21, C22, C33, C34, C35, C100, C101	1nF
C15, C32	1.8pF (IF = 246MHz)
C16	2.7pF (IF = 246MHz)
CSI (not placed on test board, but it is possible to add the comp.)	2.2pF
C26, C28, C29, C31	not required
L5, L6	33nH (IF = 246MHz)
L8	330nH (LO2O = 164MHz)
	47nH (LO2O = 492MHz)
R100	51
R103	270
BAL1, BAL2, BAL3, BAL5	1:1 Balun TOKO 617DB-1023
BAL4	1:2 Balun TOKO 617DB-1010
D2	BBY51

Test Circuit 1.1 (+ components of test circuit 1)

R200, R201	4.7k
R202, R203	560
C200, C201	18p
C202, C204	2.2p
C203, C205	8.2p

(C203 and C205 are on test board as C203 differential between LO2E and LO2EX, a splitting of these capacitance are better for phase noise. It can be placed parallel to R202 and R203.)

L4	15n (492MHz)

These components replace the following components of test circuit 1:

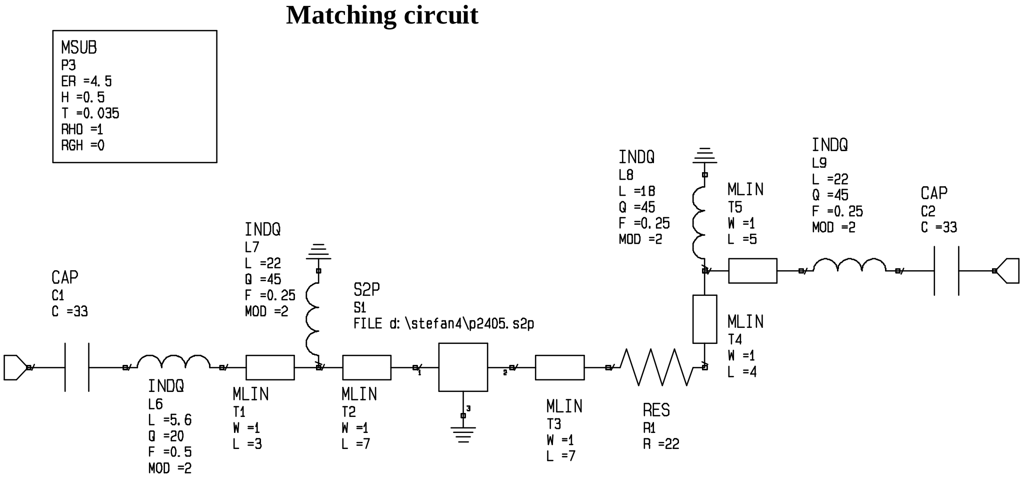
BAl5, R100, C100, C101, R103

8 Design hints

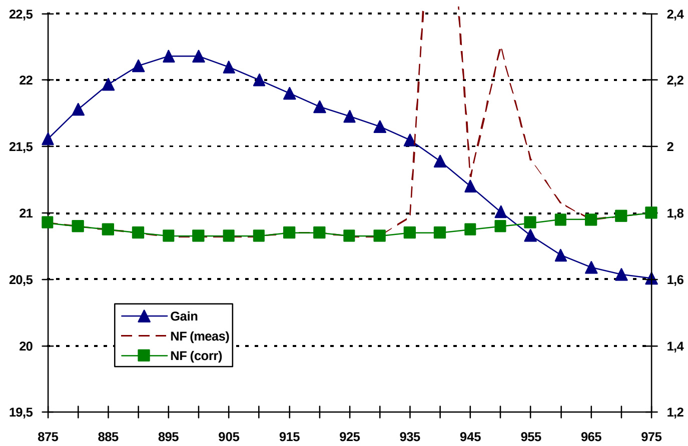
8.1 LNA matching for 925MHz (GSM 900); <u>all parameters are measured;</u> dimensions in mm

Test boards are available

Matching circuit



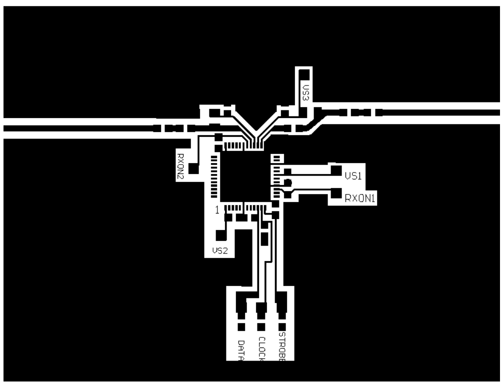
Gain and Nois Figure results versus RF-frequency



Gain/dB; NF/dB; f/MHz

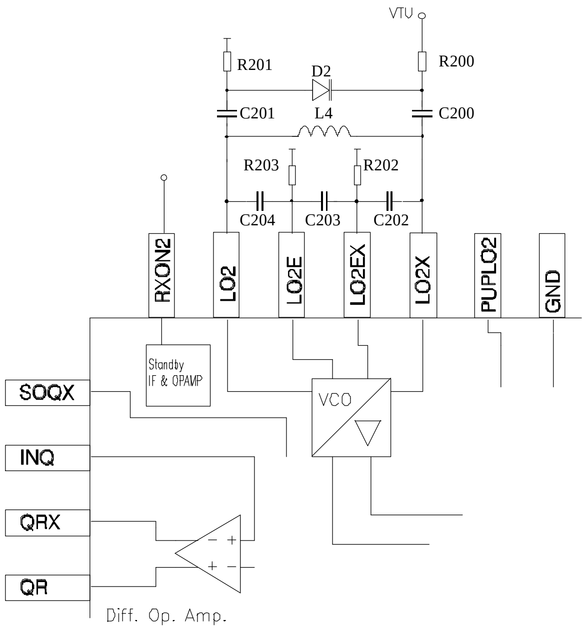
stability factor K	> 2.3
input return loss	> 17 dB
output return loss	> 14 dB

Test board

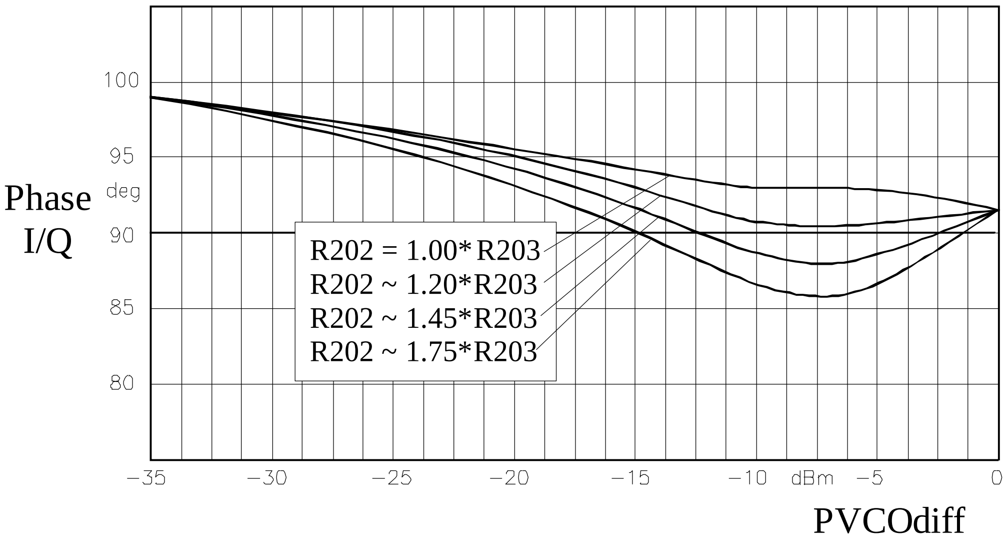


8.2 VCO: Possibility of I/Q phase error correction with a wanted resistor mismatch in the external VCO-circuit (R202, R203)

VCO - test circuit



Phase error correction diagram



To optimize phase-error the resistor R203 has to be fix and the resitor R202 has to be changed for the ideal phase.
An increase of even harmonics of maximal 5dB at LO2O/X-output can be expected.

For example the VCO has a diff. level of about -12.5dBm, R203=560Ω then R202 has to be 820Ω.

8.3 Sample and Hold: Offset compensation diagram for smallband applications

Baseband frequency ≤ 400kHz

A differential DC-offset at the demodulator's outputs is also amplified by the OpAmp's. Hence this differential offset must be compensated, it is sensed via the sample and hold circuitry (one separate circuit for each channel I and Q) at both opamp's outputs IR/IRX (QR/QRX). A feedback loop corrects the remaining offset error below the tolerable input value of the baseband A/D converter. Figure 8.3.1 shows the block diagram of one of the two offset compensation circuits. Figure 8.3.2 shows the timing diagram of the compensation. The voltage drift during hold time is determined by the external capacitance C.

Figure 8.3.1: Offset compensation diagram

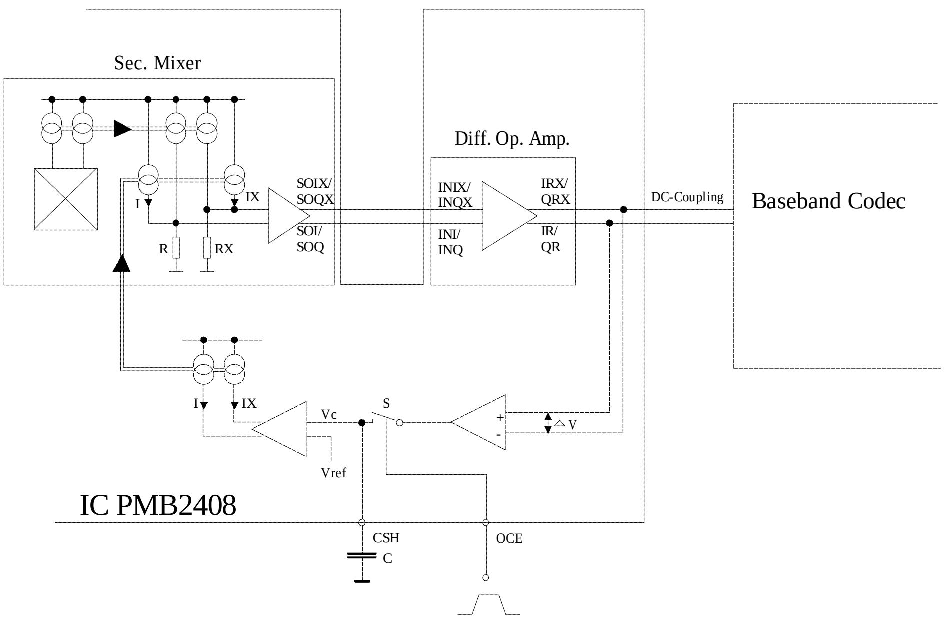
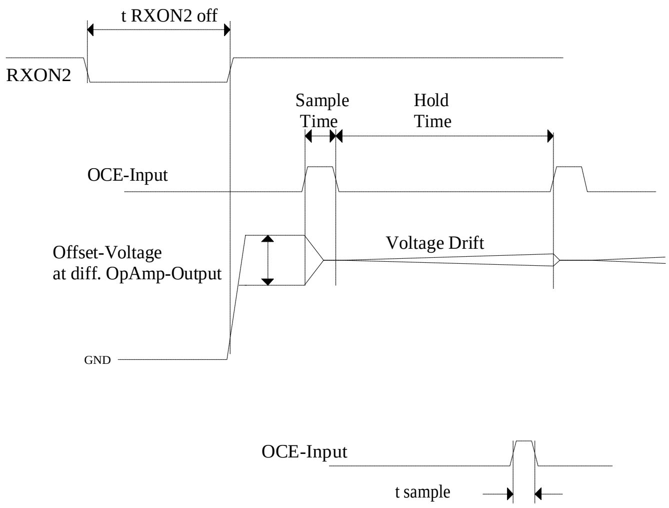
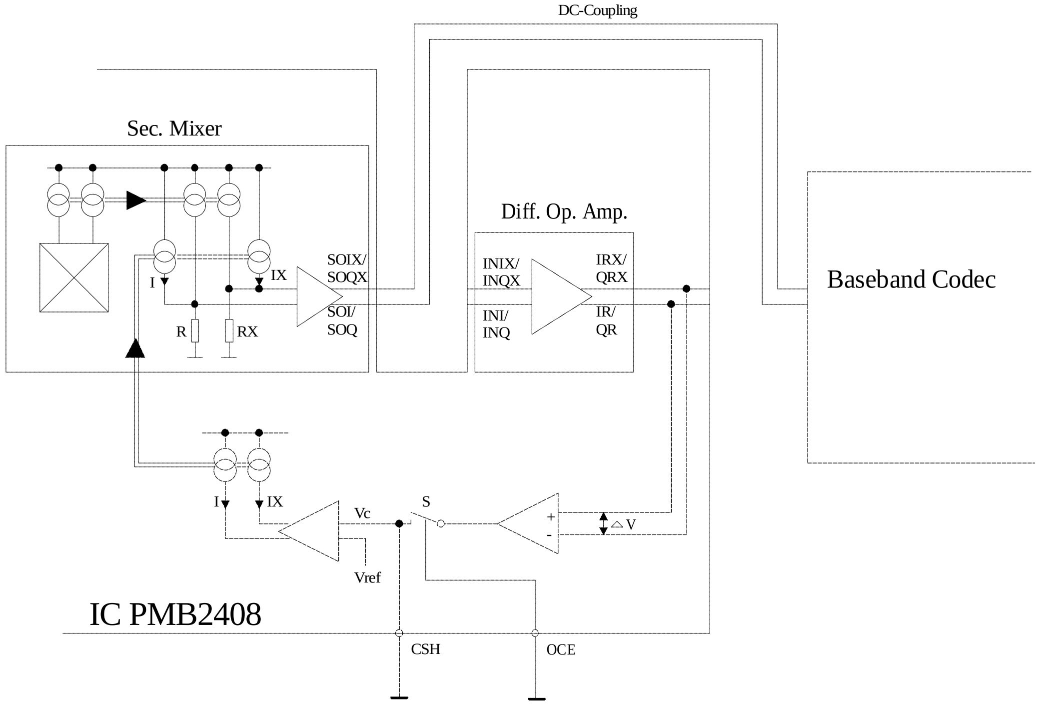


Figure 8.3.2: Offset compensation timing



8.4 Sample and Hold: Offset compensation diagram for wideband applications

Baseband frequency ≥ 400kHz

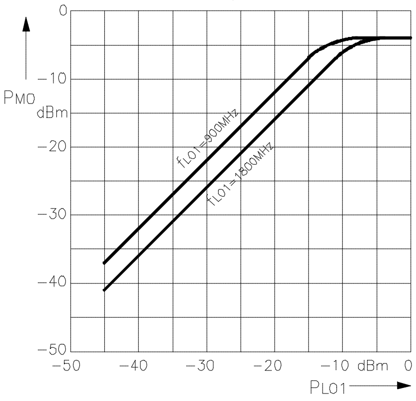


In wideband applications the use of the Sample and Hold is not to be recommended.
The Sample and Hold has to be deactivated by connecting the pins CSH1, CSH2 and OCE to GND.

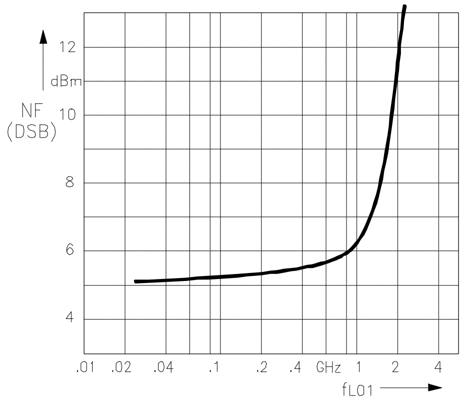
Explanation:
The internal operational amplifiers do not offer wideband capability and will not be used in a wideband application.
An offset compensation loop as described under 8.3 might cause an additional I/Q phase error in the baseband path. (The operation point of the Sample and Hold circuitry has an influence on the roll-off of the I/Q demodulator. Since this operation point might be different between I and Q channel, the baseband roll-off is also slightly different between I and Q which causes an additional phase error).
Connecting the pins CSH1, CSH2 and OCE to GND avoids this problem and sets both sample and hold circuits in a defined state. Note that this causes a differential output voltage of ±100mV max. at the pins SOI/SOIX (and SOQ/SOQX, respectively).

9 Diagrams

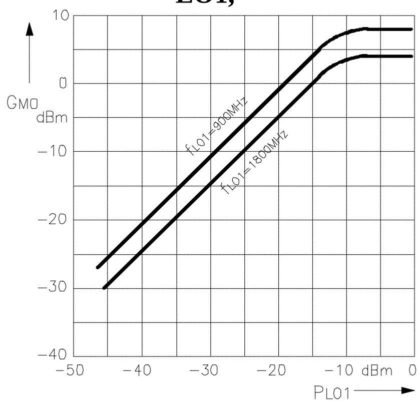
9.1 Diagram 1: First Mixer: Output power versus LO-Level P_{LO1}, IF = 246MHz



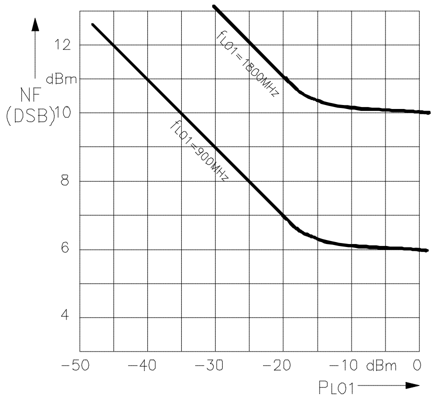
9.2 Diagram 2: First Mixer: Noise Figure NF versus LO-Frequency f_{LO1}, IF = 246MHz



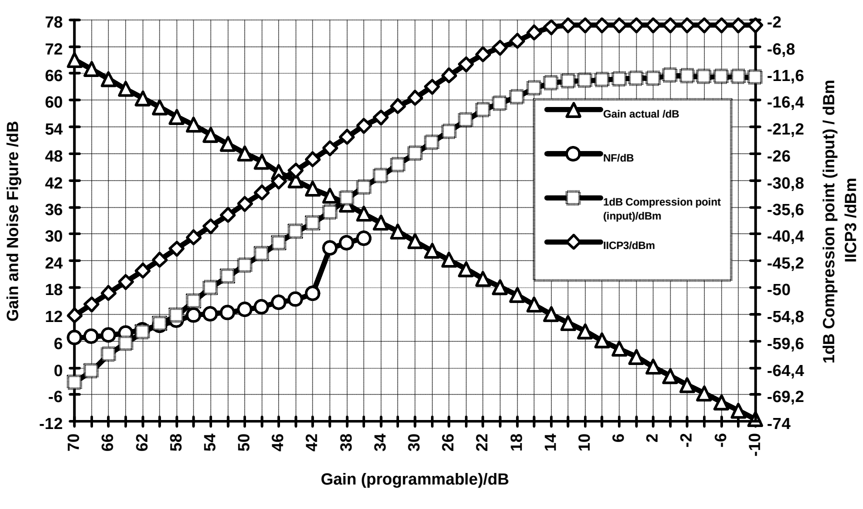
9.3 Diagram 3: First Mixer: Mixer gain versus LO-Level P_{LO1}, IF = 246MHz



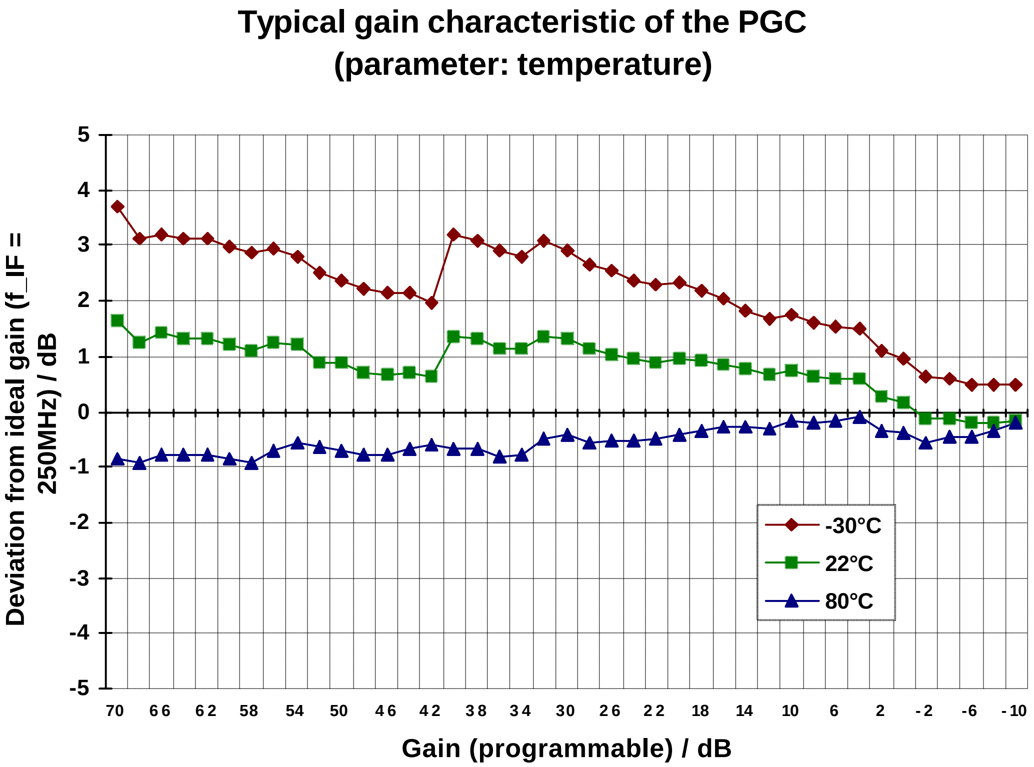
9.4 Diagram 4: First Mixer: Noise Figure NF versus LO-level P_{LO1}, IF = 246MHz



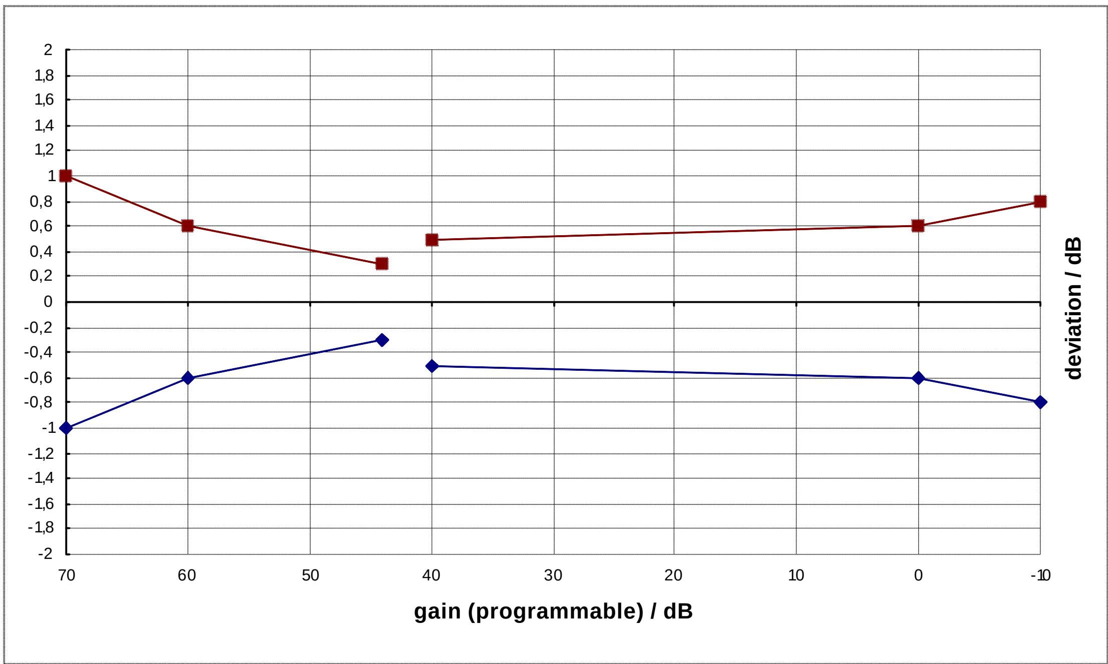
9.5.1 Diagram 5.1: Gain, Noise Figure, 1dB Compression point and IICP3 of PGC versus prog. Gain



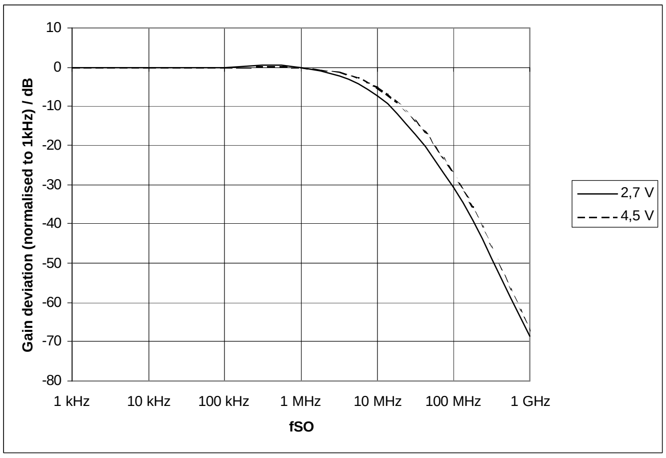
9.5.2 Diagram 5.2: Deviation from ideal gain versus prog. gain (parameter: temperature)



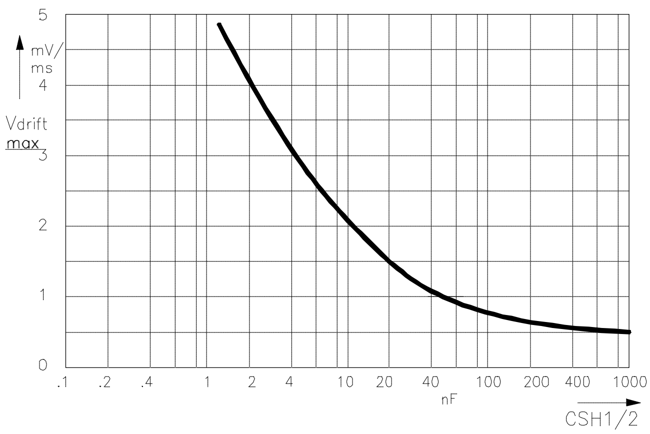
9.5.3 Diagram 5.3: Deviation / tolerances from typical PGC gain characteristic (fix-point: gain = 42dB, temperature range: -20 - 80°C)



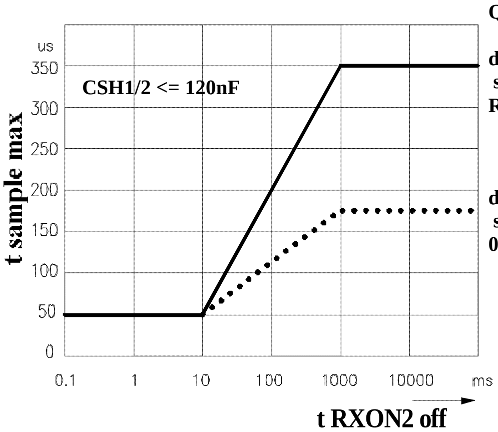
9.6 Diagram 6: Baseband frequency response versus baseband frequency (normalised to 1kHz)



9.7 Diagram 7: Sample and Hold circuit: Voltage drift (during hold time) versus capacitance C.



9.8 Diagram 8: Sample and Hold circuit:Maximum sample-time versus PD2 time in switched off mode.



Load at OP-output QR/QRX, IR/IRX:

diff. load Rdiff >= 50kOhm, single ended load Rse to GND Rse >= 50 MOhm

diff. load Rdiff >= 50kOhm, single ended load Rse to Vref = 0.8 to 1.3V Rse >= 50 kOhm

9.9 Diagram 9: S - Parameters

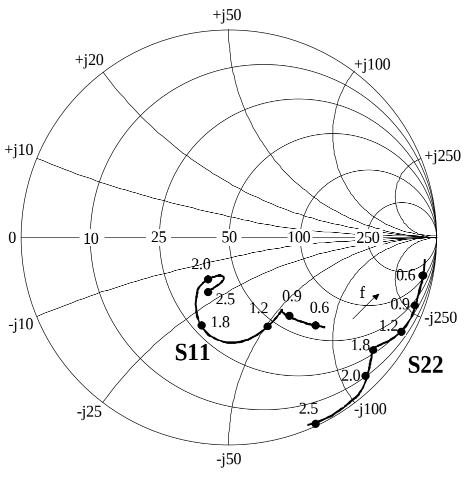
S - Parameters are available on 3.5"-disk or by E-Mail

All S-parameters are measured.

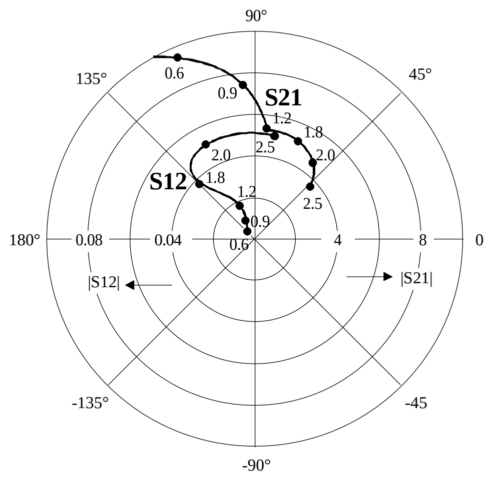
Diagram 9.1: S Parameters Low Noise Amplifier LNA (High - gain)

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.50000	0.60219	-40.3	10.69917	123.2	0.003164	117.3	0.94803	-11.0
0.60000	0.55175	-46.6	9.61832	114.8	0.004373	131.2	0.94778	-12.9
0.70000	0.49605	-48.1	8.75558	108.1	0.007302	125.5	0.93671	-14.8
0.80000	0.47690	-51.1	7.90483	102.5	0.009100	119.0	0.94320	-17.0
0.90000	0.43958	-55.5	7.26950	96.7	0.010875	112.7	0.92531	-19.0
1.00000	0.42526	-56.4	6.51932	91.7	0.013142	120.0	0.93766	-21.5
1.10000	0.42963	-58.4	5.87501	88.4	0.015218	117.5	0.94495	-23.9
1.20000	0.44745	-62.3	5.35753	86.9	0.016878	109.5	0.95041	-27.0
1.30000	0.47224	-69.4	5.07177	86.8	0.017269	104.7	0.95011	-30.4
1.40000	0.48599	-79.3	5.02650	86.8	0.016418	105.7	0.93809	-33.8
1.50000	0.47538	-91.1	5.17023	84.5	0.015493	118.0	0.91518	-36.6
1.60000	0.43460	-103.3	5.30013	79.3	0.019177	134.6	0.89318	-38.1
1.70000	0.37255	-112.9	5.26928	73.1	0.026538	138.2	0.88071	-38.8
1.80000	0.30599	-119.5	5.11285	66.9	0.038264	134.6	0.85575	-40.2
1.90000	0.24813	-122.2	4.88020	61.0	0.044188	127.0	0.90822	-40.8
2.00000	0.20416	-120.1	4.61071	56.2	0.051163	118.4	0.93424	-42.6
2.10000	0.17949	-114.5	4.35266	52.1	0.055754	110.0	0.95955	-45.3
2.20000	0.17545	-108.6	4.10839	48.4	0.059411	102.1	0.97890	-48.4
2.30000	0.18662	-104.2	3.87209	45.7	0.062352	94.8	1.00177	-52.3
2.40000	0.22967	-106.3	3.65636	44.5	0.059714	85.3	1.01585	-57.4
2.50000	0.27790	-116.7	3.61054	44.2	0.053020	78.8	1.01013	-63.5

S11, S22 = f (f) (High - gain)



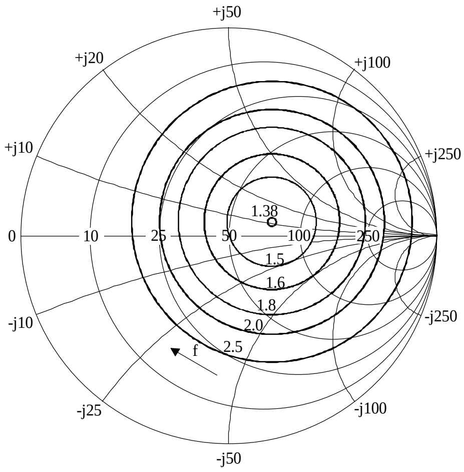
S21, S12 = f (f) (High - gain)



Noise Parameters

Freq.	NFmin	Γopt		Yopt		Rn
[GHz]	[dB]	Mag	Angle	Gopt [mS]	Bopt [mS]	[Ω]
0.9	1.386	0.201	23.2	13.62	-2.25	12.35
1.8	2.573	0.101	16.9	16.46	-0.97	18.45

Noise Characteristic 900MHz



1.8GHz

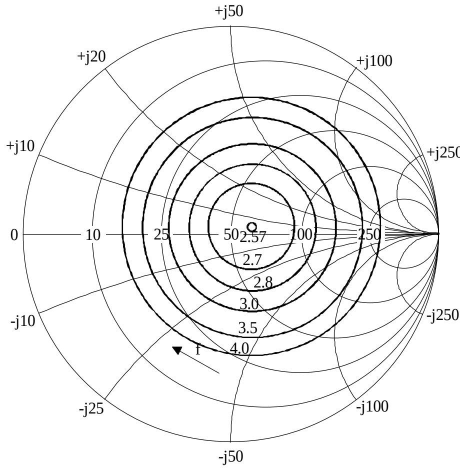
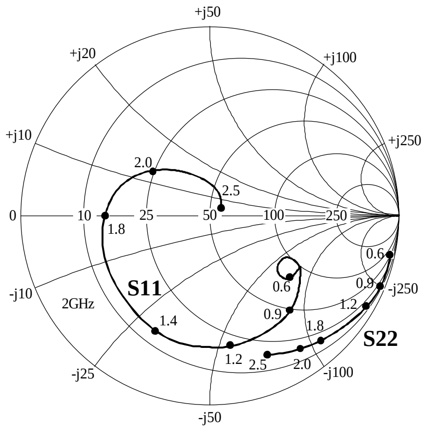


Diagram 9.2: S Parameters Low Noise Amplifier LNA (Low - gain)

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.50000	0.53673	-28.4	1.19991	119.7	0.004303	110.4	0.98268	-12.0
0.60000	0.55460	-36.2	1.04425	108.4	0.004681	125.0	0.97743	-14.5
0.70000	0.55834	-32.6	0.95402	100.1	0.008020	109.9	0.97039	-17.3
0.80000	0.60876	-40.3	0.82273	91.2	0.009226	104.0	0.96565	-20.0
0.90000	0.62694	-50.2	0.68876	84.9	0.008710	102.6	0.95902	-22.9
1.00000	0.66372	-58.3	0.57105	79.1	0.008306	103.7	0.95351	-25.8
1.10000	0.71236	-69.2	0.46408	77.3	0.008386	108.9	0.94672	-28.7
1.20000	0.73322	-82.7	0.37931	80.4	0.008422	132.1	0.93941	-31.7
1.30000	0.73998	-96.7	0.33736	88.4	0.011434	152.9	0.93136	-34.7
1.40000	0.72803	-111.4	0.33704	96.8	0.018059	160.8	0.92316	-37.7
1.50000	0.70182	-126.8	0.36716	101.3	0.026780	157.7	0.91338	-40.6
1.60000	0.66266	-142.7	0.40793	101.3	0.036729	151.0	0.90417	-43.3
1.70000	0.60969	-159.9	0.44921	98.2	0.047852	140.7	0.89373	-46.0
1.80000	0.54159	-178.4	0.48287	92.7	0.058903	129.9	0.88457	-48.6
1.90000	0.46230	162.3	0.49895	86.0	0.067609	118.6	0.87869	-51.2
2.00000	0.37371	142.1	0.49917	78.7	0.074069	106.8	0.86960	-53.6
2.10000	0.29255	123.9	0.48430	72.5	0.075587	95.4	0.86348	-56.3
2.20000	0.23181	105.7	0.46296	67.2	0.075901	86.4	0.85450	-59.4
2.30000	0.18204	84.7	0.44123	62.5	0.075077	77.9	0.84529	-62.7
2.40000	0.12474	56.2	0.41188	59.1	0.070290	68.1	0.83477	-66.6
2.50000	0.06166	15.7	0.38682	57.5	0.059321	62.8	0.82243	-70.9

S11, S22 = f (f) (Low - gain)



S21, S12 = f (f) (Low - gain)

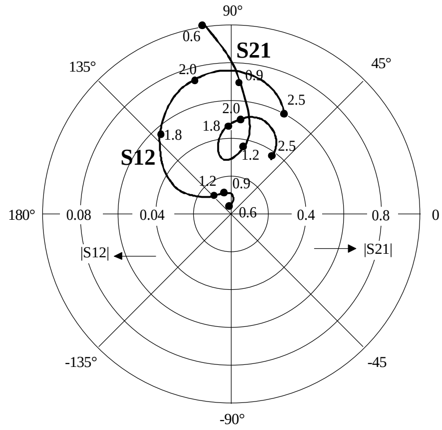


Diagram 9.3:
S Parameters First Mixer Signal Input SI/SIX

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.18000	0.33162	155.1	0.25513	17.6	0.258797	17.0	0.32044	155.9
0.30000	0.30325	146.3	0.29296	14.1	0.297072	13.6	0.29138	147.6
0.42000	0.29021	140.7	0.31037	10.4	0.313587	9.6	0.27509	142.9
0.54000	0.28686	136.8	0.31769	7.4	0.320856	6.5	0.26819	139.5
0.66000	0.28826	133.7	0.31843	5.0	0.321270	4.1	0.26426	136.6
0.78000	0.29359	131.0	0.31660	3.2	0.318838	2.3	0.26449	133.9
0.90000	0.29875	128.3	0.31389	2.1	0.315233	0.8	0.26466	131.4
1.02000	0.29969	124.1	0.31810	1.6	0.320269	−0.2	0.26391	126.2
1.14000	0.29937	124.8	0.30274	−2.6	0.299654	−4.4	0.25743	126.7
1.26000	0.31080	120.8	0.29508	−2.4	0.290249	−4.4	0.26547	122.2
1.38000	0.31895	116.7	0.28869	−2.7	0.280016	−4.9	0.27351	117.5
1.50000	0.32770	112.0	0.28234	−3.0	0.266453	−5.4	0.28443	112.8
1.62000	0.34112	106.3	0.27895	−3.1	0.250136	−2.7	0.31008	107.1
1.74000	0.34253	99.7	0.27948	−5.3	0.273966	−0.8	0.32802	96.7
1.92000	0.36085	93.0	0.26247	−8.3	0.262338	−7.9	0.33713	89.9
2.04000	0.37616	88.4	0.24655	−10.2	0.243372	−11.1	0.35517	87.0
2.16000	0.41158	84.7	0.23428	−8.1	0.217772	−8.9	0.39579	84.6
2.28000	0.43738	80.1	0.23007	−9.9	0.208548	−7.7	0.42343	81.2
2.40000	0.46035	77.1	0.21704	−11.7	0.201611	−5.7	0.45105	78.6

Diagram 9.4:
S Parameters First Mixer Local Oscillator Input LO1/LO1X

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.18000	0.91927	−5.7	0.06317	31.2	0.064323	33.4	0.92220	−6.1
0.27000	0.91601	−8.6	0.07342	38.8	0.077420	41.1	0.91846	−9.3
0.36000	0.90857	−11.5	0.08655	44.9	0.093003	46.9	0.90983	−12.5
0.45000	0.90053	−14.5	0.10133	48.8	0.111080	49.2	0.89859	−15.8
0.54000	0.89330	−17.6	0.11802	50.4	0.129258	50.0	0.88882	−19.0
0.63000	0.88553	−20.8	0.13434	51.0	0.148203	49.6	0.87743	−22.4
0.72000	0.87500	−23.9	0.15117	50.5	0.166500	48.3	0.86539	−25.8
0.81000	0.86598	−27.3	0.16727	49.0	0.184574	46.4	0.85357	−29.1
0.90000	0.85542	−30.6	0.18218	47.2	0.199612	44.1	0.84010	−32.7
0.99000	0.84298	−34.2	0.19576	45.6	0.215129	41.4	0.82709	−36.3
1.08000	0.83289	−37.6	0.20782	43.3	0.228460	38.6	0.81336	−39.9
1.17000	0.82146	−41.1	0.21942	41.1	0.240106	35.7	0.80065	−43.4
1.26000	0.81124	−44.4	0.22840	39.0	0.248419	32.8	0.78694	−46.9
1.35000	0.80184	−47.8	0.23587	36.7	0.255844	29.6	0.77285	−50.2
1.44000	0.79156	−51.1	0.24163	34.5	0.261942	26.8	0.76010	−53.6
1.53000	0.78188	−54.4	0.24690	32.5	0.265680	23.8	0.74681	−56.8
1.62000	0.77115	−57.5	0.25018	30.7	0.267054	20.8	0.73190	−60.0
1.71000	0.76168	−60.6	0.25256	29.0	0.266984	18.0	0.71652	−62.9
1.80000	0.75013	−63.6	0.25551	27.7	0.266617	15.8	0.70176	−65.7
1.89000	0.74337	−66.5	0.25844	26.2	0.263411	12.7	0.68508	−68.5
1.98000	0.73338	−69.7	0.26043	24.6	0.260051	10.1	0.67025	−71.2
2.07000	0.72066	−72.5	0.26090	23.3	0.252836	7.7	0.65370	−73.8
2.16000	0.70873	−76.0	0.26058	21.9	0.245740	5.4	0.63540	−76.6
2.25000	0.69207	−79.1	0.26117	20.4	0.236150	3.2	0.61491	−79.5
2.34000	0.67605	−82.6	0.25994	19.5	0.226954	2.0	0.59347	−82.5
2.43000	0.65687	−86.4	0.25987	18.3	0.216999	0.4	0.56871	−86.0
2.52000	0.63462	−90.3	0.25857	17.6	0.207094	−0.9	0.54045	−89.6

Diagram 9.5:
S Parameters First Mixer Output MO/MOX

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.03000	0.99719	−0.6	0.00459	33.3	0.004033	45.3	0.99600	−0.6
0.06000	0.99758	−1.2	0.00562	59.7	0.006612	64.3	0.99659	−1.3
0.09000	0.99715	−1.9	0.00695	73.0	0.009555	74.7	0.99646	−2.0
0.12000	0.99715	−2.5	0.00911	77.1	0.012983	78.3	0.99659	−2.6
0.15000	0.99588	−3.2	0.01152	84.4	0.016260	82.3	0.99531	−3.3
0.18000	0.99380	−3.8	0.01485	94.0	0.019141	84.4	0.99369	−3.9
0.21000	0.99065	−4.4	0.01749	94.9	0.022643	85.4	0.99317	−4.6
0.24000	0.98853	−5.1	0.02132	99.0	0.026705	87.3	0.99238	−5.4
0.27000	0.98808	−5.5	0.02469	97.8	0.029340	87.3	0.99113	−6.0
0.30000	0.98701	−6.1	0.02878	97.5	0.033407	86.8	0.98882	−6.6
0.33000	0.98341	−6.8	0.03365	98.7	0.037011	87.3	0.98722	−7.4
0.36000	0.98035	−7.4	0.03774	98.5	0.041449	87.6	0.98546	−8.0
0.39000	0.97882	−7.9	0.04138	97.8	0.045975	86.9	0.98444	−8.6
0.42000	0.97643	−8.6	0.04569	96.1	0.049833	87.0	0.98117	−9.4
0.45000	0.97703	−9.2	0.05006	95.1	0.054043	85.7	0.98180	−9.9
0.48000	0.97426	−9.8	0.05463	94.4	0.057552	86.0	0.97988	−10.7
0.51000	0.97320	−10.4	0.05871	93.3	0.061744	85.1	0.97713	−11.5
0.54000	0.97049	−11.0	0.06315	92.2	0.065453	84.1	0.97534	−12.2
0.57000	0.97025	−11.7	0.06697	91.3	0.069334	83.5	0.97452	−12.8
0.60000	0.96768	−12.4	0.07028	89.7	0.072912	82.7	0.97167	−13.6

Diagram 9.6:
S Parameters PGC IF Signal Input IFI/IFIX

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.03000	0.15954	145.5	0.19307	25.1	0.192654	25.2	0.13415	139.3
0.06000	0.16114	117.0	0.26459	28.9	0.266046	29.2	0.14626	107.4
0.09000	0.15718	94.2	0.32046	25.0	0.321280	24.9	0.15169	84.6
0.12000	0.15338	77.8	0.35581	20.6	0.354433	20.6	0.15610	69.3
0.15000	0.15126	65.1	0.37844	16.4	0.375977	16.8	0.15776	58.5
0.18000	0.14784	55.4	0.39303	12.8	0.389353	13.8	0.15987	50.7
0.21000	0.14444	47.5	0.40053	9.8	0.398930	11.1	0.16224	44.9
0.24000	0.14151	41.5	0.40433	7.2	0.406531	8.8	0.16332	39.9
0.27000	0.13825	36.9	0.40592	4.9	0.412252	6.8	0.16485	35.6
0.30000	0.13581	33.9	0.40721	3.2	0.416247	5.0	0.16533	32.0
0.33000	0.13253	31.3	0.40670	1.7	0.419099	3.2	0.16489	29.4
0.36000	0.13145	28.9	0.41043	0.7	0.421127	1.5	0.16320	26.7
0.39000	0.12935	27.5	0.40710	−0.8	0.421983	0.1	0.16205	24.3
0.42000	0.12678	26.1	0.40656	−1.9	0.422372	−1.3	0.16058	22.8
0.45000	0.12607	24.4	0.40636	−3.0	0.421432	−2.7	0.15882	21.1
0.48000	0.12543	23.0	0.40641	−3.9	0.421485	−3.9	0.15490	19.4
0.51000	0.12491	22.4	0.40577	−4.9	0.420387	−4.9	0.15353	18.3
0.54000	0.12290	21.4	0.40545	−5.8	0.419516	−6.0	0.15125	17.4
0.57000	0.12181	20.4	0.40487	−6.7	0.417551	−7.0	0.14924	16.8
0.60000	0.12060	18.5	0.40454	−7.6	0.416237	−7.9	0.14581	15.6

Diagram 9.7:
S Parameters VCO (as Amplifier) Second Local Oscillator Input LO2/LO2X

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.06000	0.91728	−1.6	0.04815	7.6	0.048228	7.1	0.91633	−1.8
0.09000	0.91500	−2.5	0.04741	10.8	0.047301	10.8	0.91509	−2.7
0.12000	0.91272	−3.3	0.04769	15.9	0.047700	15.1	0.91205	−3.5
0.15000	0.91025	−4.0	0.04904	20.5	0.048758	19.0	0.90924	−4.4
0.18000	0.90877	−4.8	0.05061	24.2	0.049913	23.7	0.90802	−5.2
0.21000	0.90584	−5.6	0.05294	28.5	0.052925	26.8	0.90583	−6.2
0.24000	0.90353	−6.4	0.05551	31.2	0.055658	30.0	0.90332	−6.9
0.27000	0.90132	−7.1	0.05836	34.0	0.058649	32.7	0.90051	−7.7
0.30000	0.89965	−7.8	0.06233	37.0	0.061103	35.0	0.89753	−8.5
0.33000	0.89621	−8.6	0.06651	39.3	0.065708	37.7	0.89477	−9.4
0.36000	0.89233	−9.3	0.07062	40.6	0.070187	38.7	0.89115	−10.2
0.39000	0.89022	−10.1	0.07552	42.1	0.073967	39.8	0.88900	−11.0
0.42000	0.88687	−10.8	0.08009	43.0	0.078695	40.5	0.88574	−11.9
0.45000	0.88368	−11.7	0.08538	43.2	0.083168	41.8	0.88100	−12.7
0.48000	0.88110	−12.4	0.09067	43.7	0.088625	41.7	0.88077	−13.5
0.51000	0.87852	−13.2	0.09541	43.7	0.092739	42.0	0.87602	−14.3
0.54000	0.87421	−13.9	0.10098	43.7	0.097744	41.8	0.87183	−15.2
0.57000	0.87101	−14.6	0.10573	43.5	0.103285	41.4	0.87057	−16.0
0.60000	0.86780	−15.4	0.11129	43.1	0.107551	41.1	0.86655	−17.0
0.63000	0.86541	−16.2	0.11622	42.7	0.112417	40.3	0.86177	−17.7
0.66000	0.86172	−17.0	0.12210	41.8	0.117785	39.8	0.85914	−18.7
0.69000	0.85712	−17.7	0.12698	41.1	0.122172	39.2	0.85634	−19.5
0.72000	0.85350	−18.6	0.13215	40.1	0.127186	38.3	0.85041	−20.5
0.75000	0.85005	−19.4	0.13766	39.3	0.132210	37.2	0.84845	−21.2
0.78000	0.84664	−20.2	0.14246	38.3	0.136839	36.4	0.84513	−22.3
0.81000	0.84489	−21.1	0.14807	37.1	0.141312	35.2	0.84043	−23.0
0.84000	0.83946	−21.9	0.15293	36.1	0.146257	34.4	0.83646	−23.9
0.87000	0.83599	−22.8	0.15759	35.1	0.150917	33.0	0.83313	−24.9
0.90000	0.83175	−23.5	0.16194	33.7	0.155108	32.1	0.83029	−25.7
0.93000	0.82696	−24.3	0.16704	32.6	0.160036	30.6	0.82608	−26.6
0.96000	0.82505	−25.2	0.17213	31.3	0.165208	29.4	0.82192	−27.4
0.99000	0.82177	−25.9	0.17703	30.1	0.169104	28.2	0.81795	−28.4