SIEMENS

ICs for Communications

RF/IF Double PLL Frequency Synthesizer

PMB 2347 Version 1.1

Preliminary Specification 05.99

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PMB 2347 **Revision History:** **Current Version: 08.98**		
Previous Version:		
old Page	new Page	Subjects (major changes since last revision)

Table of Contents **Page**

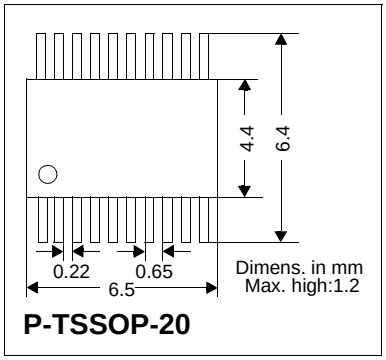
SIEMENS

RF/IF Double PLL Frequency Synthesizer **PMB 2347**

Version 1.1 **BiCMOS IC**

1 Overview

The PMB 2347 is a RF/IF double PLL frequency synthesizer implemented in Siemens' high speed BiCMOS technology B6HFC. The device contains two PLLs with integrated prescalers especially designed for use in battery powered radio equipment and mobile telephones. Primary applications are single- and dual-band digital cellular systems e.g. GSM, PCN (DCS 1800) and PCS systems.



P-TSSOP-20

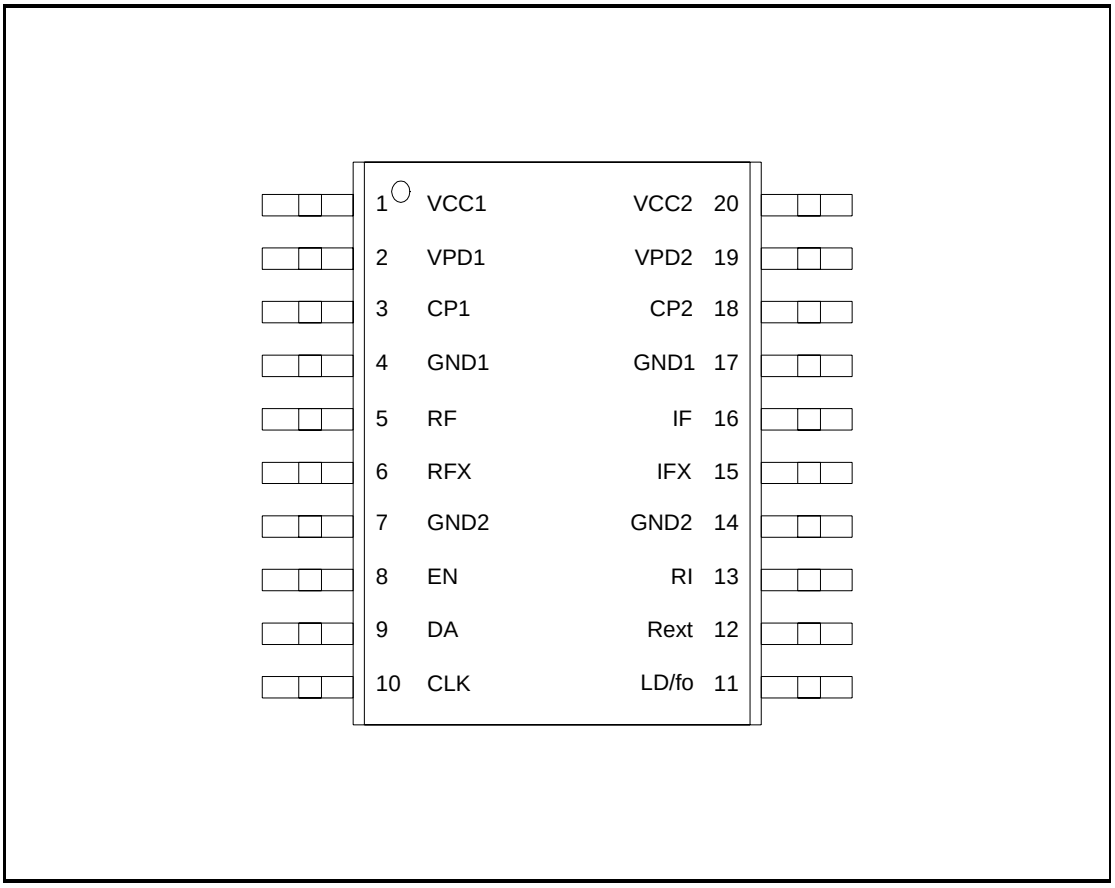
1.1 Features

- Operation range 2.7 to 5.0 V
- Low operating current consumption
- Programmable power down modes
- High input sensitivity and high input frequencies:
  PLL1 (RF): 2.8 GHz PLL2 (IF): 500 MHz
- Programmable dual modulus prescaler divide ratio:
  PLL1: 1:64/65 or 1:32/33 PLL2: 16/17 or 1:8/9
  Dividing ratios:
  A counters: PLL1: 0 to 63 PLL2: 0 to 15
  N counters: PLL1: 3 to 16,383 PLL2: 3 to 16,383
  R counters 3 to 16,383 for PLL1 and PLL2
- Fast phase detectors and charge pump outputs without dead zone
- High phase noise performance
- Switchable polarity and programmable phase detector currents
- External reference current setting for PD outputs
- Fast serial 3-wire bus interface with low threshold voltage Schmitt-Trigger inputs for interfacing with low voltage baseband circuits
- Two data registers in PLL2 for fast IF band switching
- A programmable multi-functional output port for lock detect (quasidigital lock detect) and test mode

Type	Ordering Code	Package
PMB 2347		P-TSSOP-20

1.2 Pin Configuration

(top view)

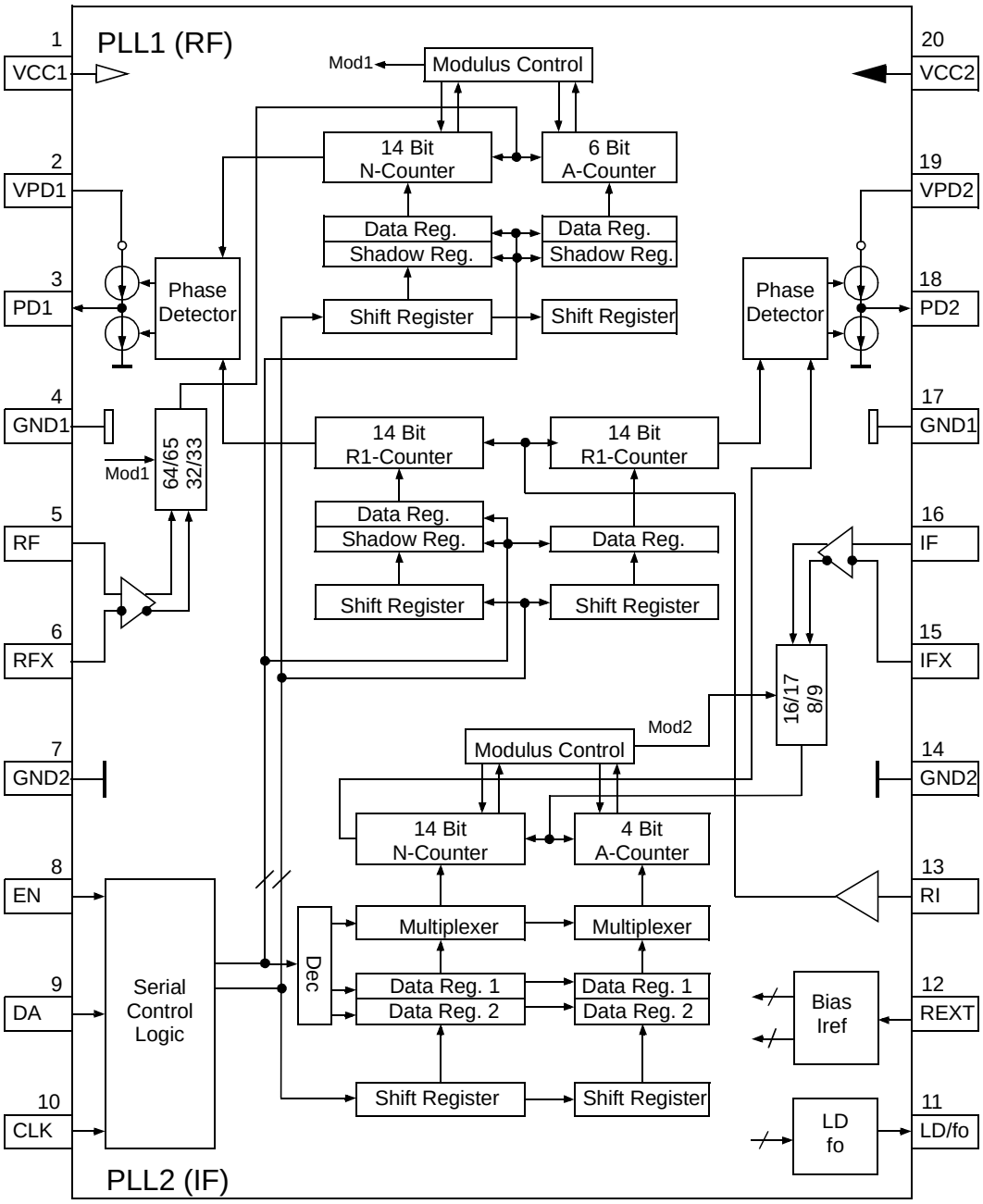


P-TSSOP-20

1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
1	VCC1	Positive supply voltage for CMOS circuitry
2	VPD1	Positive supply voltage for charge pump of PLL1
3	CP1	**PLL1 charge pump output** Phase detector tristate charge pump output
4	GND1	Ground for CMOS circuitry
5	RF1	**RF frequency input 1** RF input with highly sensitive preamplifier for PLL1. AC coupling must be set up.
6	RFX	**RF frequency input (inverted)** RF input with highly sensitive preampifier for PLL1. AC coupling must be set up
7	GND1	Ground for bipolar circuitry
8	EN	**3-Wire bus input: Enable** Enable input of the serial control interface with Schmitt-Trigger input stage. When EN=H the input signals CLK and DA are disabled. When EN=L the serial control interface is enabled. The received data are transferred to the registers with the positive edge of the EN-signal.
9	DA	**3-Wire bus input: Data** Data input of the serial control interface with Schmitt-Trigger input stage.The serial data are read into the internal shift register with the positive edge of CLK.
10	CLK	**3-Wire bus input: Clock** Clock input of the serial control interface with Schmitt-Trigger input stage
11	LD/fo	**Lock detector output** Unipolar output of the phase detector in the form of a pulse-width modulated signal. In the locked state the output signal is at H-level. In standby mode the output is resistive. For test purpose the push pull output fo is enabled.
12	Rext	**CP& Prescaler reference current setting** External resistor for CP & Prescaler reference current setting.
13	RI	**Reference frequency input** Input with highly sensitive preamplifier. With small input signals AC coupling must be set up, where DC coupling can be used for large input signals.
14	GND2	Ground for bipolar circuitry
15	IFX	**IF frequency input (inverted)** IF input with highly sensitive preampifier for PLL2. AC coupling must be set up.
16	IF	**IF frequency input** IF input with highly sensitive preampifier for PLL2. AC coupling must be set up.
17	GND1	Ground for CMOS circuitry
18	CP2	Phase detector tristate charge pump output for PLL2
19	VPD2	Positive supply voltage for charge pump 2.
20	VCC2	Positive supply voltage for bipolar circuitry

1.4 Functional Block Diagram



P-TSSOP-20

1.5 Circuit Description

General Description

The PMB 2347 consists of two fully programmable PLLs, one for the RF and one for the IF frequency range. Each PLL contains a high frequency dual modulus prescaler, an A- and a N-counter with dual modulus control logic, a reference- (R-) counter, and a phase detector with charge pump output. The two synthesizers are controlled via the common serial 3-wire interface.

The reference frequency is applied at the common RI-input and divided by the R-counter of each PLL. Its maximum value is 45 MHz. The RF and IF input frequencies will be divided by the corresponding prescalers with a programmable 32/32 or 64/65 (RF) and 8/9 or 16/17 (IF) divide ratio and the following programmable A/N-counters. The maximum RF frequency value is 2.8 GHz and 500 MHz for the IF frequency.

The phase and frequency detectors with the charge pumps have a linear operating range without a dead zone for very small phase deviations.

The multifunctional output port LD/fo can be programmed as lock detector and test output.

Programming

Programming of the IC is done via the serial data interface. The content of the bus telegram (serial data format) is assigned to the functional units according to the address.

The most significant bit (MSB) of the serial data formats is shifted first.

The *short control data format* allows a fast PD-current change.

The *long control data format* allows the programming of asynchronous or synchronous data acquisition of PLL1 (RF), 4 different PD-output current modes for the PLL1 and 1 PD-output current modes for PLL2, polarity setting of the PD-output signals, 2 standby modes, charge pump pulse width and the prescaler divide ratio.

The *A/N-counter data format* of PLL1 contains the A/N-counter value.. The data format of PLL2 comprise the counter values as well.

The *R-counter data format* contains the R-counter values.

The PLL1 (RF) of PMB 2347 offers the possibility of synchronous counter and charge pump current programming to avoid phase errors at the phase detector when R- **and** A-/N-counter are programmed one after another or the charge pump current is altered.

Asynchronous Mode:

The serial data is written directly to the data registers of the addressed counter with the Enable pulse. As each counter is loading the new starting value after it is decremented to „zero“, the counters changes therefore their counter values asynchronously to the others.

Synchronous Mode (only for RF):

In this mode counter programming is controlled by the R- and N-counters. The serial data (exception: higher part of long control data format) is first written with the Enable pulse to the corresponding shadow registers. From there the values for R-counter, A-/N-counter and charge pump current values of short/long control data format are loaded into the corresponding data register when the N-counter reaches „zero+1“. Therefore the change of all counter states is synchronised to the reloading of the N-counter to avoid additional phase error caused by the programming. The transfer of the charge pump current values into the corresponding data register is tied to the N-counter loading, but follows the loading of the N-data register in the distance of one N-counter dividing ratio. This guarantees that a new PD-current value becomes valid at the same time when the counters are loaded with the new data.

Synchronous programming sequence:

1.Setting of synchronous counter programming by bit c13 of long control data format.

2.Programming of the R-counter, and optional short control data format. With the Enable signal data is loaded into the shadow registers.

3.Programming of the A/N-counter. Data is loaded into shadow registers, the EN-signal starts the synchronous transfer to the data registers.

Synchronous data programming is of especial advantage, when large frequency steps are to be made in a short time. For this purpose a high reference frequency can be programmed in order to achieve rapid – “rough” – transient response. This method increases the fundamental frequency by nearly the square root of the reference frequency ratio and therefore the settling time is reduced. When rough lock is achieved, another synchronous data transfer is needed to switch back to the original channel spacing. A “fine” lock in will finish the total step response. It may not be necessary to change reference frequency, but it make sense to perform synchronous data acquisition in any case. Especially for GSM, PCN (DCS 1800) and PCS systems the synchronous mode should be used to achieve best performance of the PMB 2347.

Standby Condition (power down)

Each PLL of the PMB 2347 has two programmable standby modes to reduce the current consumption (standby 1, standby 2).

Standby 1: The corresponding PLL is switched off, the current consumption is reduced below 1 µA.

Standby 2: The corresponding counters, the charge pump and the outputs are switched off. Only the preamplifier of RI-input stays active. **(See standby table)**

Divide ratio programming

The frequency of an external VCO controlled by the PMB 2347 is given below:

$$f_{VCO} = [(P \cdot N) + A] \cdot \frac{f_{RI}}{R} = \frac{M}{R} \cdot f_{RI}$$

with $A \leq N$.

f_{VCO}:	frequency of the external VCO
f_{RI}:	reference frequency
N:	divide ratio of the N-counter
A:	divide ratio of the A-swallow counter
P:	divide ratio of the prescaler
R:	divide ratio of the R-counter
M=P*N+A:	total divide ratio

Note: for continuous frequency steps following condition is necessary

$$[P \cdot N + A] \geq P \cdot (P - 1)$$

Prescaler Divide Ratio

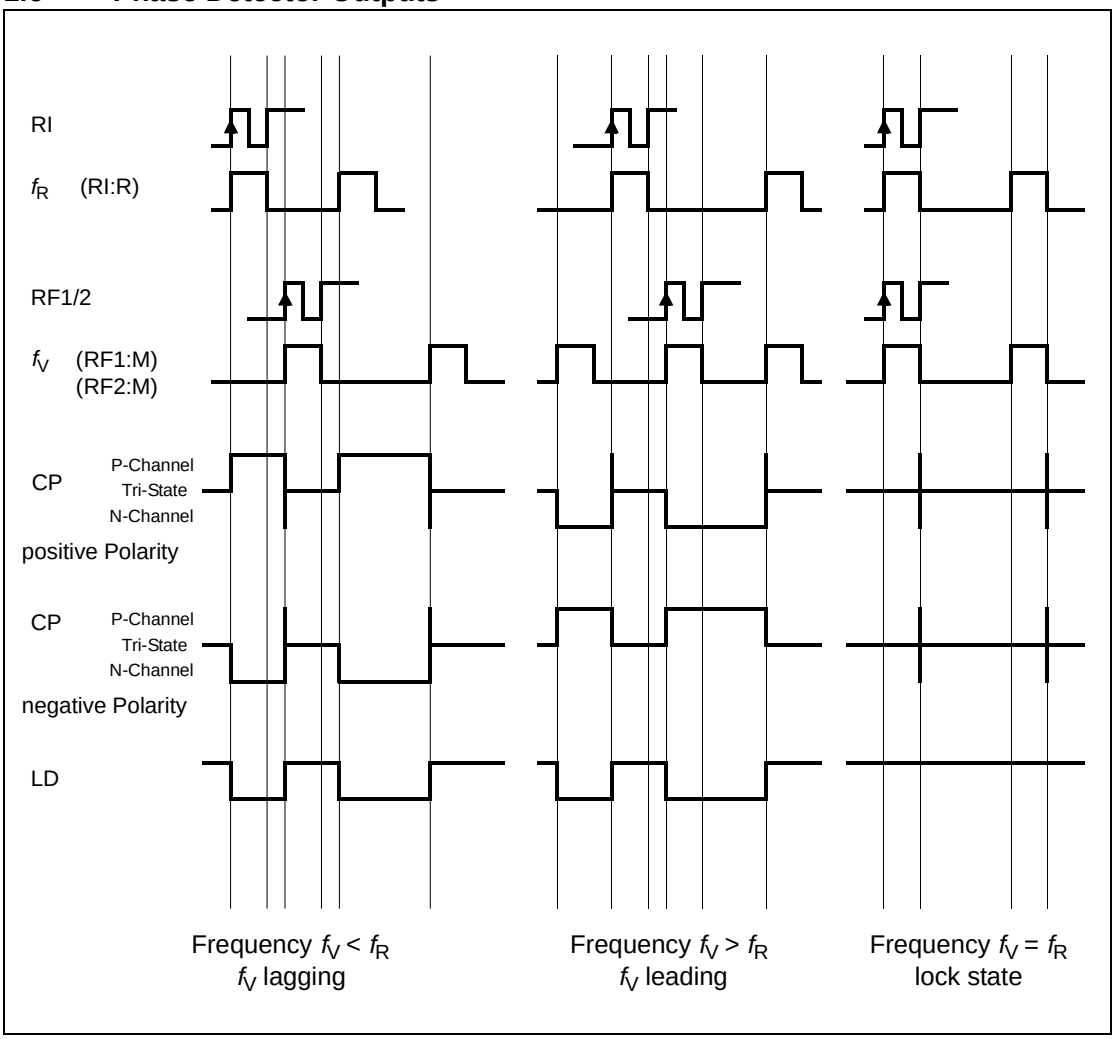
For the highest input frequencies of the prescalers the larger divide ratio is necessary:
RF-PLL:64/65 for frequencies greater 1500 MHz
IF-PLL:16/17 for frequencies greater 375 MHz

Fast wake-up programming

When the circuit is connected to the supply voltage all registers are undefined. Due to the fact that each counter is loading its new start value after it is decremented to „zero“, the start-up time of the counters with the programmed values is too long for some applications. If the counters are programmed in standby mode 2 and the PLLs are switched afterwards in operating mode, the counters are starting immediatly with the programmed values. Therefore following data transfer sequence is recommended:

Fast Wake Up Data Transfer Sequence	
Step	**Serial Data Transfer Sequence**
1	Long Control Word: Asynchronous Mode, Standby2
2	R-Counter
3	A-/N-Counter
4	Long Control Word: Synchronous Mode, Operating Mode

1.6 Phase Detector Outputs



The timing diagram is valid for PLL1and PLL2.

1.7 Serial Control Data Formats

Address of Data Formats

Address			Data Format	Addressed PLL
a2	a1	a0		
0	0	0	Short Control Data Format	PLL1 (RF)
0	1	0	Long Control Data Format	PLL1 (RF)
1	0	0	A-/N-Counter	PLL1 (RF)
1	1	0	R-Counter	PLL1 (RF)
0	0	1	Short Control Data Format	PLL2 (IF)
0	1	1	Long Control Data Format	PLL2 (IF)
1	0	1	A-/N-Counter	PLL2 (IF)
1	1	1	R-Counter	PLL2 (IF)

In general each PLL can independently be addressed without affecting the other PLL (See also Test Modes).
NOTE: MSB of all serial data is shifted first

Short Control Data Formats

PLL1			
Bit		Bit	Function
LSB 0	0	a0	Address
1	0	a1	Address
2	0	a2	Address
3		c0	LD InActive
4		c1	CP current 2
5		c2	CP current 1
6 MSB		c3	PLLSel

PLL2			
Bit		Bit	Function
LSB 0	1	a0	Address
1	0	a1	Address
2	0	a2	Address
3		c0	reserved
4		c1	reserved
5		c2	CP current
6 MSB		c3	reserved

Long Control Data Formats

PLL1			
Bit		Bit	Function
LSB 0	0	a0	Address
1	1	a1	Address
2	0	a2	Address
3		c0	reserved
4		c1	CP current 2
5		c2	CP current 1
6		c3	PLLSel
7		c4	PSC Div. Ratio
8		c5	reserved
9		c6	CPP width 2
10		c7	CPP width 1
11		c8	standby 2
12		c9	standby 1
13		c10	CP polarity
14		c11	Mode 2
15		c12	Mode 1
16 MSB		c13	Sync/Async Mode

PLL2			
Bit		Bit	Function
LSB 0	1	a0	Address
1	1	a1	Address
2	0	a2	Address
3		c0	reserved
4		c1	reserved
5		c2	CP current 1
6		c3	reserved
7		c4	PSC Div. Ratio
8		c5	reserved
9		c6	CPP width 2
10		c7	CPP width 1
11		c8	standby 2
12		c9	standby 1
13		c10	CP polarity
14		c11	reserved
15		c12	reserved
16 MSB		c13	reserved

A/N-counter Data Formats

PLL1			
Bit		**Bit**	**Function**
LSB 0	0	a0	Address
1	0	a1	Address
2	1	a2	Address
3	LSB	n0	N1-Counter
4		n1	
5		n2	
6		n3	
7		n4	
8		n5	
9		n6	
10		n7	
11		n8	
12		n9	
13		n10	
14		n11	
15		n12	
16	MSB	n13	
17	LSB	ac0	A1-Counter
18		ac1	
19		ac2	
20		ac3	
21		ac4	
22	MSB	ac5	

PLL2			
Bit		**Bit**	**Function**
LSB 0	1	a0	Address
1	0	a1	Address
2	1	a2	Address
3	LSB	n0	N2-Counter
4		n1	
5		n2	
6		n3	
7		n4	
8		n5	
9		n6	
10		n7	
11		n8	
12		n9	
13		n10	
14		n11	
15		n12	
16	MSB	n13	
17	LSB	ac0	A2-Counter
18		ac1	
19		ac2	
20	MSB	ac3	

R-counter Data Formats

PLL1			
BitNo		**Bit**	**Function**
LSB 0	0	a0	Address
1	1	a1	Address
2	1	a2	Address
3	LSB	r0	R1-Counter
4		r1	
5		r2	
6		r3	
7		r4	
8		r5	
9		r6	
10		r7	
11		r8	
12		r9	
13		r10	
14		r11	
15		r12	
16 MSB	MSB	r13	

PLL2			
BitNo		**Bit**	**Function**
LSB 0	1	a0	Address
1	1	a1	Address
2	1	a2	Address
3	LSB	r0	R2-Counter
4		r1	
5		r2	
6		r3	
7		r4	
8		r5	
9		r6	
10		r7	
11		r8	
12		r9	
13		r10	
14		r11	
15		r12	
16 MSB	MSB	r13	

Function Tables:

Programming of Operation and Test Modes				
c12 Mode 1	**c11 Mode2**	**c3 PLLSel**	**Functional Mode**	**Affected Output: Pin11 = BSW/LD**
0	0	0	Test 1	fvn1 (PLL1)
1	0	0	Test 2	frn1 (PLL1)
0	1	0	reserved	frn1 (PLL1)
1	1	0	NORMAL OPERATION, LD of PLL1 active	Lock Detect PLL 1
0	0	1	Test 3	fvn2 (PLL2)
1	0	1	Test 4	frn2 (PLL2)
0	1	1	reserved	frn2 (PLL2)
1	1	1	NORMAL OPERATION, LD of PLL2 active	Lock Detect PLL 2

Programming of CP Current of PLL1			
c2 CP current1	**c1 CP current2**	**CP Current [mA]**	**Remark**
0	0	1.2 mA	with 100µA reference current
1	0	2.0 mA	
0	1	2.8 mA	
1	1	4.0 mA	

Programming of CP Current of PLL2			
c2 CP current1		**CP Current [mA]**	**Remark**
0		Tristate	with 100µA reference current
1		1.0 mA	

Programming of Charge Pump Pulse Width of both PLLs			
c7 CPP Width 1	**c6 CPP Width 2**	**Pulse Width [ns] typ.**	**Remark**
0	0	1.6 ns	
1	0	6.0 ns	
0	1	9.0 ns	
1	1	13.0 ns	

Standby or Power Down Programming of both PLLs					
Control Bits		**Mode**	**Affected Output Pins** Z: High Impedance (Tristate)		
c9 standby1	**c8 standby2**		**Pin11 LD/fo**	**Pin3 CP1**	**Pin18 CP2**
0	0	standby1	off	Z	Z
1	0	standby2	off	Z	Z
0	1	standby1	off	Z	Z
1	1	Operation Mode	active	active	active

Programming of Syncronous/Asyncronous Mode of PLL1	
c13 Sync/Async	**Syncronous/Asyncronous Mode**
0	Asynchronous Mode of PLL 1
1	Synchronous Mode of PLL 1

Programming of PD Polarity of both PLLs	
Control Bit	**PD Polarity**
c10 PD Polarity	
0	negative Polarity
1	positive Polarity

Programming of Prescaler Divide Ratio of both PLLs		
Control Bit	**Prescaler Divide Ratio**	
c4 PSC Div. Ratio		
0	PLL1: 32/33	PLL2: 8/9
1	PLL1: 64/65	PLL2: 16/17

Programming of PLL Select	
Control Bit	**PLL Select**
c3 of PLL1	
0	PLL1 (RF)
1	PLL2 (IF)

Programming of Data Register Select	
Control Bits	**IF Data Register Select**
c3 of PLL2	
0	Data register 1
1	Data register 2

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, due to permanent damage to the device.

Parameter	Symbol	Limit Values		Units	Remarks
		Min	Max		
Supply Voltage	$V_{CC1/2}$	-0.3	5.5	V	
Input Voltage	V_I	-0.3	$V_{CC1/2}$+0.3	V	
Output Voltage	V_O	GND	$V_{CC1/2}$	V	
Total power dissipation	P_{tot}		300	mW	
Ambient temperature	T_A	-40	85	°C	in operation
Storage temperature	T_{Stg}	-50	125	°C	
Thermal Resistance	R_{thJA}		170	K/W	
ESD Integrity (according to MIL 883 Method 3015.7)	V_{ESD}			KV	

2.2 Operational Range

Within the operational range the IC operates as described in the circuit description.
The AC/DC characteristic limits are not guaranteed.

Supply voltage $V_{CC1/2}$ = 2.7V...5.0V, Ambient temperature T_{amb} = -40°C...85°C Typical

Parameter	Symbol	Limit Values		Units	
		Min	Max		
Supply Voltage	$V_{CC1/2}$	2.7	5.0	V	
Input frequency RF	f_{RF}	250	2800	MHz	$V_{CC1/2}$ = 3.6V
Input frequency IF	f_{IF}	100	500	MHz	
Input reference frequency	f_{Ri}	1	45	MHz	
CP-output current of PLL1	$/ I_{CP1} /$		4 +20%	mA	
CP-output current of PLL2	$/ I_{CP2} /$		1 +20%	mA	
CP-output voltages	$V_{CP1/2}$	0.5	$V_{PD1/2}$ - 0.5	V	
Ambient temperature	T_A	-40	85	°C	

2.3 Typical Supply Current I_{CC}

Parameter	Symbol	Limit Values			Units	Test Conditions
		Min	Typ	Max		
Supply voltage	$V_{CC1/2}$		3.6		V	R_{EXT} = 12k
Supply current:						Note 1)
PLL1 & PLL2 active	$I_{CC1/2}$		9.5		mA	typical values for preliminary design S1004E1
PLL1 active, PLL2 standby	$I_{CC1/2}$		7.3		mA	
PLL1 standby2, PLL2 active	$I_{CC1/2}$		3.4		mA	'standby1'-current will be below 1uA in design 'PMB2347v1.1'
PLL1 & PLL2 standby 2	$I_{CC1/2}$		379		µA	
PLL1 & PLL2 standby 1	$I_{CC1/2}$		220		µA	

1) f_{RF1} = 900MHz, V_{RF} = 150mVrms, f_{RF2} = 420MHz, V_{RF2} = 150mVrms, f_{RI} = 10MHz, V_{RI} = 150mVrms,
I_{CP1} = 4.0mA, I_{CP2} = 2.0mA, Iref = 100 µA

2.4 AC/DC Characteristics

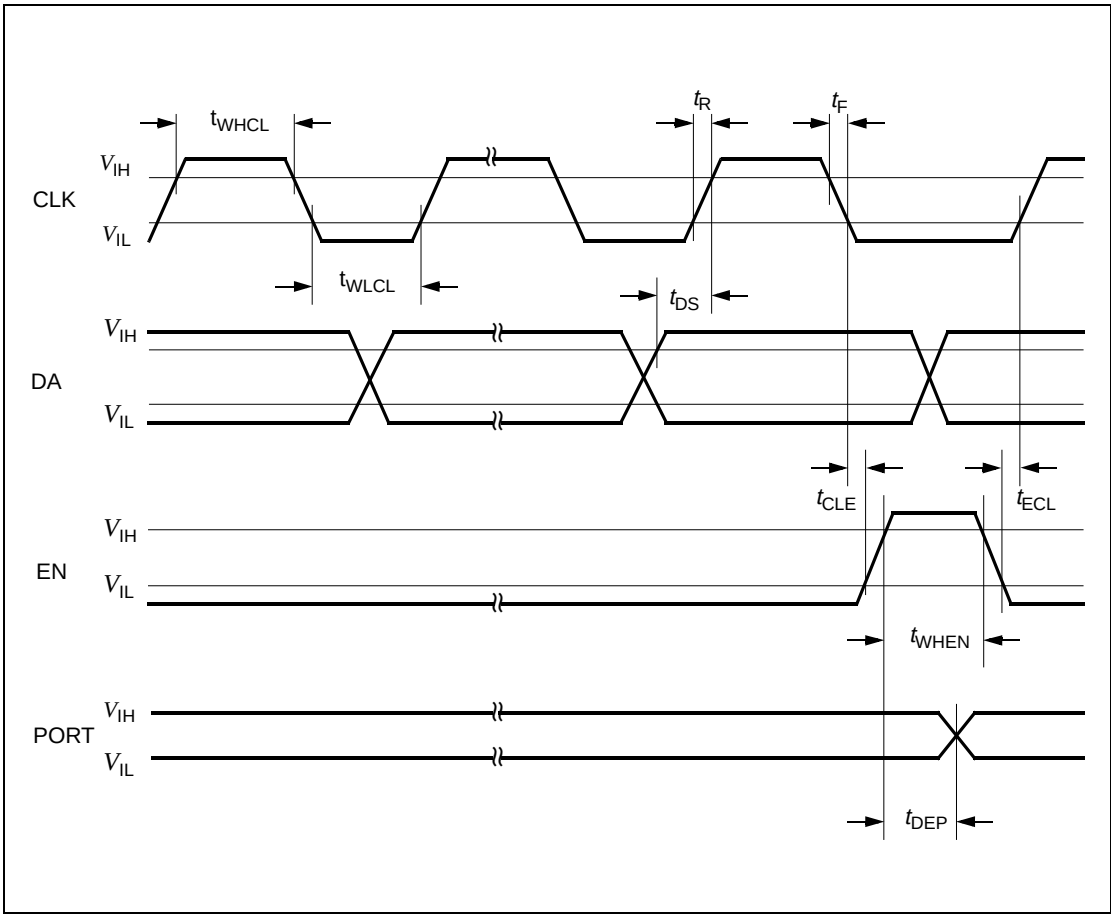
AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Supply voltage $V_{CC1/2}$ = 2.7V...5.0V, Ambient temperature T_{amb} = -40°C to 85°C

Parameter	Symbol	Limit Values			Units	Test Conditions
		Min	Typ	Max		
Input Signals DA, CLK, EN (Schmitt-Trigger input stage)						
H-input voltage	V_{IH}	0.7 V_{CC}		V_{CC}	V	
L-input voltage	V_{IL}			0.3 V_{CC}	V	
Input capacity	C_I			5	pF	
H-input current	I_H			10	µA	V_I = V_{CC2} = 3.6V
L-input current	I_L	-10			µA	V_I = GND
Input Signal RI						
Input voltage	V_I	100			mVrms	f = 4...45MHz, $V_{CC\ 1}$= 3.6V
Slew rate		4			V/µs	V_{CC1} = 2.7...5.0V
Input capacity	C_I			3	pF	
H-input current	I_H			30	µA	V_I = V_{CC1} = 5.0
L-input current	V_I	-30			µA	V_I = GND
Input Signals RF						
Input voltage	V_I				mVrms	f = 150...450MHz,
	P_I	-12		+6	dBm	
Input voltage	V_I				mVrms	f = 450...2500MHz,
	P_I	-20		+4	dBm	
Input voltage	V_I				mVrms	f = 2500...2800MHz,
	P_I	-10		-2.5	dBm	
Input Signals IF						
Input voltage	V_I				mVrms	f = 100...350 MHz,
	P_I	-16		+4	dBm	
Input voltage	V_I				mVrms	f = 350...450 MHz,
	P_I	-25		-5	dBm	
Input voltage	V_I				mVrms	f = 450...600 MHz,
	P_I	-25		-15	dBm	
Output Current *I*CP1						
"1.2 mA"	I_{CP1}	-20%	1.2	+20%	mA	V_{PD1}= 3.6V, V_{CP1} = V_{PD1}/2
"2.0 mA"	I_{CP1}	-20%	2.0	+20%	mA	I_{REF} = 100µA
"2.8 mA"	I_{CP1}	-20%	2.8	+20%	mA	
"4.0 mA"	I_{CP1}	-20%	4.0	+20%	mA	
"Tristate"	$/I_{CP1}/$		0.1	10*)	nA	*) guaranteed by design
Output Current *I*CP2						
"1.0 mA"	I_{CP2}	-20%		+20%	mA	V_{PD2} = 3.6V, V_{CP2} = V_{PD2}/2
						I_{REF} = 100µA
"Tristate"	$/I_{CP2}/$		0.1	10*)	nA	*) guaranteed by design
Magnitude Variation						
"+1.2 mA"	I_{CPMV}		4		%	V_{PD1}= 5V, V_{CP1} = V_{PD1}/2
"+2.0 mA"	I_{CPMV}		4		%	I_{REF} = 100µA
"+2.8 mA"	I_{CPMV}		4		%	
"+4.0 mA"	I_{CPMV}		4		%	see 'Chargepump Specification' for
"-1.2 mA"	I_{CPMV}		6		%	details on spurious suppression
"-2.0 mA"	I_{CPMV}		6		%	
"-2.8 mA"	I_{CPMV}		6		%	
"-4.0 mA"	I_{CPMV}		6		%	

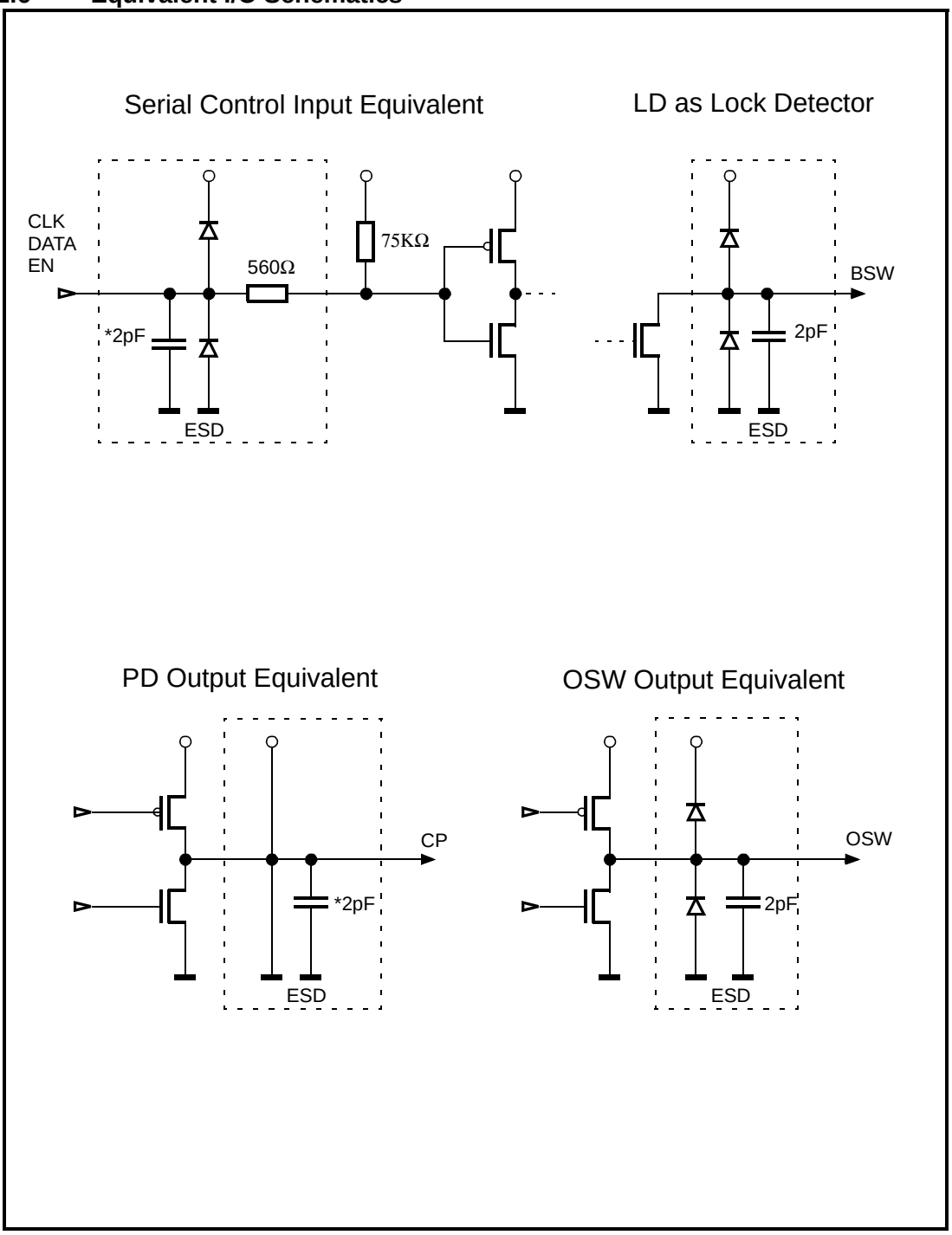
Parameter	Symbol	Limit Values			Units	Test Conditions
		Min	Typ	Max		
Current Mismatch						
"1.2 mA"	I_{CPMM}		0.7		%	V_{PD2}= 5V, V_{CP2} = V_{PD2}/2 I_{REF} = 100µA
"2.0 mA"	I_{CPMM}		1.3		%	
"2.8 mA"	I_{CPMM}		1.8		%	
"4.0 mA"	I_{CPMM}		1.5		%	
Output Rext						
V_{Rext}	V_{Rext}		1.2		V	V_{CC2} = 3.6V, *Rext=12k*
I_{Rext}	I_{Rext}		100		µA	V_{CC2} = 3.6V, *Rext=12k*
Output Signal BSW at BSW/LD-Pin (n-channel open drain)						
L-output voltage	V_{OL}			0.4	V	V_{CC1} = 2.7...3.6V, I_{OL} = 0.3mA
Fall time	t_F		3	10	ns	V_{CC1} = 3.6V,C_l=10pF

2.5 Serial Control Data Format Timing



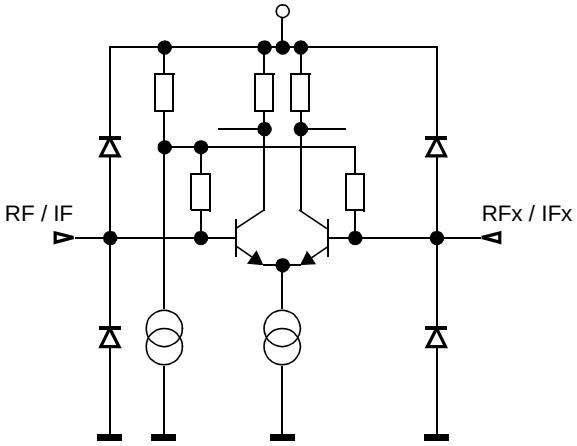
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{CL}		15	MHz
H-pulsewidth (CLK)	t_{WHCL}	30		ns
L-pulsewidth (CLK)	t_{WLCL}	30		ns
Data setup	t_{DS}	20		ns
Setup time Clock-Enable	t_{CLE}	20		ns
Setup time Enable-Clock	t_{ECL}	20		ns
H-pulsewidth (Enable)	t_{WHEN}	60		ns
Rise, fall time	t_R, t_R		10	µs
Propagation delay time EN-PORT	t_{DEP}		1	µs

2.6 Equivalent I/O Schematics

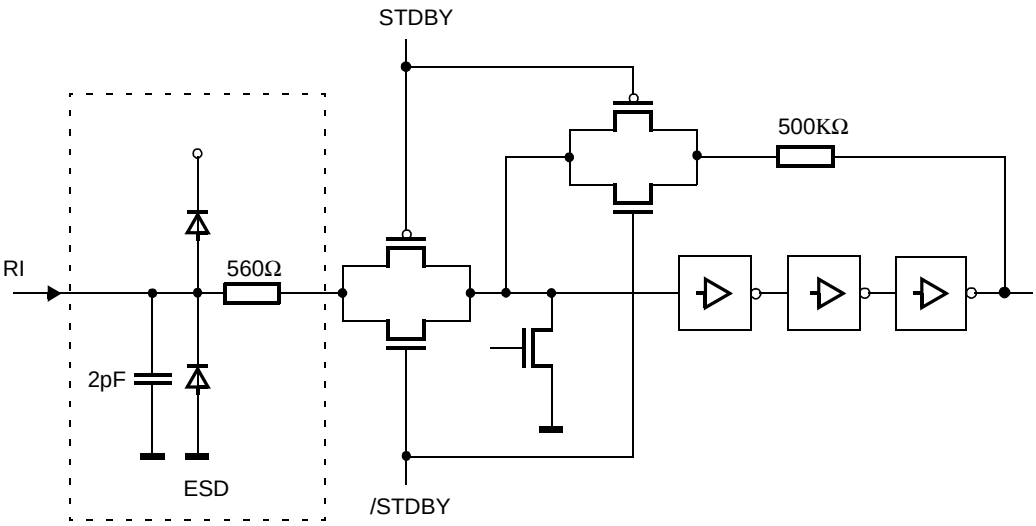


2.7 Equivalent I/O Schematics (continued)

RF and IF Input Equivalent



RI Input Equivalent

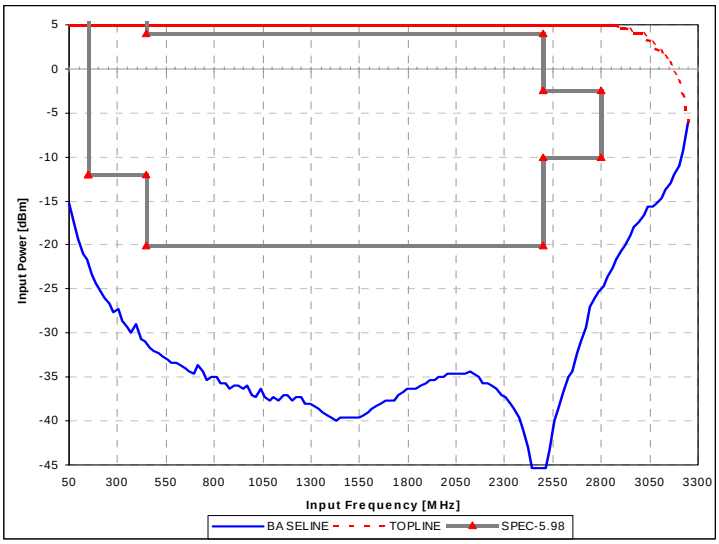


2.8 Input Sensitivities

The following sections show the typical performance at +25'C.

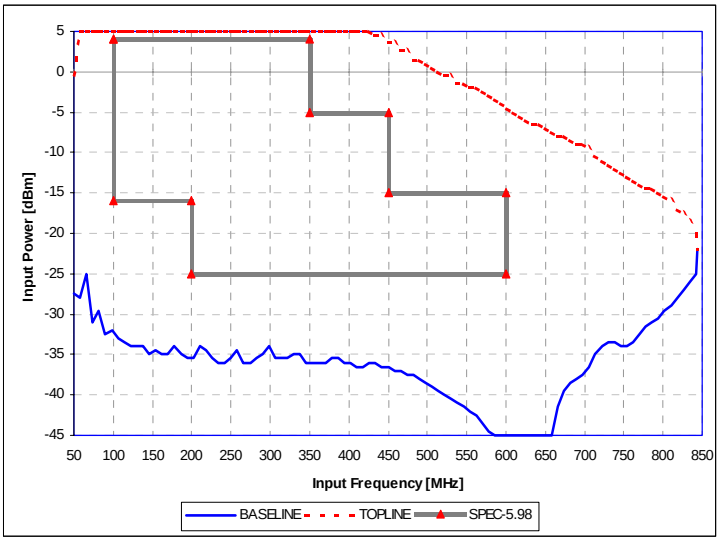
2.8.1 Typical RF Sensitivity

The PLL setup is: Psc:64/65. N:3, A:0, IF-PLL is in standby mode. V_{CC} is 2.7 V. The testport open-drain pin is pulled to 2.0 V over 5k1. The cut-off frequency can be increased to typ. >3.45GHz by using a V_{CC} of 5.0 V;



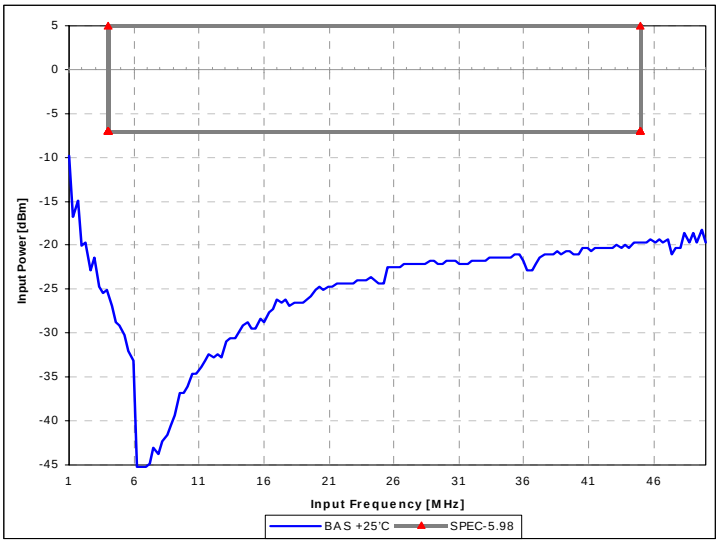
2.8.2 Typical IF Sensitivity

The PLL setup is: Psc:16/17. N:3, A:1, RF-PLL is in standby mode. V_{CC} is 2.7 V. The testport open-drain pin is pulled to 2.0 V over 5k1.



2.8.3 Typical Ri Sensitivity

The PLL setup is: R:3; RF-PLL is in standby mode. V_{CC} is 3.6V. The testport open-drain pin is pulled to 2.0 V over 5k1.



2.9 Charge Pump Currents

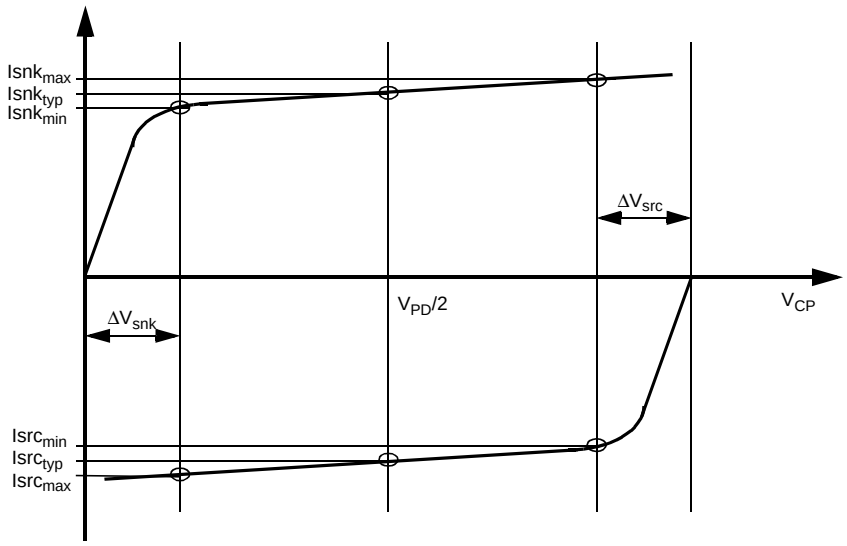


Fig. 1: Definition of Charge Pump Currents

Terms and Abbreviations:

V_{PD}	Supply Voltage of Charge Pump	$\Delta V_{src/snk}$	Offset Voltage from GND or V_{PD}
$Isnk_{max}$	Maximum Sink Current @ V_{PD}-ΔV_{snk}	$Isrc_{max}$	Maximum Source Current @ GND+ΔV_{src}
$Isnk_{typ}$	Typical Sink Current @ $V_{PD}/2$	$Isrc_{typ}$	Typical Source Current @ $V_{PD}/2$
$Isnk_{min}$	Minimum Sink Current @ GND+ΔV_{src}	$Isrc_{min}$	Minimum Source Current @ V_{PD}-ΔV_{snk}

Specification of Charge Pump Characteristics

Charge Pump Output Magnitude Variation CPMV:

$$\frac{\frac{Isnk_{max} - Isnk_{min}}{2}}{\frac{Isnk_{max} + Isnk_{min}}{2}} \cdot 100\% \qquad \frac{\frac{Isrc_{max} - Isrc_{min}}{2}}{\frac{Isrc_{max} + Isrc_{min}}{2}} \cdot 100\%$$

Charge Pump Current Mismatch CPCM:

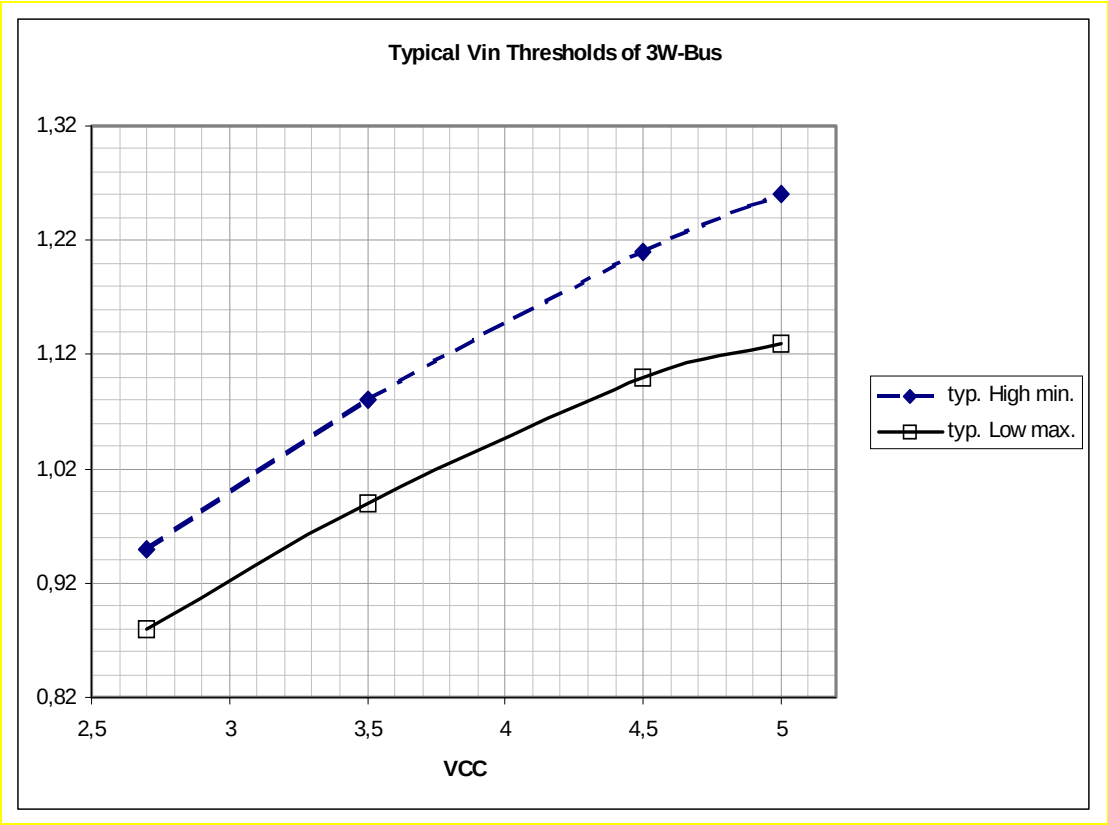
$$\frac{\frac{Isnk_{typ} - Isrc_{typ}}{2}}{\frac{Isnk_{typ} + Isrc_{typ}}{2}} \cdot 100\%$$

Spurious Suppression:

Presuming a standard GSM-application - *RF: 900MHz, PD frequency: 200kHz, Vcc: 2.7V, T_A.: -40...+85'C* - for spurious suppression better than 70dB, it is recommendet that

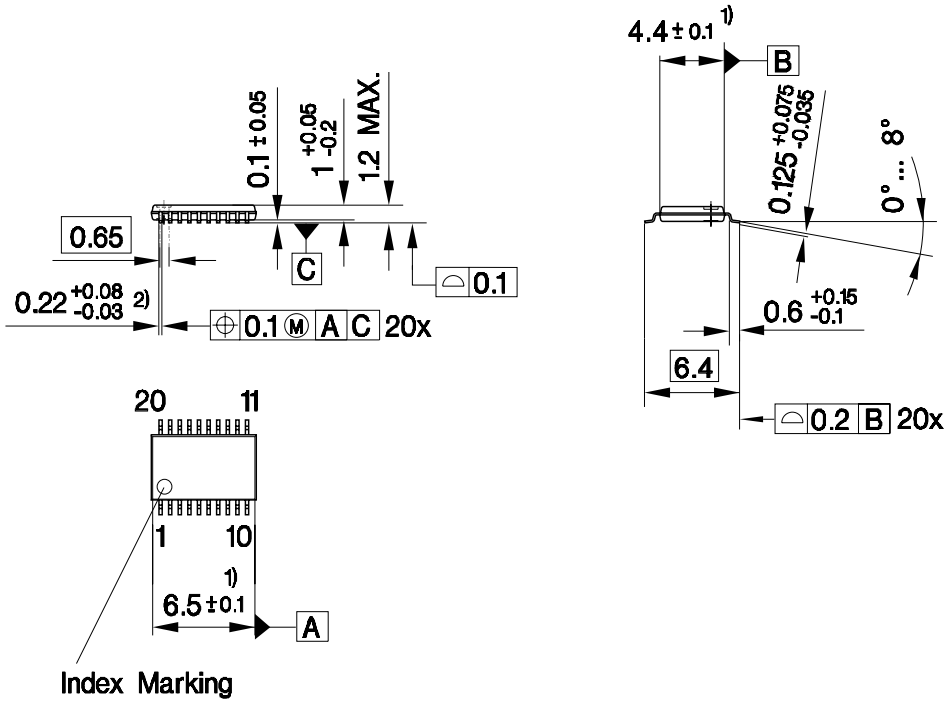
ΔV_{snk} should be less or equal than 0.85 V and ΔV_{src} less or equal than 1.05 V.

2.10 Threshold Voltages of Schmitt-Trigger Input



3 Package Outlines

P-TSSOP-20
(Plastic Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side