



Wireless Components

10-pin Single PLL

PMB 2341 Version 1.0

Specification October 1999

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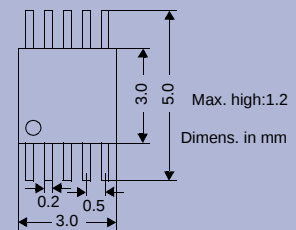
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Productinfo

General Description

The PMB 2341 is a monolithic, low power, high performance phase-locked-loop (PLL) frequency synthesizer. It is primarily designed to be used for very stable low noise LO signals in mobile communication systems such as GSM, PCN (GSM 1800), PCS and PDC. The wide range of divider ratios also allows application in modern analog systems.

Package



Features

- B6HFC BiCMOS technology
- 2.7 to 4.5 V operation
- Low operating power consumption
- Programmable power down modes
- High input sensitivity and high input frequencies up to 2.5 GHz
- Reference frequencies up to 100 MHz.
- Programmable dual modulus prescaler divide ratio (1:64/65 or 1:32/33).
- Dividing ratios: A, N, R counter: 0 to 63, 3 to 4095, 3 to 4095, respectively
- Fast phase detector with switchable polarity
- charge pump output with programmable current and without dead zone
- Fast serial 3-wire bus interface with low threshold voltage Schmitt-Trigger inputs
- One multi-functional port
- Very small Mini-TSSOP-10 Package

Ordering Information

Type	Ordering Code	Package
PMB 2341		Mini-TSSOP-10

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Product Description

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2.1 Overview

The PMB 2341 is a monolithic, low power, high performance phase-locked-loop (PLL) frequency synthesizer. It is primarily designed to be used for very stable low noise LO signals in mobile communication systems such as GSM, PCN (GSM 1800), PCS and PDC. The wide range of divider ratios also allows application in modern analog systems.

2.2 Features

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2.3 Package outline

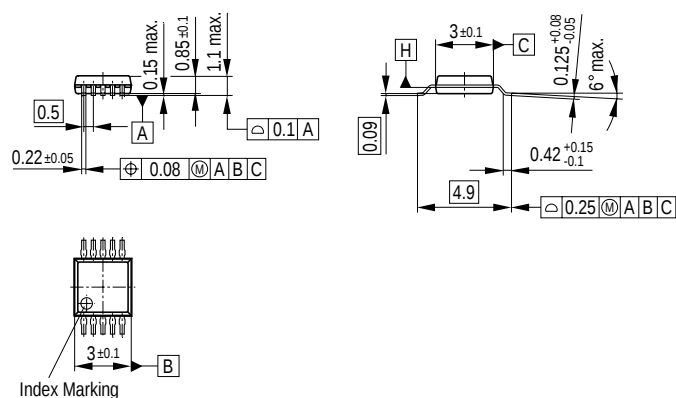


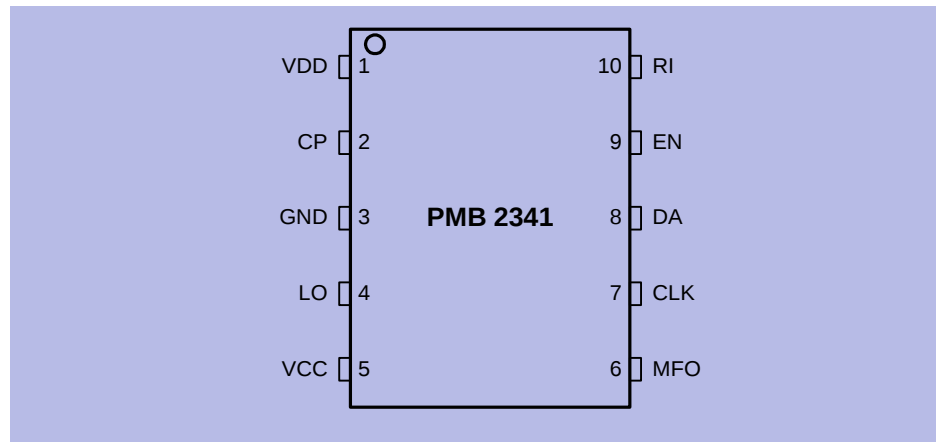
Figure 2-1 Mini-TSSOP-10

3 Functional Description

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3.1 Pin Configuration



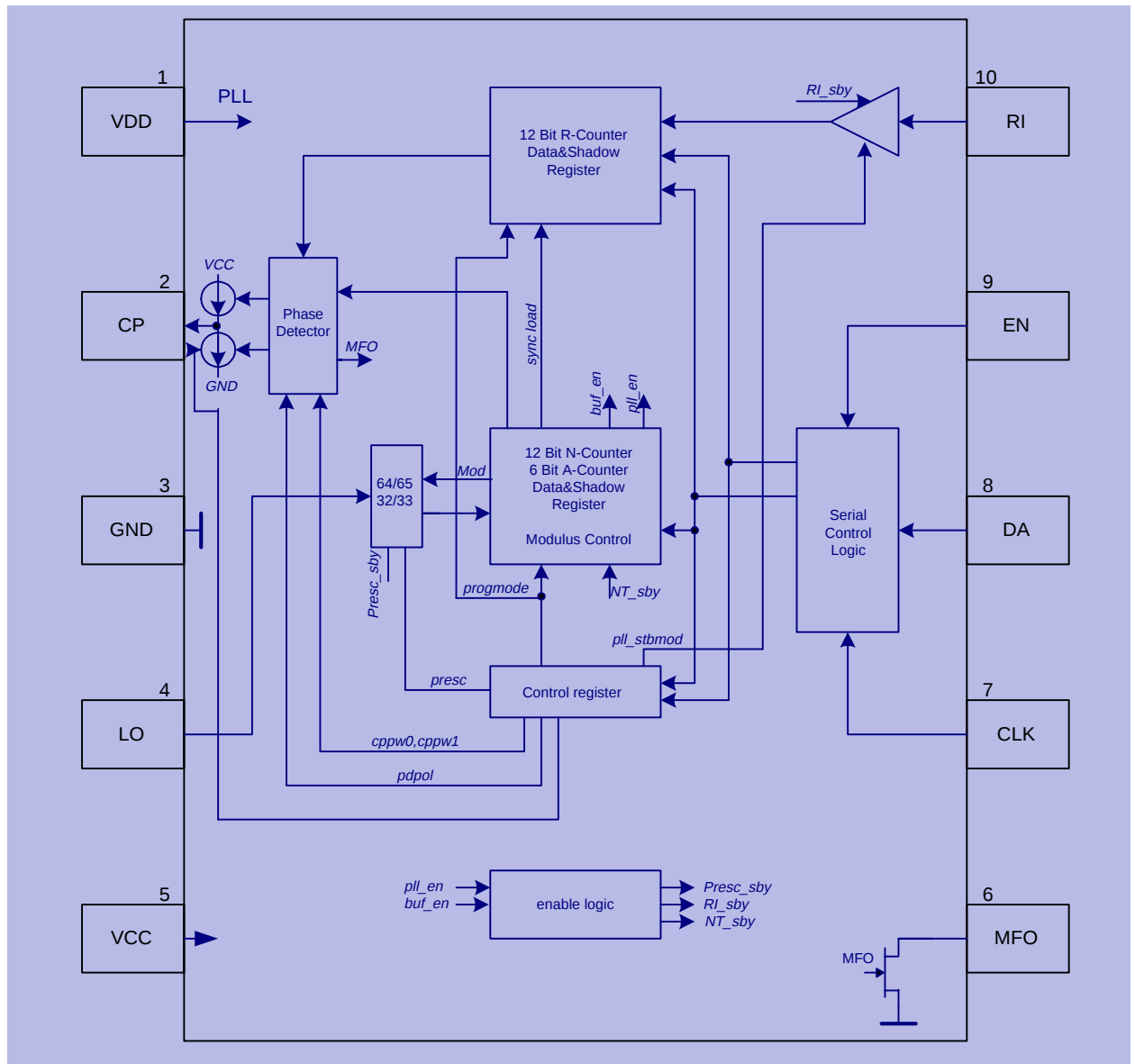
Pin_config.wmf

Figure 3-1 IC Pin Configuration

3.2 Pin Definition and Functions

Pin No.	Symbol	Function
1	VDD	Digital CMOS supply voltage. Note: VDD and VCC must be equal!
2	CP	PLL charge pump output
3	GND	Analog / bipolar ground, Charge pump ground and Digital CMOS ground (VSS) Used for bipolar prescaler, charge pump and Digital CMOS
4	LO	RF frequency input AC coupling is required.
5	VCC	Analog / bipolar supply and Charge pump supply Used for bipolar prescaler, input buffer and chargepump Note: VDD and VCC must be equal!
6	MFO	Multi-functional output (Open-drain)
7	CLK	3-Wire bus input: Clock Clock input of the serial control interface with CMOS Schmitt-Trigger input stage
8	DA	3-Wire bus input: Data Data input of the serial control interface with CMOS Schmitt-Trigger input stage. The serial data are read into the addressed internal shift register with the positive edge of CLK
9	EN	3-Wire bus input: Enable Enable input of serial control interface with CMOS Schmitt-Trigger input stage. When EN=H the input signals CLK and DA are disabled. When EN=L the serial control interface is enabled. The received data bits are transmitted into the addressed registers with the positive edge of EN
10	RI	Reference frequency input Input with highly sensitive preamplifier. With small input signals AC coupling must be set up, whereas DC coupling can be used for large input signals

3.3 Block diagram



Block_diag.wmf

Figure 3-2 Main block diagram

3.4 Functional Blocks

3.4.1 General information

The PMB2341 consists of a dual band single PLL. The device is designed to work in mobile communication systems and can handle VCO input frequencies up to 2.5 GHz.

3.4.2 PLL

The PLL in the PMB 2341 consists of a high frequency bipolar configurable 32/33 or 64/65 dual modulus prescaler, an A- and a N-counter with dual modulus control logic, a reference- (R-) counter, and a phase detector with charge pump output with programmable output current drive capability. The counter and mode settings of the synthesizer are programmed via a serial 3-wire interface.

The reference frequency is applied at the RI-input and divided by the PLL's R-counter. Its maximum value is specified to be 100 MHz. The VCO's RF input signal is divided by the bipolar prescaler with a programmable 32/33 or 64/65 divider ratio and the following programmable A/N-counters. For a wide range of divider ratios, both N and R counter can be programmed from 3 to 4095 .

The phase and frequency detectors with the charge pumps have a linear operating range without dead zone for very small phase deviations.

The operating modes allow the selection of 4 different charge pump output currents, polarity setting of the phase detector, 2 standby modes and the control of the multi-functional output port MFO.

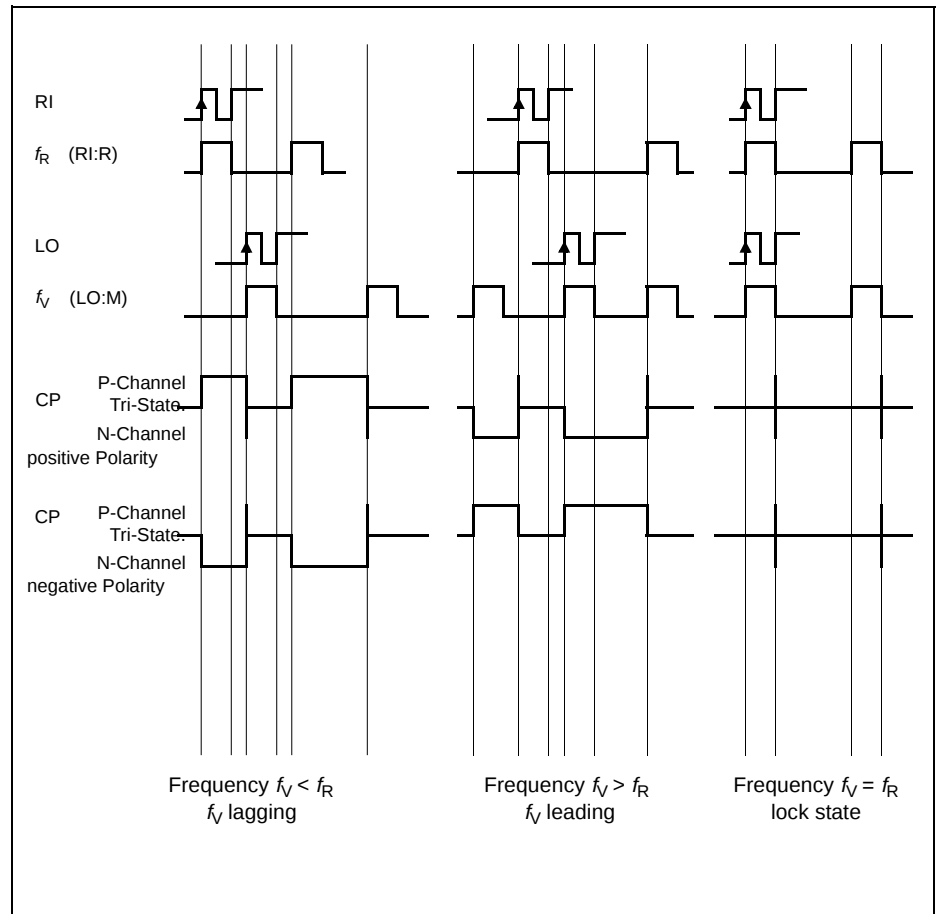


Figure 3-3 Frequency detector output waveforms

Frequency setting / divider ratio calculation:

The frequency of an external VCO controlled by the PMB 2341 is given below:

$$f_{VCO} = [(P \cdot N) + A] \cdot \frac{f_{RI}}{R} = \frac{M}{R} \cdot f_{RI}$$

with .

f_{VCO} : frequency of the external VCO

f_{RI} : reference frequency

N: divide ratio of the N-counter

A: divide ratio of the A-swallow counter

P: divide ratio of the prescaler (33 in case of 23/33 prescaler selected)

R: divide ratio of the R-counter

$M=P \cdot N + A$: total divide ratio

Note: for continuous frequency steps following condition is necessary

$$[P \cdot N + A] \geq P \cdot (P - 1)$$

Further restrictions have to be fulfilled:

$$A < P$$

$$A \leq N$$

3.4.3 Stand-by / power down conditions

The PMB 2341 device has 2 different stand-by modes to reduce the power consumption. The standby modes allow separate power up and down modes for the PLL itself and for the RI input amplifier circuitry. The selection of a desired power-down mode is done by setting two bits 'standby1' and 'standby2' located in the A/N-counter control word (see table 4-1: A/N counter data format).

This enables a fast wake-up of the device and programming of a VCO-frequency with only one bus cycle!

The encoding of the defined modes can be obtained from table 4-5: standby mode selection bits.

4 Applications

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4.1 Programming

General information:

Programming of the IC is done via the 3 wire serial data interface consisting of a clock line, data line and an enable line. Data are shifted into the device with every rising CLK edge and are overtaken into internal registers with the rising edge of EN according to the schematic timing diagram shown in Figure 4-1.

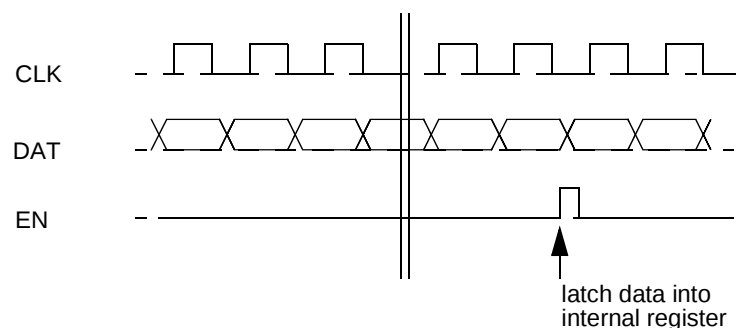


Figure 4-1 Schematic bus signal timing

Depending on the desired functional units to be programmed, several serial data formats exist. A common fact is that all multibit values are ordered in little endian notation in the bitstream meaning their MSB is sent first.

Every bus cycle starts with the dedicated data bits followed by at least 1 register address bit and is terminated with two device address bits. In chapter 4.2 Register, Data format the available data formats are explained.

The short control data format allows a fast PD-current change.

The long control data format allows the programming of 4 different PD-output current modes for the PLL, polarity setting of the PD-output signals, 2 standby modes, test mode select and the prescaler divide ratio.

The A/N-counter data format contains the A/N-counter values, the multifunctional output bit and standby mode switch bits.

The R-counter data format contains the R-counter values and PLL programming mode switch bit.

The PLL is programmed in an asynchronous mode: The serial data is written directly to the data registers of the addressed counter with the enable pulse. As each counter is loading the new starting value after it is decremented to „zero“, the counters changes therefore their counter values asynchronously to the others.

4.2 Register, Data format



Note

MSB of all serial data is shifted first!

Table 4-1 A/N counter data format

PLL			
Bit-Nr		Bit	Function
LSB 0	0	caddr0	chip address
1	1	caddr1	
2	1	raddr0	A/N register address
3		n0	N-counter
4		n1	
5		n2	
6		n3	
7		n4	
8		n5	
9		n6	
10		n7	
11		n8	
12		n9	
13		n10	
14		n11	
15		standby1	PLL on/off
16		standby2	Ri input amp on/off
17		a0	A-counter
18		a1	
19		a2	
20		a3	
21		a4	
22		a5	
23 MSB		MFO	multifunc. output port 2 (MFO)

Table 4-2 R counter data format

PLL			
Bit-Nr		Bit	Function
LSB 0	0	caddr0	chip address
1	1	caddr1	
2	0	raddr0	R register address
3	1	raddr1	
4		r0	R-counter
5		r1	
6		r2	
7		r3	
8		r4	
9		r5	
10		r6	
11		r7	
12		r8	
13		r9	
14		r10	
15 MSB		r11	

Table 4-3 Control data formats

Long control data format PLL				Short control data format PLL		
Bit-Nr	Value	Bit	Function	Value	Bit	Function
LSB 0	0	caddr0	chip address	0	caddr0	chip address
1	1	caddr1		1	caddr1	
2	0	raddr0	long control word address	0	raddr0	short control word address
3	0	raddr1		0	raddr1	
4	1	raddr2		0	raddr2	
5		cpcurr2	charge pump current setting		cpcurr2	charge pump current setting
6		cpcurr1			cpcurr1	
7		cpcurrst	charge pump current test mode		cpcurrst	charge pump current test mode
8		presc	prescaler division ratio			
9	0	n.a.	required for correct operation			
10		pdpol	phase detector polarity			
11	0	n.a.	required for correct operation			
12	1	n.a.				
13		mode2	test mode selection			
14		mode1				
15		not used				
16		not used				
17		not used				
18		not used				
19		not used				

Table 4-4 Chip address bit

Bits		Description
caddr1	caddr0	
1	0	This chip address has to be sent to access the PMB2341

Table 4-5 Standby mode selection bits

Bits		Description	Remarks
standby 1	standby 2		
1	1	ALLRUN: PLL is powered on.	Enabling or disabling of certain bipolar modules is done by turning on or off its bias currents.
1	0	not used: identical to ALLrun.	
0	1	AMPRUN: PLL is powered off, only RI input preamplifier is powered on.	
0	0	ALLOPP: Both PLL and RI input preamplifier are powered off.	

Table 4-6 Port switching bits

Bit	VALUE	Description
MFO	0	Multifunctional output MFO is driven to ground (VSS)
	1	Multifunctional output MFO is driven to VDD

Table 4-7 Charge pump current programming bits

Bits		CP Current [mA]	Remark
cpcurr 1	cpcurr 2		
0	0	1.2 mA	
1	0	2.0 mA	
0	1	2.8 mA	
1	1	4.0 mA	
0	0	1.2 mA pump 1	
1	0	1.2 mA pump 2	
0	1	0.8 mA pump 1	
1	1	0.8 mA pump 2	

Table 4-8 Prescaler mode select bit

Bit	Value	Description
presc	0	32/33
	1	64/65

Table 4-9 Phase detector polarity select bit

Bit	Value	Description
pdpol	0	negative polarity
	1	positive polarity

Table 4-10 Test mode installation bits

Control Bits		Mode
mode 1	mode 2	
1	1	OPERATE: Normal operation of PLL and RI Buffer in installed mode. MFO pin has programmed level.
0	1	not used: identical to OPERATE
1	0	Testmode RCNTOUT: Charge pump is turned off. R-counter output at multifunctional MFO pin.
0	0	Testmode NCNTOUT: Charge pump is turned off. N-counter output at multifunctional MFOMFO pin.

4.3 Special programming sequences

Fast wake-up programming:

When the circuit is connected to the supply voltage all registers are undefined. Due to the fact that each counter is loading its new start value after it is decremented to „zero“, the start-up time of the counters with the programmed values is too long for some applications. If the device has previously been set to ALLOFF- or AMPRUN-mode (see Table 5) afterwards is turned to operating mode ALLRUN, the counters are starting immediatly with the preprogrammed start values. Therefore for fast startup after standby the following data transfer sequence is recommended:

Table 4-11 Fast Wake Up Data Transfer Sequence

Step	Serial Data Transfer Sequence
1	Long Control Word: 'OPERATE'
2	Set A-/N-Counter: AMPRUN mode
3	Set R-Counter
4	Set A-/N-Counter, AMPRUN mode
5	Set A-/N-Counter, ALLRUN mode

5 Reference

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5.1 Absolute Maximum Range

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, due to permanent damage to the device.

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Units	Remarks
		min	max		
CMOS Supply Voltage	V_{DD_lim}	-0.3	5	V	with respect to related ground.
Bipolar Supply Voltage	V_{CC_lim}	-0.3	5	V	
Difference between V_{CC} and V_{DD} levels			0.2	V	V_{CC} and V_{DD} are intended to have the same level
Applied voltage at pins CLK, DA, EN, RI, CP	V_{InCMOS_lim}	-0.3	$V_{DD} + 0.3$	V	
Input voltage (LO)	$V_{I_Bip_lim}$	-0.3	$V_{cc} - 0.8V$	V	
Output current open-drain-stage (MFO)	I_{O_OD}		1	mA	
Total power dissipation	P_{tot_lim}		t.b.d.	mW	
Ambient temperature	T_A	-40	85	°C	
Storage temperature	T_{stg}	-50	125	°C	
ESD integrity	V_{ESD}	t.b.d.	t.b.d.	V	

5.2 Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC characteristic limits are not guaranteed.

Table 5-2 Operating Ratings

Parameter	Symbol	Limit Values		Units	L	Remarks
		min	max			
CMOS Supply Voltage	V_{DD}	2.7	4.5	V		V_{CC} and V_{DD} are intended to have the same level
Bipolar Supply Voltage	V_{CC}	2.7	4.5	V		
Input VCO frequency at LO	f_{LO}		2500 (t.b.d.)	MHz		Prescaler set to 32/33-mode
Input VCO frequency at LO	f_{LO}		2500	MHz		Prescaler set to 64/65-mode
Input frequency at RI	f_{RI}		100 (t.b.d.)	MHz		

Output current open-drain-stage (MFO)	$ I_{O_PP} $	0.2	mA	
CP-output current of PLL	$ I_{O_CP} $	4	mA	
CP-output voltages	V_{O_CP}	0.5	$V_{CC} - 0.5$	V
Ambient temperature	T_A	-40	85	°C

5.3 Typical Power-On Time

Time required to turn PLL and/or LO-buffer-chain from installed standby-mode to mode ALLRUN. Time is measured from time point when the ENable-signal is sent on 3-wire bus after programming the appropriate data bits.

Table 5-3

Previously installed standby mode (see Table 5)	Turn-ON-time	Units	Remarks
AMPRUN	t.b.d	μs	see Note 1)
ALLOFF	1	μs	

NOTE 1: Only the turn-on time from PLL is measured, not the required lock-in time, which strongly depends on the loopfilter, etc.

5.4 Typical Supply current

Table 5-4

Standby mode (see Table 5)	CMOS-Supply I_{DD}	Bipolar Supply I_{CC}	Units	Test item	Test condition
ALLRUN	t.b.d	7.5	mA	1.1	see Note 1)
AMPRUN	t.b.d.	0	mA	1.3	
ALLOFF	0	0	mA	1.4	

Note 1) : Room temperature, All supplies set to 3.6V, $T_A = 27^\circ\text{C}$, $f_{RI} = 13\text{MHz}$, $f_{LO} = 1.2\text{GHz}$, internal fref = 200KHz, PLL locked in mode ALLRUN, charge pump output current set to 4mA. No bus programming activities. Values may vary within 10%

5.5 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production. Supply voltage V_{CC} , V_{DD} , V_{CP} = 2.7V...4.5V, Ambient temperature T_{amb} = -40°C to 85°C except especially mentioned other values

Table 5-5 AC/DC Characteristics

	Symbol	Limit Values			Units	Test Item	Test Conditions
		min	typ	max			
Input Signals (Schmitt-Trigger) DA, CLK, EN when configured as input							
H-input voltage	$V_{L_ST_H}$	1.5V		V_{DD}	V	2.1	$V_{DD} \leq 3.5V$
H-input voltage	$V_{L_ST_H}$	0.5 V_{DD}		V_{DD}	V	2.1	$V_{DD} \geq 3.5V$
L-input voltage	$V_{L_ST_L}$			0.5V	V	2.2	$V_{DD} \geq 2.7V$
Input capacity	C_{L_ST}			5	pF	2.3	
DC High-input current	I_{ST_H}		0	t.b.d.	μA	2.4	
DC Low-input current	I_{ST_L}		0	t.b.d.	μA	2.5	
Output Signals MFO (open drain)							
L-output voltage	$V_{O_OD_L}$			0.1V	V	3.2	$I_{O_OD_L} \leq 25\mu A$
H-output current	$I_{O_OD_H}$			0.2	mA	3.3	
Charge Pump Output Current I_{O_CP}							
"1.2 mA"	$ I_{O_CP} $	-20%	1.2	+20%	mA	5.1	$V_{CP} = 3.6V$, $V_{O_CP} = V_{CP}/2$
"2 mA"	$ I_{O_CP} $	-20%	2.0	+20%	mA	5.2	
"2.8 mA"	$ I_{O_CP} $	-20%	2.8	+20%	mA	5.3	
"4 mA"	$ I_{O_CP} $	-20%	4.0	+20%	mA	5.4	
"Leakage Current"	$ I_{O_CP} $		0.1	1*)	nA	5.5	*) guaranteed by design
Output Tolerance I_{O_CP} with varying voltage at pin CP							
$\Delta I_{O_CP} / I_{O_CP}$				t.b.d		6.1	$V_{CP} = 3.6V$, $V_{O_CP} = V_{CP}/2$
$\Delta I_{O_CP} / I_{O_CP}$				t.b.d		6.2	$V_{O_CP} = 0.5...3.1V$
Crystal Oscillator Input Signal RI							
Input voltage	V_{L_RI}	100			mV rms	7.1	Note 1)
Input at LO; VCC=3.6 V							
DC voltage at LO	V_{LODC}		2		V	8.1	

Note 1: f_{RI} =4..30 MHz, V_{DD} =3.6 V measured with PLL in mode RCNTOUT (see Table 4-10) at pin MFO.

5.6 Serial Control Data Format Timing

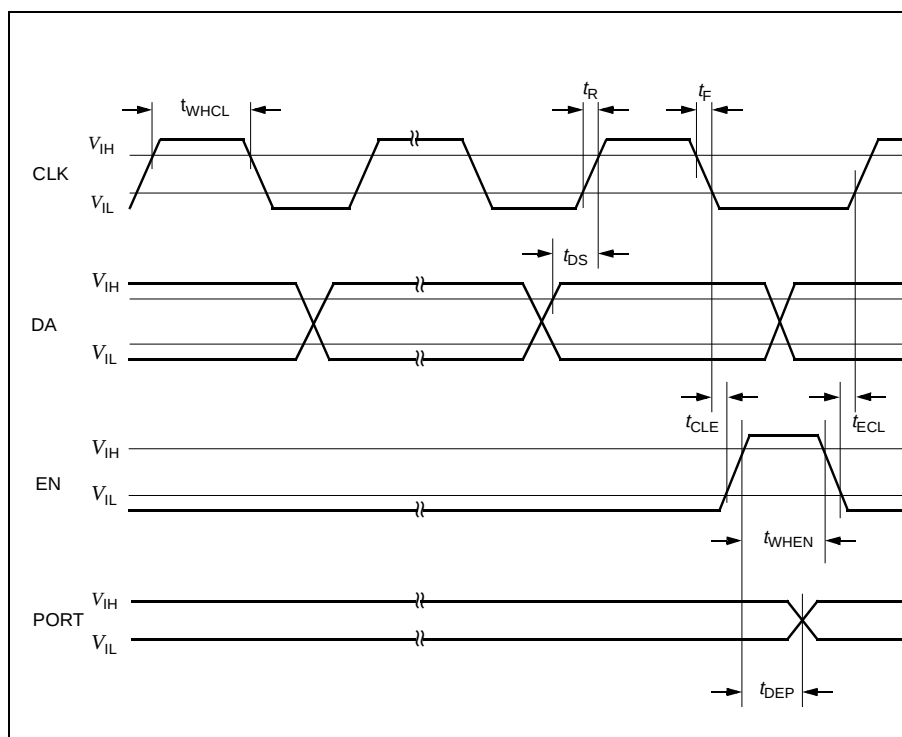


Figure 5-1 Serial Control Data Format Timing

Table 5-6

Parameter	Symbol	Limit Values		Units
		min	max	
Clock frequency	f_{CLK}		15	MHz
H-pulsewidth (CLK)	t_{WHCL}	30		ns
Data setup	t_{DS}	20		ns
Setup time Clock-Enable	t_{CLE}	20		ns
Setup time Enable-Clock	t_{ECL}	20		ns
H-pulsewidth (Enable)	t_{WHEN}	60		ns
Rise, fall time	t_R, t_F		10	μ s
Propagation delay time EN-PORT	t_{DEP}		1	μ s

5.7 RF Input Sensitivity

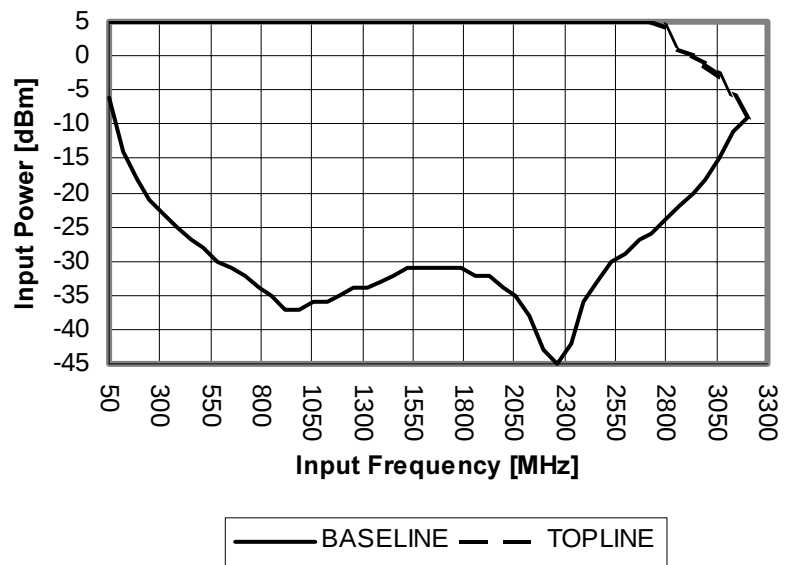


Figure 5-2 RF Input Sensitivity

Measured Prescler RF Sensitivity ($V_{cc}=2.7V$, 64/65 divider)