SIEMENS

ICs for Communications

LNA/MIXER

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Ausgabe 06.96

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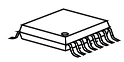
SIEMENS

LNA/MIXER **PMB 2332**

Version 1.2 **Bipolar IC**

1 Overview

1.1 Functional Description, Benefits



P-TSSOP-16

- New B6HF bipolar technology, 25GHz ft
- Frequency range up to 1.1 GHz
- Small outline P-TSSOP 16 package
- 2.7-4.5V supply voltage
- -40°C to +85°C operational temperature range
- 7.7 mA total current consumption, adjustable
- Standby function
- Reduced external components
- High isolation between mixer ports
- Good crosstalk performance

LNA:

- 17 dB gain, 1.3dB noise figure at 0.9GHz
- Gain adjustable over 20 db range
- 5.5mA current consumption

MIXER:

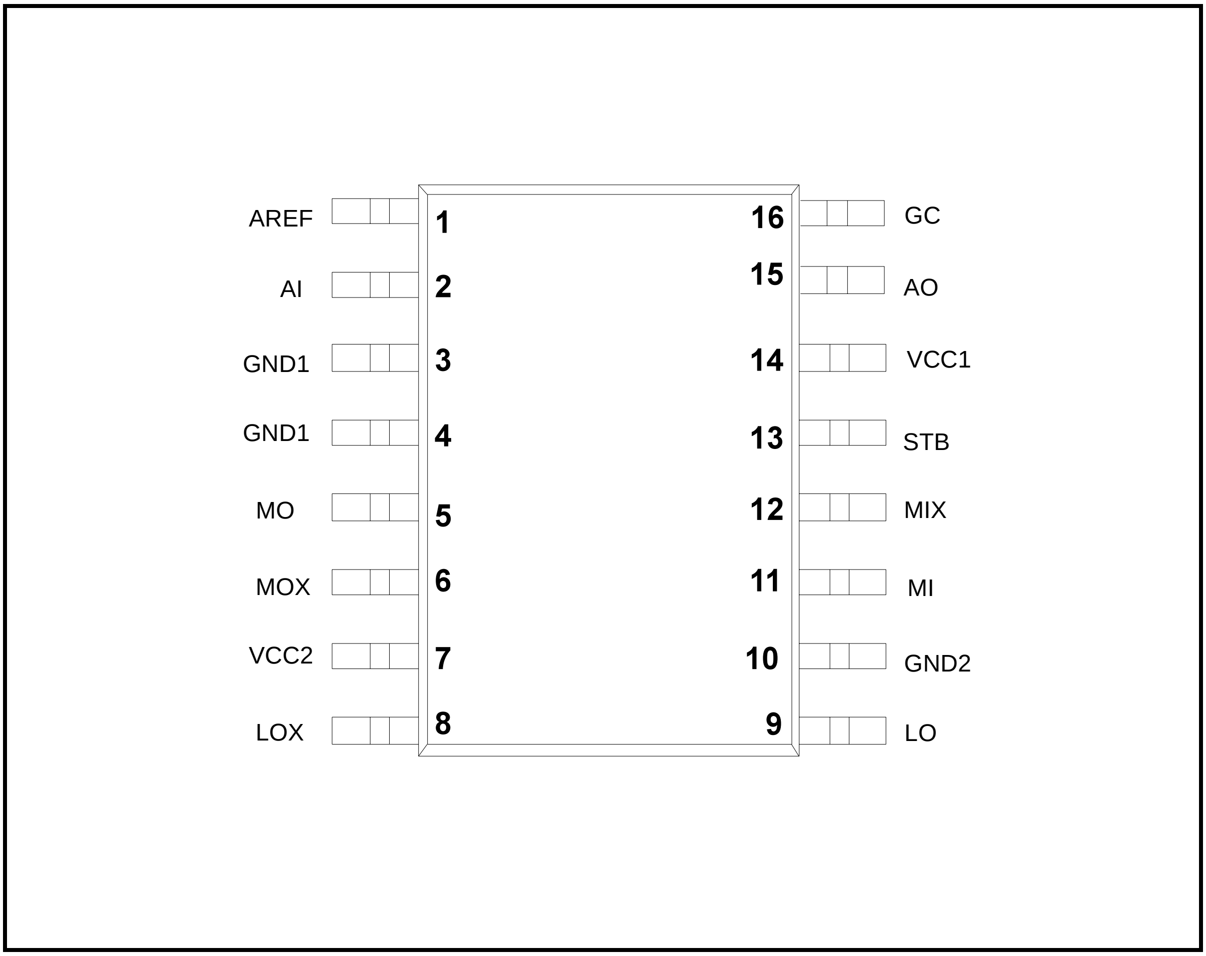
- Universal Gilbert cell mixer with adjustable mixer current
- 15dB gain, 9dB ssb noise figure for 0.9GHz at 45MHz IF
- IF up to 3GHz

1.2 Applications:

- All wireless systems up to 1.1GHz

Type	Ordering Code	Package
PMB 2332		P-TSSOP-16

1.3 Pin Configuration
(top view)

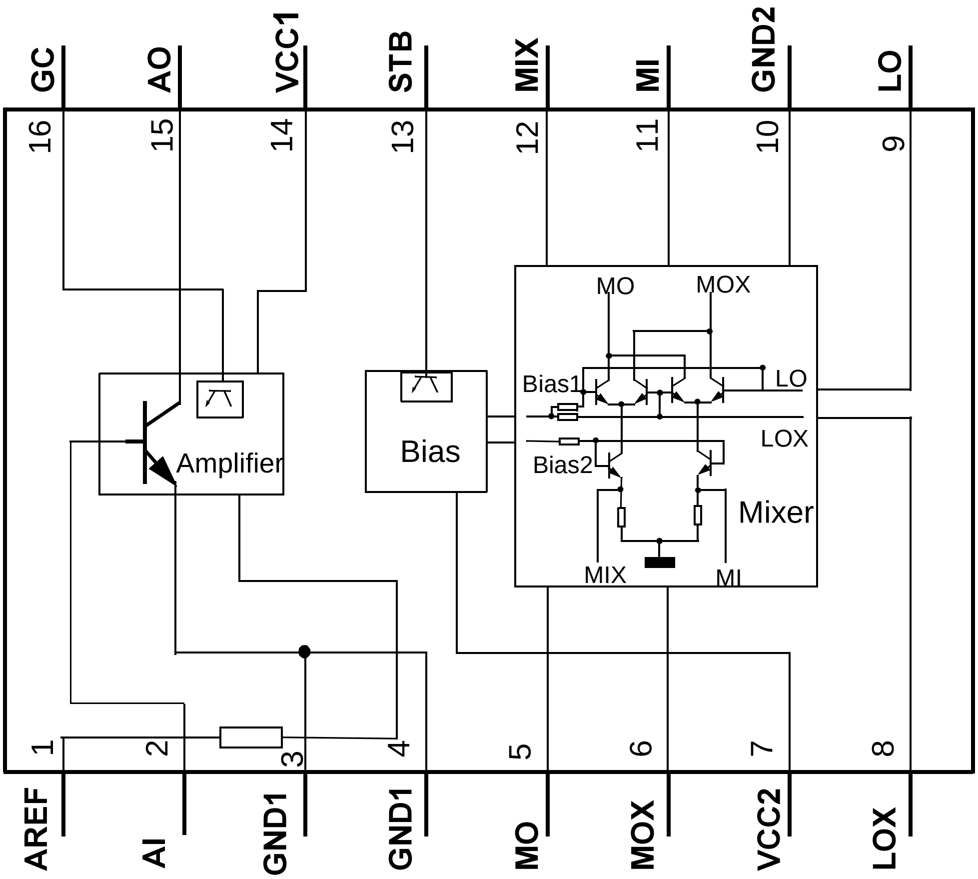


P-TSSOP-16

1.4 Pin Definitions and Functions

Pin No.	Symbol	Function
1	AREF	LNA bias supply for AI input
2	AI	LNA signal, base input
3	GND1	LNA ground
4	GND1	LNA ground
5	MO	Mixer signal open collector output, not inverted
6	MOX	Mixer signal open collector output, inverted,
7	VCC2	Mixer voltage supply
8	LOX	Mixer local oscillator signal base input, inverted
9	LO	Mixer local oscillator signal base input, not inverted
10	GND2	Mixer ground
11	MI	Mixer signal emitter input, not inverted
12	MIX	Mixer signal emitter input, inverted
13	STB	Standby total circuit
14	VCC1	LNA voltage supply
15	AO	LNA signal output, open collector
16	GC	LNA gain control input

1.5 Functional Block Diagram



1.6 Circuit Description

General Description

LNA

After entering the IC at pin AI the RF input signal is amplified in the lna stage. The gain of this lna is controlled with the dc level at pin GC and can be adjusted over a range of 20 db. The output pin AO makes the amplified signal externally available for further use. Matching networks at in-/ and output can be used to improve the gain and noise performance. For reducing the series feedback of the emitter line the lna is connected to GND with the two GND1 pins. At AREF the internal supplied reference voltage has to be blocked for improving the noise performance and needs to be connected to AI for biasing the lna transistor stages. VCC1 is the voltage supply for the lna.

MIXER

The mixer used in this design is a symmetric gilbert cell mixer. The amplified and filtered RF signal reenters the IC via a transformer at the pins MI/MIX, a base grounded balanced input configuration. With an external supplied local oscillator at LO/LOX a up/ down converted output signal is created at the open collector pins MO/MOX. For biasing the open collector pins need to be connected to an external voltage supply. The input pins MI/MIX and LO/LOX can be used in a balanced or unbalanced configuration. Via the pins VCC2 and GND2 the mixer voltage supply has to be connected to the IC.

COMMON

Differential signals and symmetrical circuits are used throughout the mixer part of the IC. An internal bias driver generates supply voltage and temperature compensated reference voltages. The STB pin allows the circuit to be switched in a low power consuming mode. All pins with the exception of AI,AO and GND1,2 are ESD protected.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Ambient temperature T_{amb} = -40°C...+85°C

#	Parameter	Symbol	Limit Values		Units	Remarks
			Min	Max		
1	Supply Voltage	V_S	-0.3	5.5	V	V_S=V_{CC1} =V_{CC2}
2a	Input Voltage	$V_{MI/MIX}$	-0.3	1.9	V	V_S = 0V
2b	Input Voltage	$V_{LO/LOX}$	0.6	V_S+0.3	V	
2c	Input Current	I_{AI}		0.16	mA	
2d	Input Voltage	V_{GC}	-0.3	V_{CC1}+0.3	V	
2e	Input Voltage	V_{STB}	-0.3	V_S+0.3	V	
2f	Output current	I_{AO}		8	mA	
3a	Output Voltage	V_{AREF}	no external Voltage			to be connected to AI
3b	Open Collector Output Voltage	$V_{MO/MOX}$	1.3	V_S+0.3	V	
3c	Open Collector Output Voltage	V_{AO}, V_{CC1}	1.0	V_S+0.3	V	
4	Differential Input Voltage	VI_{DIFF}		2.0	V_{PP}	
5	Junction Temperature	T_j		125	°C	
6	Storage Temperature	T_S	-40	125	°C	
7	Thermal Resistance	R_{thJA}		184	K/W	

2.2 Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC characteristic limits are not guaranteed.

Supply voltage V_{VCC} = 2.7V...4.5V, Ambient temperature T_{amb} = -40°C...85°C

#	Parameter	Symbol	Limit Values		Units	Remarks
			Min	Max		
1	AI Input Frequency	f_{AI}		1100	MHz	
2	MI/X Input Frequency	f_{MI}		3000	MHz	
3	LO/X Input Frequency	f_{LO}		3000	MHz	
4	IF Intermediate Frequency	f_{IF}		3000	MHz	
5	Standby Voltage On	STB_{ON}	2.0	V_S	V	
6	Standby Voltage Off	STB_{OFF}	0	0.5	V	
7	Gain Control On	GC_{ON}	0	1.2	V	Diagram4
8	Gain Control Off	GC_{OFF}	2.3	V_S	V	Diagram4

Note: Power levels refer to 50 Ohms impedance

2.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Supply voltage V_{VCC} = 2.7V...4.5V, Ambient temperature T_{amb} = +25°C

#	Parameter	Symbol	Limit Values			Units	Test Conditions	Test Circuit
			Min	Typ	Max			
Supply Current								
1	Supply current, total IC	$I_{5,6,7,14,15}$		7.7		mA	STB ON, no external resistors R1,2	1a,b
2	Supply current, total IC	$I_{5,6,7,14,15}$		10.7		mA	STB ON, with ext. resistors R1,2=180Ω*	1a,b
3	Supply current, total IC	$I_{5,6,7,14,15}$		<20		µA	STB OFF	1a,b
Gain Control								
	Adjustable gain range	ΔG		20		dB	Diagram 4	1a,b
LNA, Signal Input AI, max. gain adjusted								
5	Input impedance vs. freq.	S_{11}					Diagram 2a	1a,b
6	Max. input level, 1db comp.	P_{AI}		-18.0		dBm	f=0.9GHz	1a
7	Input intercept, third order	$IICP_{AI}$		0		dBm	f=0.9GHz	1a
8	Noise figure	F_{AI}		1.3		dB	f=0.9GHz	1a**
LNA, Signal Input AI , min. gain adjusted								
9	Input impedance vs. freq.	S_{11}					Diagram 2b	1a,b
10	Max. input level, 1db comp.	P_{AI}		-18.0		dBm	f=0.9GHz	1a
11	Input intercept, third order	$IICP_{AI}$		0		dBm	f=0.9GHz	1a
12	Noise figure	F_{AI}		8.0		dB	f=0.9GHz	1a**

All LNA mesasurements have been done with Siemens RT5880 Duroid (Teflon) Boards

* Minimum Values for external resistors at MI/MIX R1=R2=180Ω
** matching network used

AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Supply voltage V_{VCC} = 2.7V to 4.5V, Ambient temperature T_{amb} = +25°

#	Parameter	Symbol	Limit Values			Unit	Test Conditions	Test Circuit
			Min	Typ	Max			
LNA, Signal Output AO, max. gain								
13	Output current	I_{AO}		5.0		mA		1a
14	Output impedance vs. freq.	S_{22}					Diagram 2a	1a
15	Power gain	S_{21LNA}		17		dB	f=0.9GHz	1a
LNA, Signal Output AO, min. gain								
16	Output current	I_{AO}		0.5		mA		1a
17	Output impedance vs. freq.	S_{22}					Diagram 2b	1a
18	Power gain	S_{21LNA}		-3		dB	f=0.9GHz	1a
MIXER, Signal Input MI/MIX, Downconversion, $R_{1/2}$=180Ohm								
19	Input impedance vs .freq.	Z_{MI}					Diagram 3a	1a,b
20	Max. input level, 1 db comp. at MO/MOX, IF=45MHz	P_{MI}		-15		dBm	f=0.9GHz	1a
21	Input intercept point, Δf=800kHz, IF= 45MHz	$IICP3_{MI}$		0		dBm	f=0.9GHz	1a
22	Blocking level, Δf=800kHz, IF=45MHz, P_{IN},unwanted= -20dB	P_{IN}, unwanted		-16		dBm	f=0.9GHz	1a
23	Noise figure, ssb ($NF_{SSB} \leq NF_{dsb}$+3dB), IF=45MHz	F_{MI}		9		dB	f=0.9GHz	1a*
MIXER, Local Oscillator Input LO/LOX, Downconversion, $R_{1/2}$=180Ohm								
24	Input impedance vs freq.	Z_{LO}					Diagram 3b	2a,b
25	Input level	P_{LO}		-3		dBm	f=0.9GHz	1a, **

*matching network used

** referenced for specified mixer performance

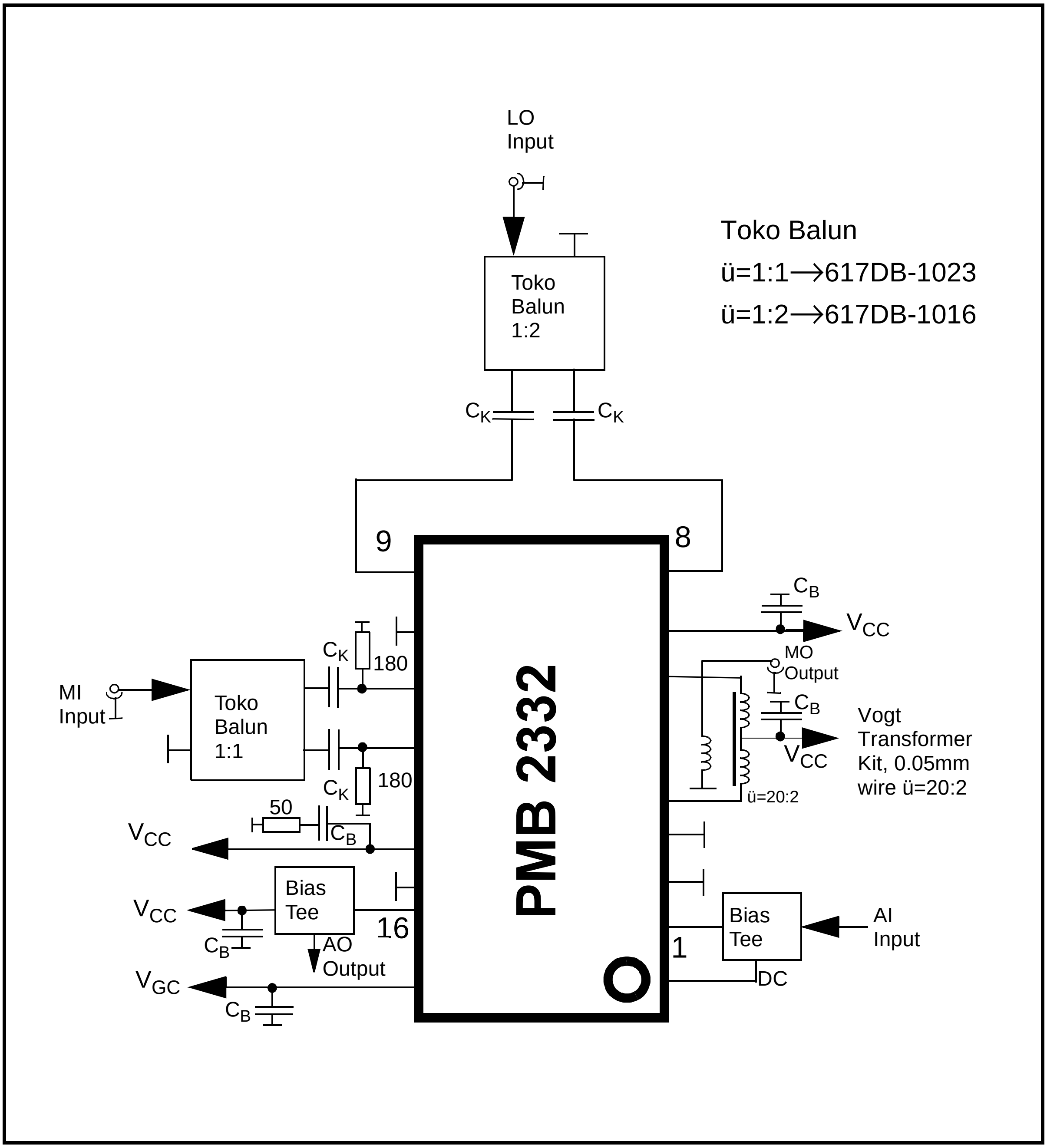
AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Supply voltage V_{VCC} = 2.7V...4.5V, Ambient temperature T_{amb} = +25°C

#	Parameter	Symbol	Limit Values			Units	Test Conditions	Test Circuit
			Min	Typ	Max			
MIXER, Signal Output MO/MOX, Downconversion, $R_{1/2}$=180Ohm								
26	Output current	I_{MO+MOX}		4.0		mA	incl. R1,R2	1a
27a	Output resistance	R_{MODiff}		32		kOhm	IF=45MHz	1a
27b		R_{MODiff}		25		kOhm	IF=300MHz	1b
28a	Output capacitance	C_{MODiff}		0.36		pF	IF=45MHz	1a
28b		C_{MODiff}		0.39		pF	IF=300MHz	1b
29	Power gain, IF=45MHz	P_{MI}		15		db	f=0.9GHz	1a
30	Power gain, IF=300MHz	P_{MI}		7		db	f=0.9GHz	1b
MIXER, Isolation Between In-/Output, 0.9GHz, Downconversion, $R_{1/2}$=180Ohm								
31	MI to MO	A_{MI-MO}		50		db	f_{MI}=945MHz, f_{LO}=900MHz	1a
32	LO to MO	A_{LO-MO}		40		db	"	1a
33	LO to MI	A_{LO-MI}		35		db	"	1a
34	MO to MI	A_{MO-MI}		60		db	"	1a
35	MO to LO	A_{MO-LO}		60		db	"	1a

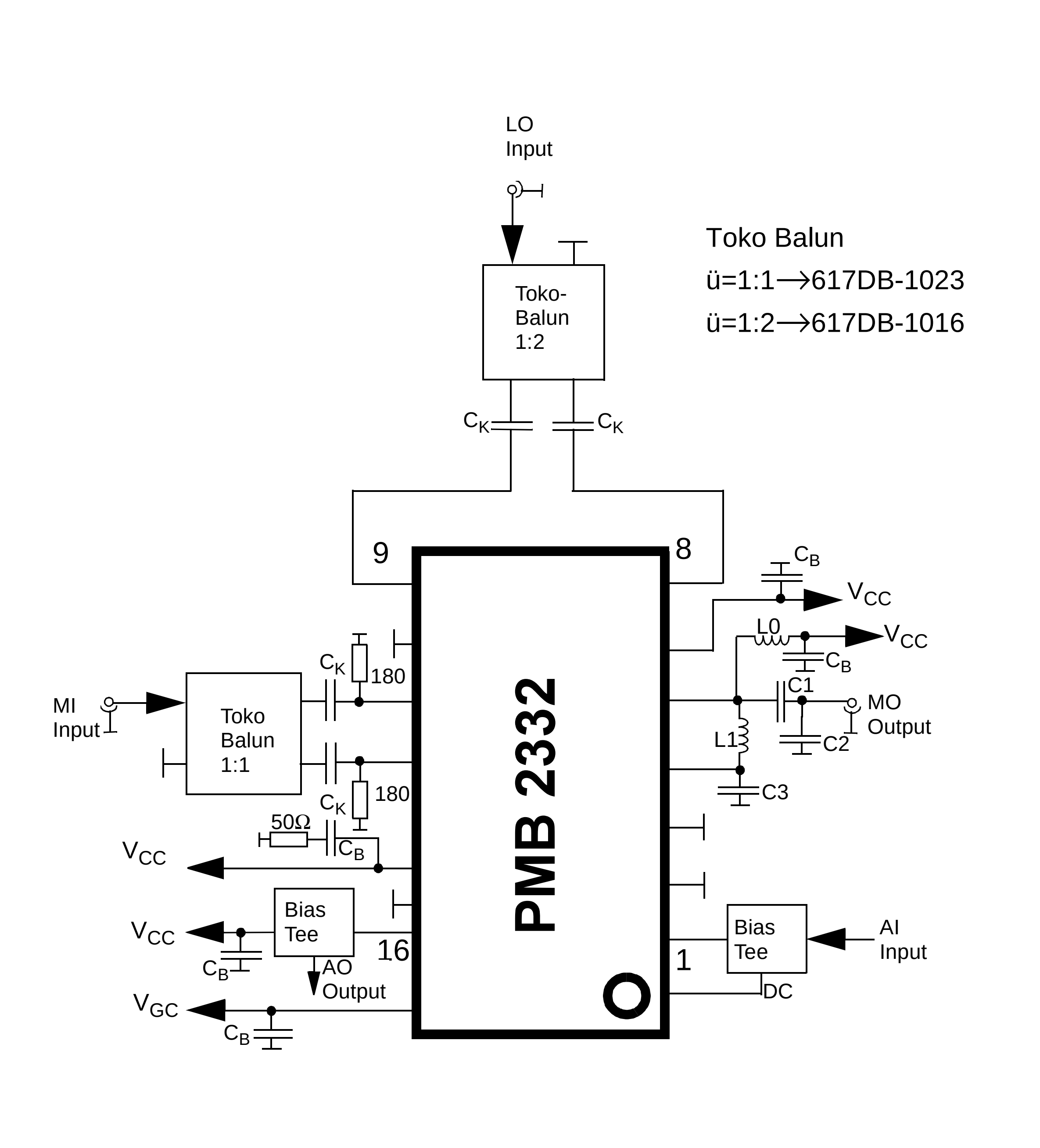
Test Circuit 1a



Test Circuit for 45 MHz Intermediate frequency

Test Circuit	f_{IF}[MHz]	C_B[pF]	C_K[pF]	X	X
1a	45	15/100	15	X	X

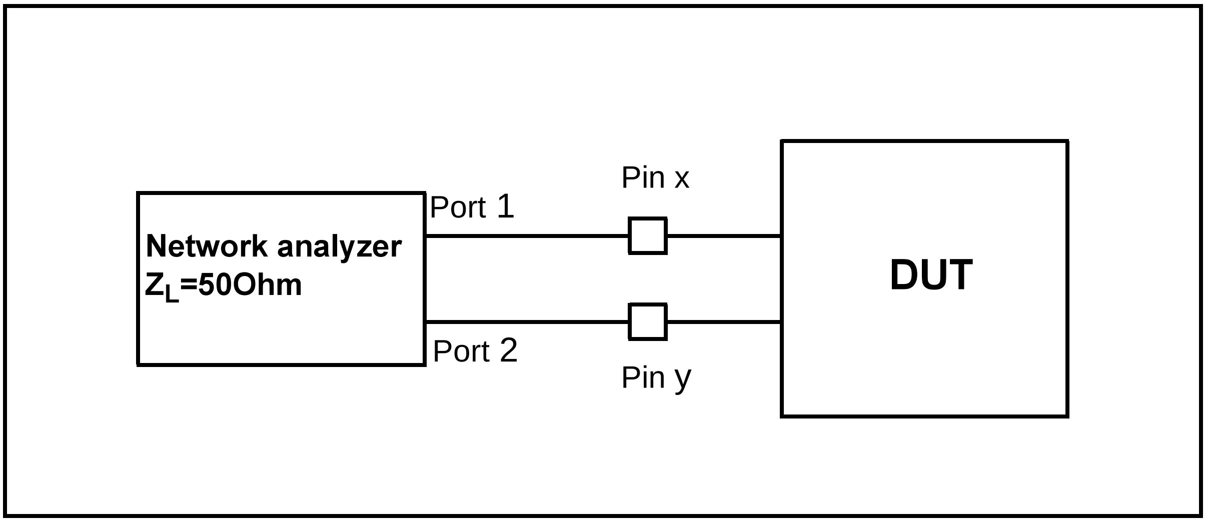
Test Circuit 1b



Test Circuit for 300 MHz intermediate frequency

Test Circuit	f_{IF}[MHz]	L0[nH]	L1[nH]	C1[pF]	C2[pF]	C3[pF]	C_K[pF]
1b	≈300	680	150	2.7	12	1.8	15

Test Circuit 2



S-Parameter Measurement of Amplifier
S11, S12, S21, S22

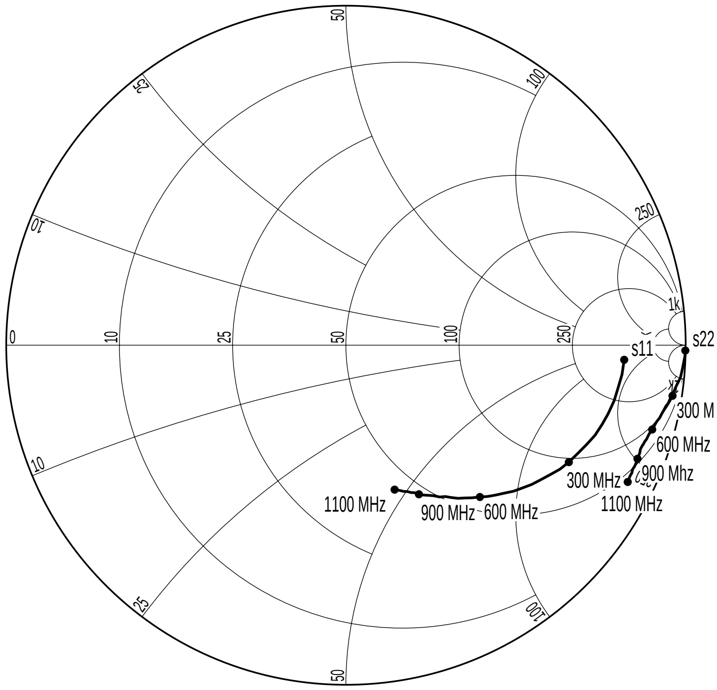
The S-Parameters are tested at the indicated frequency on Duroid 5880 Teflon Boards.

Via the NWA the capacitive coupling is done.
The output levels at port1 and 2 for pin x and y are -30dbm.

S11 and S22 have to be considered as design hints and are measured with SIEMENS testboards.

Test	Test frequency MHz	Pin X	Pin Y
Amp.S11, S12, S21, S22	30 - 1100	AI	AO

Diagram 2a
S-Parameter LNA I=5mA, V_{CC}=3.3V; f=30-1100MHz; High Gain



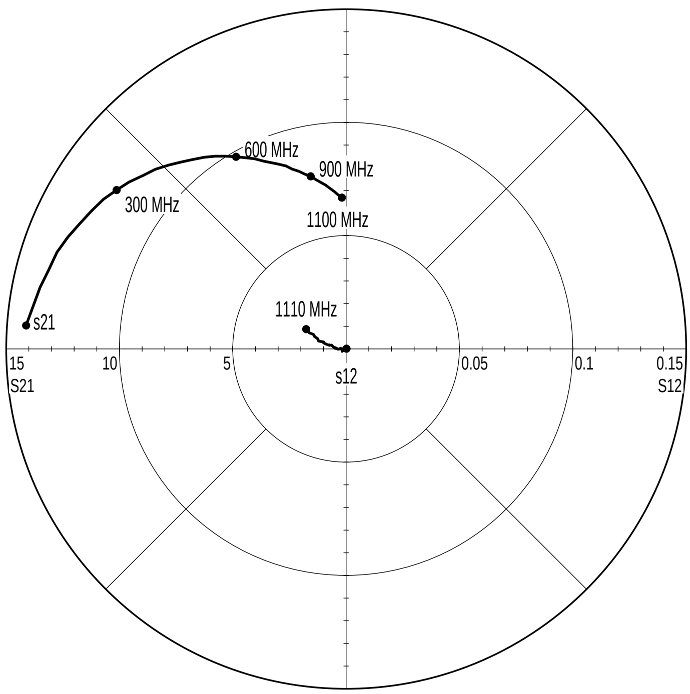
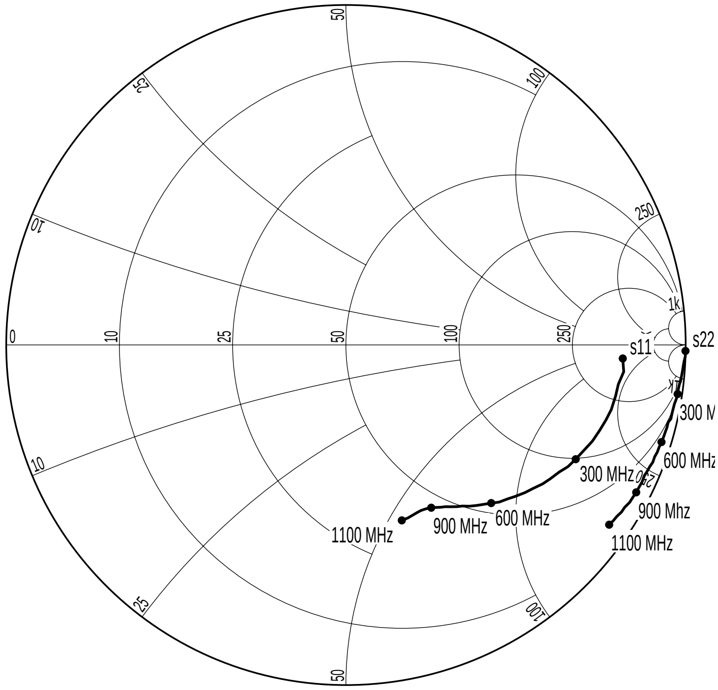
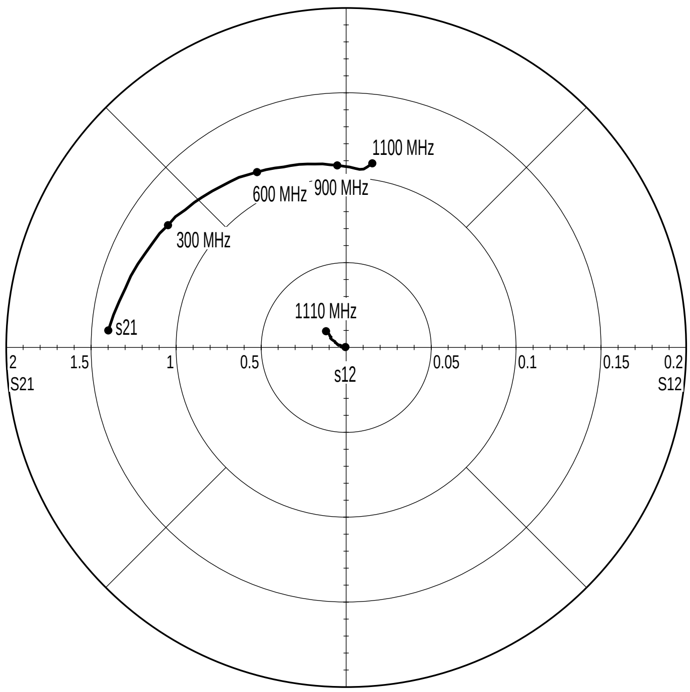
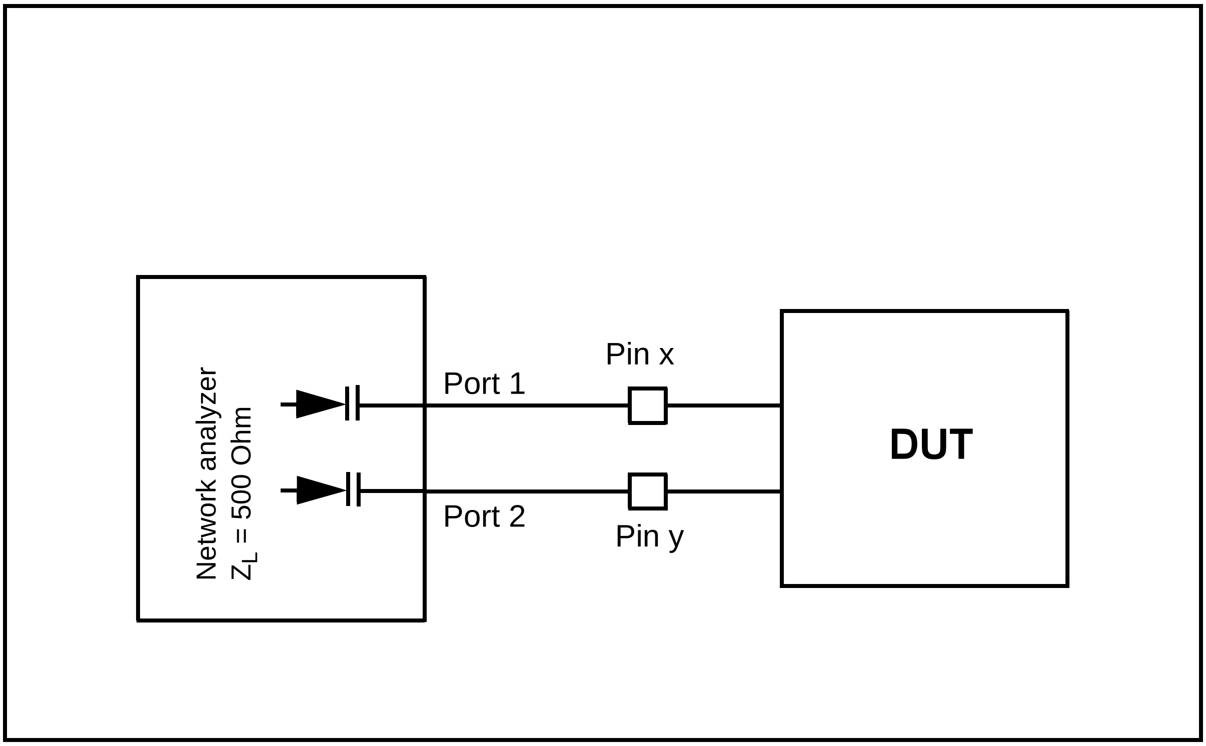


Diagram 2b
S-Parameter Amplifier I=0.5mA, V_{CC}=3.3V; f=30-1100MHz ; Low Gain





Test Circuit 3



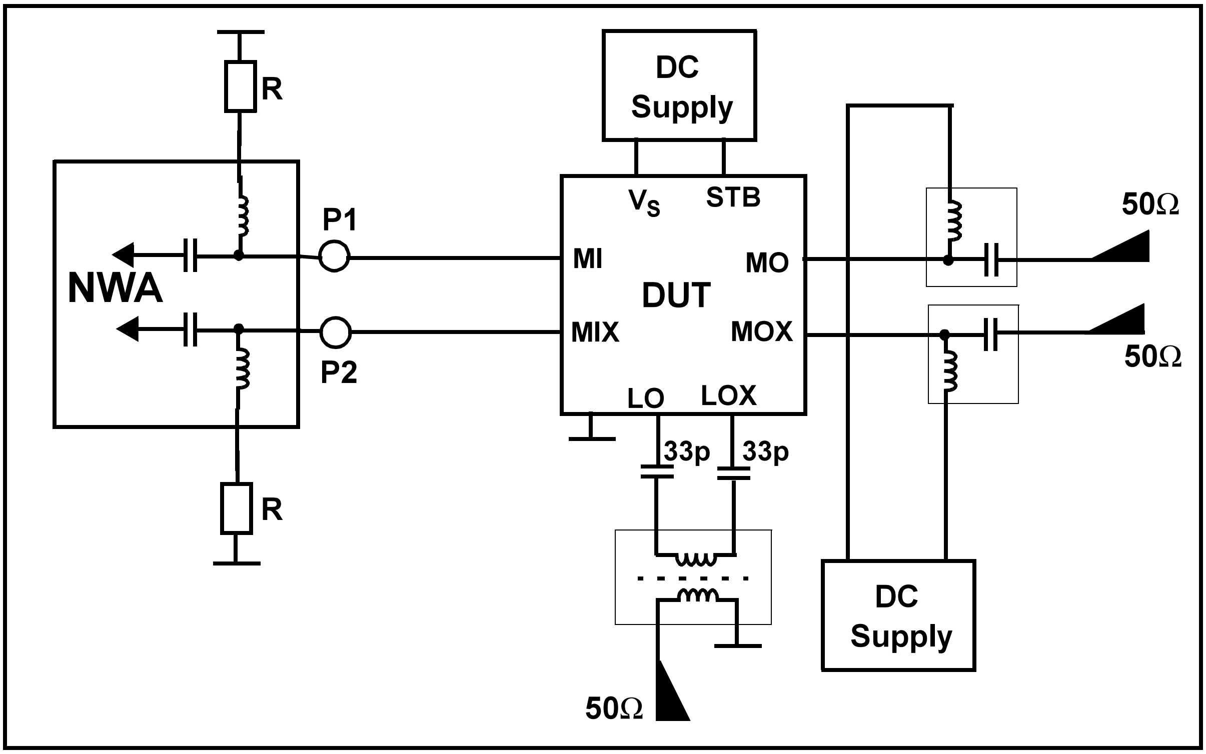
S-Parameter Measurement of Mixer
S11, S21, S12, S22

Test	Test Frequency [GHz]	Pin X	Pin Y
LO/X-Input impedance	30-3000	8	9
MI/X-Input impedance	30-3000	11	12
MO/X-Output impedance	30-3000	5	6

The S-Parameters are tested at the indicated frequency and the equivalent parallel or series circuit is calculated on this base.

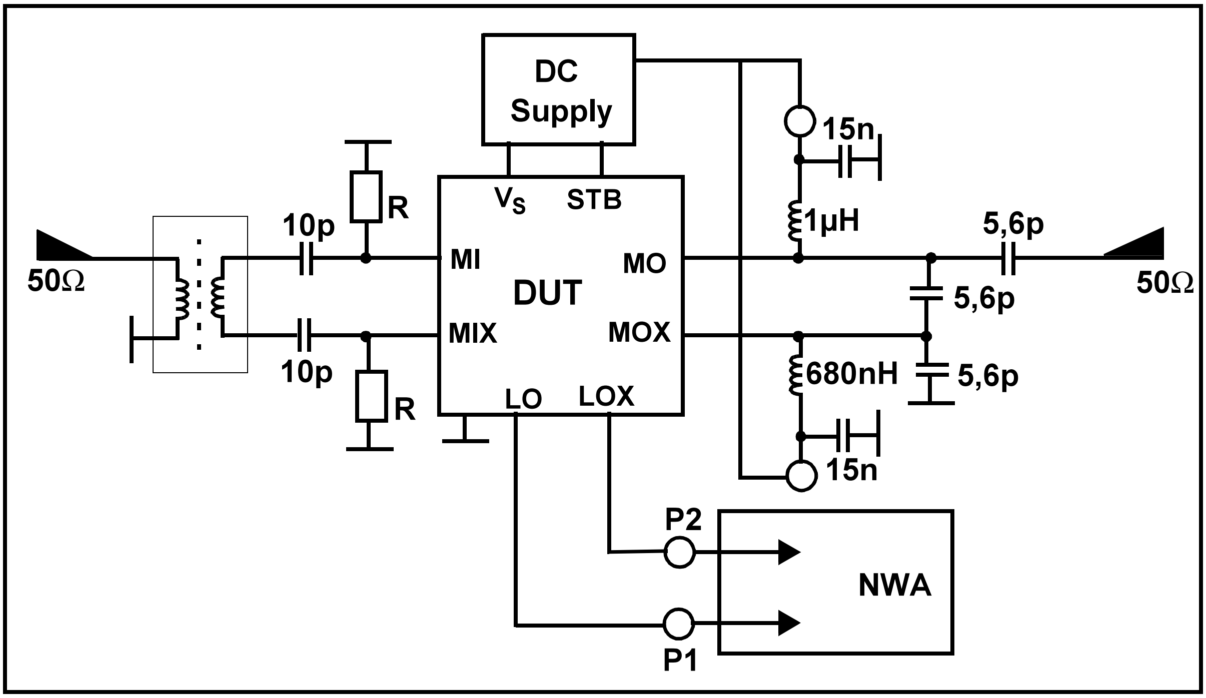
Via the NWA the capacitive coupling is done and the open collector pins are connected to VCC. The output levels at port1 and 2 for pin x and y are -30dbm for MI and MO impedances and -3dbm for the LO impedance. S-Parameters have to be considered as design hints and are measured with SIEMENS testboards. (Duroid 5880, Teflon Boards)

Test Circuit 3a



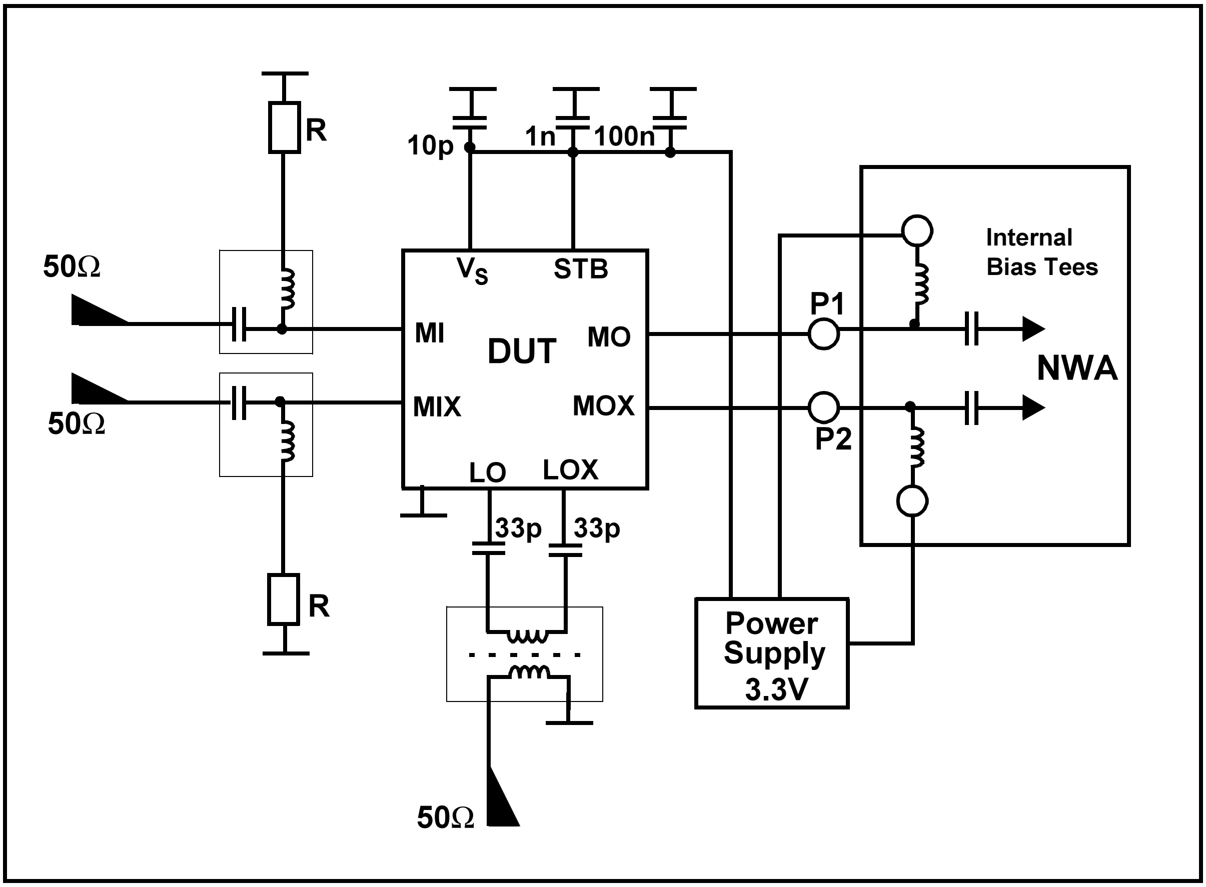
Mixer Input Impedance Measurement

Test Circuit 3b



Mixer Local Oscilllator Impedance Measurement

Test Circuit 3c



Mixer Output Impedance Measurement

Diagram 3a
Mixer MI Input Impedance Z_{MI}, $I_{MO/MOX}$ = 4mA; f=30-3000MHz

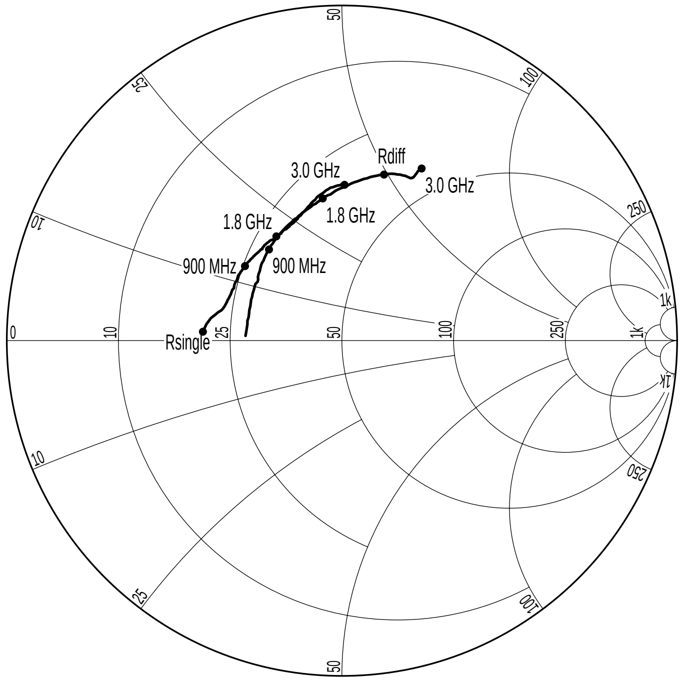
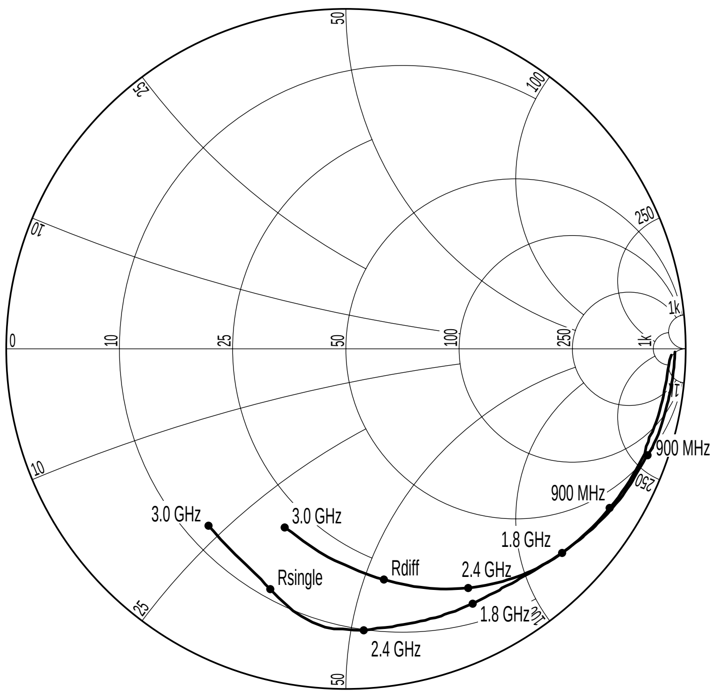


Diagram 3b
Mixer LO Input Impedance Z_{LO}, $I_{MO/MOX}$ = 4mA; f=30-3000MHz



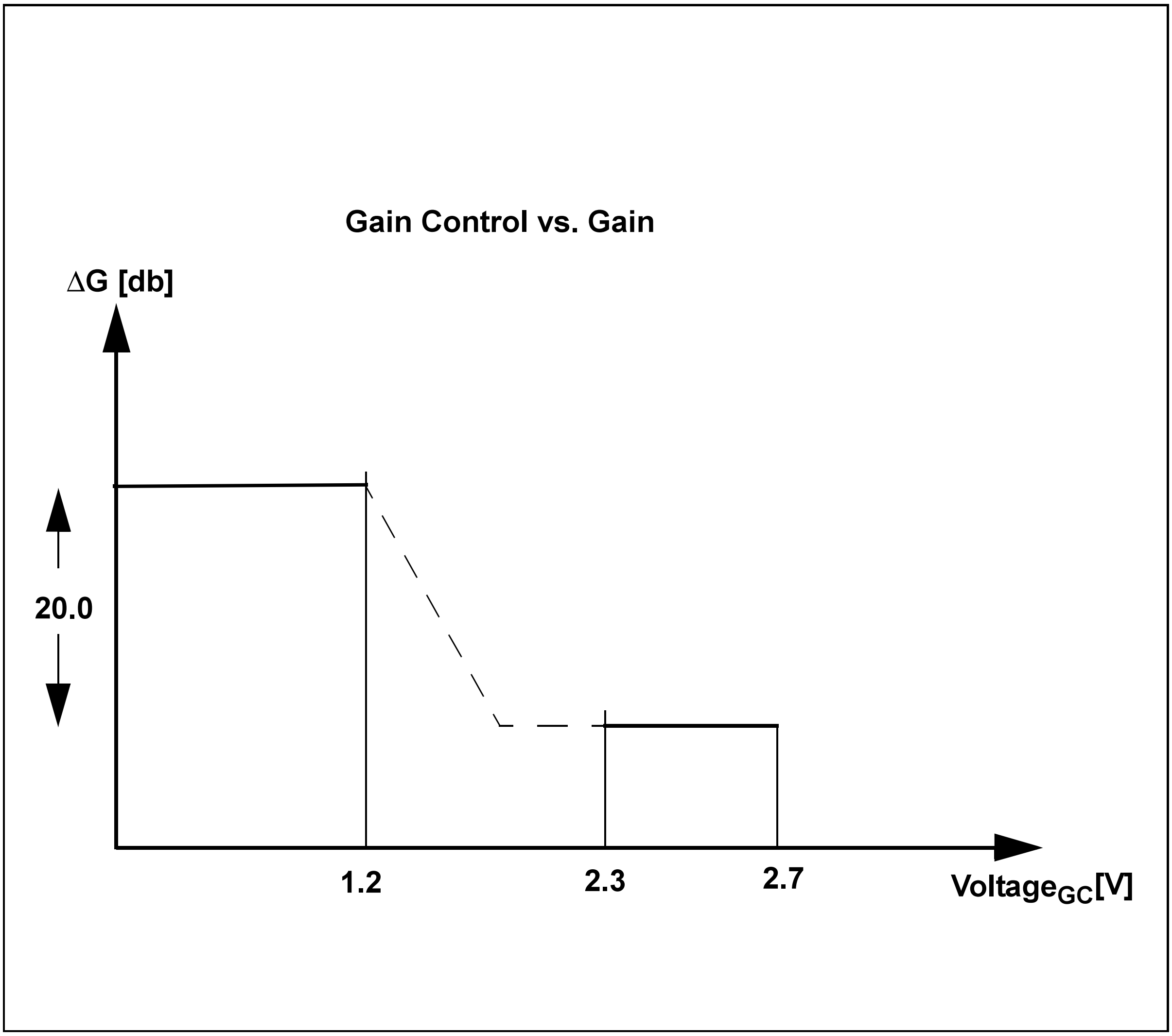
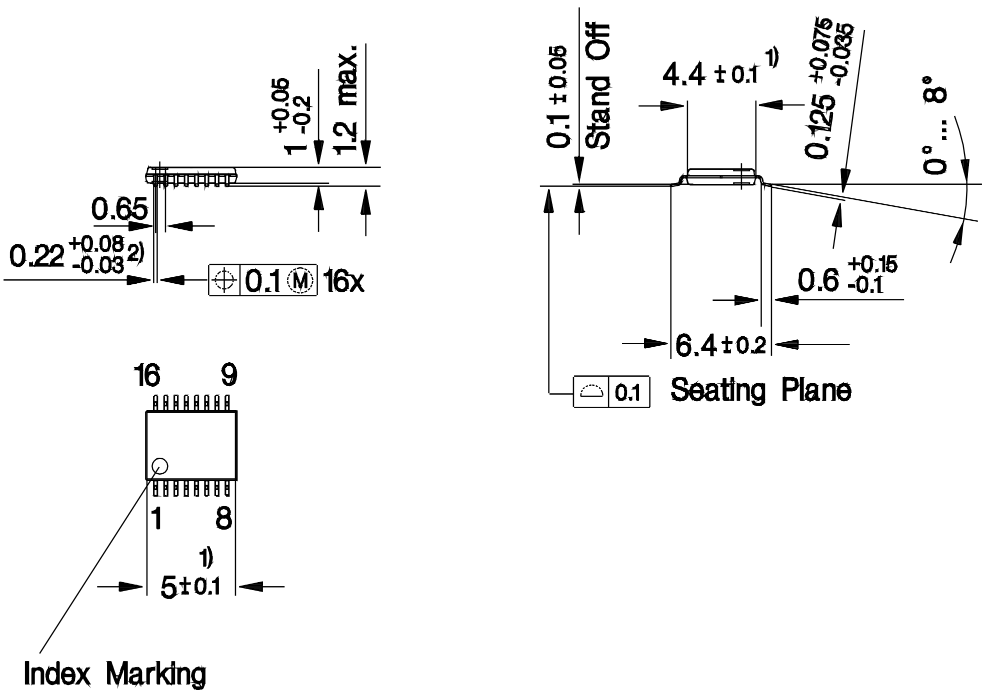


Diagram 4

3 Package Outlines

P-TSSOP-16
(Plastic Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm