Wireless Components

Transmitter PLL (Up-Conversion Loop Modulator)

PMB 2251 Version 1.3

Specification August 1999

preliminary

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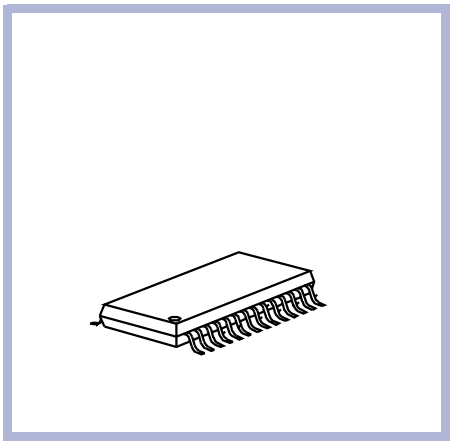
Product Info

General Description

The PMB 2251 is a transmitter PLL containing a modulator, a mixer, two programmable counters and a phase detector. The device is programmed via a three-wire bus.

Package



Features

- Vector modulator operating from 80 to 450MHz
  -Integrated generation of orthogonal carriers
  -Typ. 40dB carrier rejection, 40dB SSB rejection, 54dB IM3 supression
- Double balanced Gilbert cell mixer
  - single ended inputs and outputs
  - LO- and RF input frequency range: 800MHz to 2GHz
  - Output frequency range: DC to 450MHz
- Integrated modulation PLL
  -Input Counters programmable from 1 to 8
  -Charge pump with programmable current up to 4mA
  -Separate charge pump suppy voltage (2.7 to 5.5V)
  -Phase/Frequency-sensitive phase detector
  -Operation at up to 150MHz
  -Linear transfer characteristi (no dead zone)
- Serial data transfer via three-wire bus (Power-down modes programmable)
- Supply voltage 2.7 to 4.5V
- Temperature range -30° to 85°C

Application

- The PMB 2251 is intended for use in an up-conversion loop.
- The device has a wide frequency range and is suitable for mobile communication systems requiring a high modulation bandwidth and a low phase error.
- The device is part of the Infineon-chipset for single- and multiband mobile communication systems, such as GSM, PCN and PCS.

Ordering Information

Type	Ordering Code	Package
PMB 2251 V1.3		P-TSSOP-28

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2 Product Description

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2.1 General Description

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2.2 Application

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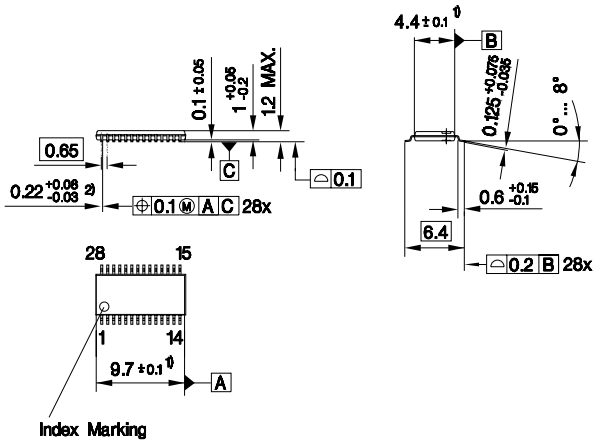
2.4 Package Outlines

P-TSSOP-28



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

3 Functional Description

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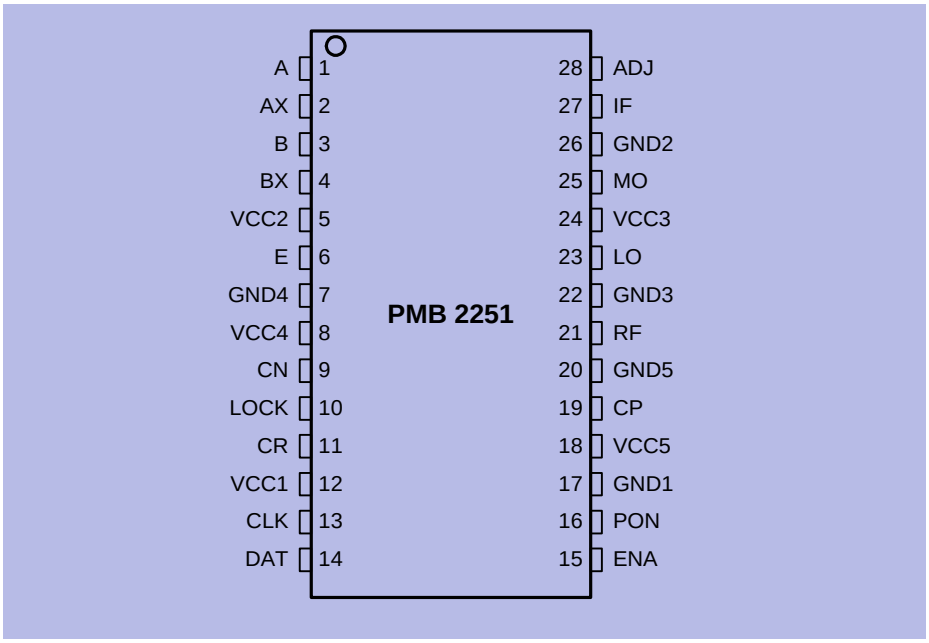
3.1 Pin Configuration

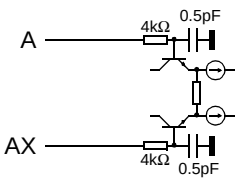


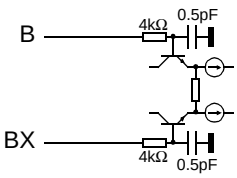
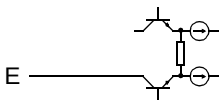
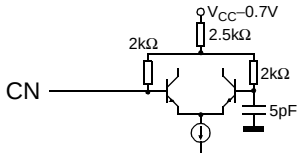
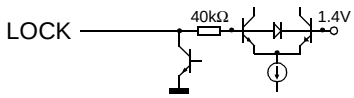
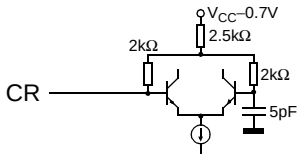
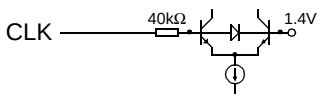
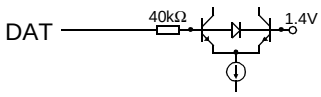
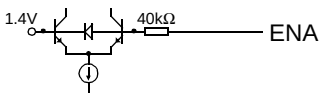
Pin_config.wmf

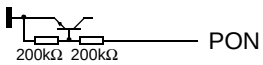
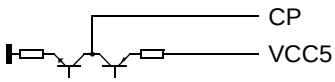
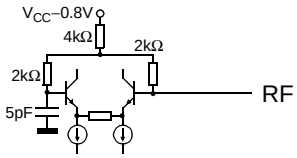
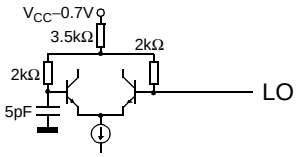
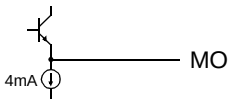
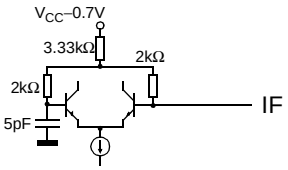
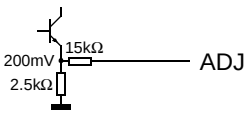
Figure 3-1 Pin Configuration

3.2 Pin Definition and Function

Table 3-1 Pin Definition and Function

Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	A		Modulation input (non-inverting)
2	AX		Modulation input (inverting)

3	B		Modulation input (non-inverting)
4	BX		Modulation input (inverting)
5	VCC2		Modulator supply voltage
6	E		Modulator output
7	GND4		Counter and phase detector ground
8	VCC4		Counter and phase detector supply voltage
9	CN		N-counter input
10	LOCK		Control input for charge pump current (also test output)
11	CR		R-counter input
12	VCC1		Bus supply voltage
13	CLK		Clock input
14	DAT		Data input
15	ENA		Enable input

16	PON		Power-on input
17	GND1		Bus ground
18	VCC5		Charge pump supply voltage
19	CP		Charge pump output
20	GND5		Charge pump ground
21	RF		Linear mixer input
22	GND3		Mixer ground
23	LO		Switching mixer input
24	VCC3		Mixer supply voltage
25	MO		Mixer output
26	GND2		Modulator ground
27	IF		Modulator carrier input
28	ADJ		Modulator phase adjust input

3.3 Block Diagram

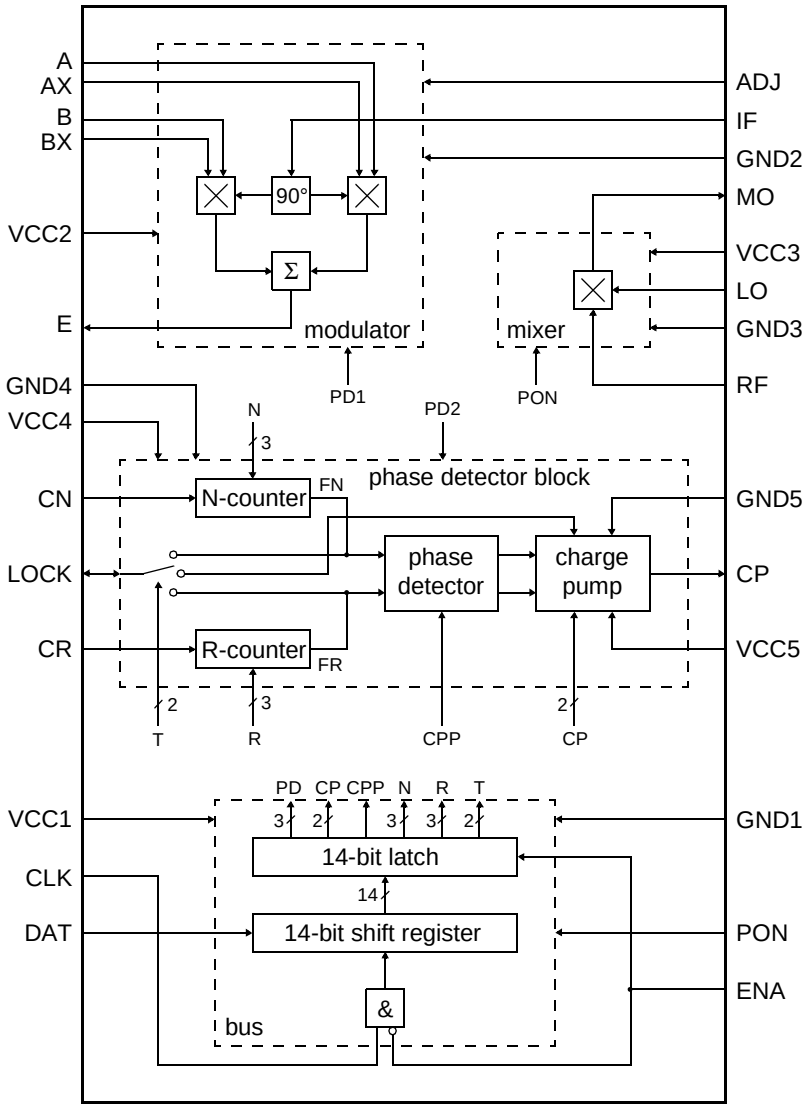


Figure 3-2 Block Diagram

3.4 Circuit Description

The modulator implements a single-sideband modulation. The signal at the IF input is split into two orthogonal carriers, which are multiplied by the signals at the modulation inputs A/AX and B/BX. The multiplication products are added and fed to the E output. The phase adjust input ADJ can optionally be used to maximise the single-sideband suppression of the modulator (see chapter 4).

The mixer multiplies the signals at the RF and LO inputs; the result appears at the MO output. The LO input is operated in switched mode, whereas the RF input is linear, which makes it suitable for a modulated signal.

The counters divide the frequency of the signals at the CN and CR inputs by the programmed factors N and R respectively, and feed the resulting signals FN and FR to the phase detector, which drives the charge pump. The counter outputs switch on the rising edge of the inputs. A test mode can be programmed in which either FN or FR is fed to the LOCK pin.

At the CP output, the charge pump generates current pulses of width equal to the time interval between the negative edges of FN and FR. The height and polarity of the pulses are programmable. In the intervals between pulses, the output is in a high-impedance state. The polarity of the pulses depends on which input has the higher frequency, or, if both inputs have the same frequency, which input leads. The charge pump can be operated at a higher supply voltage than the rest of the circuit, to allow a larger tuning voltage range. When a logic HIGH is applied to the LOCK input, the charge pump current has the value programmed via the bus. Applying a logic LOW at the LOCK input switches the charge pump current to its maximum value of 4mA.

The device is programmed by shifting in a 14-bit control word at the DAT input. Each bit is transferred on the rising edge of the CLK input, starting with the most significant bit. The control word becomes valid on the rising edge of the ENA input, when it is loaded into a latch. The programming allows the modulator, the mixer and the phase detector block (including counters and charge pump) to be powered down individually. In the programmable power-down modes, the bus is ready to receive new data, and the control word remains latched. In the hardware power-down mode, activated by a logic LOW at the PON input, the entire chip is powered down and the control word is lost. After a hardware power-on, the modulator and phase detector blocks are initially powered down, whereas the mixer is powered up with PON to prevent LO-VCO pulling.

4 Applications

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4.1 Circuit Principle

In the application circuit, the PMB 2251 is configured to form an up-conversion loop with external VCO and filters. In the feedback path of the loop, the mixer converts the transmit signal TX_OUT at the VCO output down to an intermediate frequency, where it is filtered and fed to the carrier input IF of the modulator. The modulator performs a single-sideband modulation of the baseband input signals at A_IN, AX_IN, B_IN, BX_IN on to the carrier. The modulator output at E is filtered and fed to the input CN of the N-counter. A constant reference frequency at CR_IN is applied to the R-counter. In the steady state of the loop, the VCO output is modulated so as to cancel the modulation in the modulator, so that the modulator output is a constant, unmodulated frequency.

The direct and indirect conversion methods require a highly selective bandpass filter to suppress the wideband noise of the modulator and mixer. In the up-conversion loop, the wideband noise is suppressed by the loop filter, which is a simple RC low-pass filter. Compared to other modulation methods, the up-conversion loop has the advantages of a better noise performance with lower filter costs and lower superimposed residual AM. As a result, the system can be operated with a higher efficiency in the power amplifier and a lower insertion loss in the antenna switch, both of which reduce the power consumption.

4.2 Intermediate Frequency

The mixer output MO, the carrier input IF and output E of the modulator and the N-counter input CN all operate at the intermediate frequency. In the Operational Range, the maximum intermediate frequency is specified at 400MHz, but the AC/DC characteristics are guaranteed only up to 350MHz. The functionality of mixer, modulator and N-counter in the range 300 to 400MHz is intended to allow the loop to lock for an initial VCO frequency deviation of up to 100MHz from its final value. In the locked state of the loop, the intermediate frequency may not exceed 300MHz. Note that the frequency sensitivity of the phase detector is guaranteed only up to 150MHz.

4.3 Supply and Ground Pins

On the circuit board, the ground pins GND1 to GND5 must all be connected by the shortest possible route to a common, low-impedance ground plane, and the supply pins VCC1 to VCC4 must all be connected to the same supply rail. It is permissible to connect VCC5 to a separate, higher supply voltage in order to increase the tuning voltage range. Each supply pin must be separately decoupled to the corresponding ground pin. The decoupling capacitor should be as close as possible to the pin and have its self-resonant frequency, and hence its minimum impedance, at the RF signal frequency in the block supplied by the pin.

4.4 Coupling Circuitry

The inputs CN, CR, RF, LO, IF are high-impedance inputs with internal resistors to a DC bias voltage (see Internal Input/Output Circuits). The signals at these inputs must be AC-coupled using an external capacitor. The optimum coupling is obtained when the self-resonant frequency of the capacitor is equal to the signal frequency. Note, however, that the power-up settling time depends on the time required to charge the coupling capacitors (see AC/DC Characteristics). There should be no external DC path to ground or supply at these pins, which means that any termination resistor must be placed on the other side of the coupling capacitor (e.g. R_3 and R_{10} in the application circuit).

The attenuation between TX_OUT and RF must be sufficient to ensure that the mixer is operated at least 3dB below its 1dB compression point. Because of the finite isolation of RF from LO (see AC/DC characteristics), the reverse attenuation must be sufficient to ensure that, in the signal spectrum at TX_OUT, the component at the LO frequency is within the system specification.

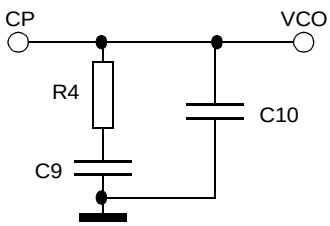
4.5 Loop Filter

In designing the loop filter, the same principles can be used as for a synthesizer PLL. The natural resonant frequency ω_n, the damping factor D and the phase margin ϕ_m are given by the following equations:

$$\omega_n = \sqrt{\frac{K_{VCO} I_{CP}}{N(C_9 + C_{10})}}$$

$$D = \frac{\omega_n R_4 C_9}{2}$$

$$\phi_m = \operatorname{atan}(4D^2) - \operatorname{atan}\left(\frac{4D^2}{1 + \frac{C_9}{C_{10}}}\right)$$



where K_{VCO} is the VCO gain in Hz V^{-1} (*not* rad s^{-1} V^{-1}), I_{CP} the programmed value of the charge pump current and N the division ratio of the N-counter. A phase margin of about 60° is recommended. The choice of values for ω_n and D involves a trade-off between phase accuracy and suppression of wideband noise. Provided the modulation frequency is less than $1/(2\pi R_4 C_9)$, the phase error depends only on ω_n and is a decreasing function of ω_n. The phase noise at a frequency offset much greater than ω_n is an increasing function of ω_n if D and ϕ_m are held constant, and a decreasing function of D (up to the point where the noise of R_4 begins to dominate) if ω_n and ϕ_m are held constant.

4.6 Other Filters

The low-pass filter between MO and IF suppresses the image frequency and any residual components at the RF and LO frequencies. To avoid excessive intermodulation, the current swing at the MO output should not exceed 2mA peak, which means a minimum load impedance of 50Ω for an output level of -10dBm.

E is a high-impedance, open-collector output, and requires a DC path to the supply voltage. The band-pass filter between E and CN suppresses the modulation product associated with the third harmonic of the carrier (see AC/DC Characteristics), which would cause in-band spurious in the VCO output spectrum due to intermodulation in the phase detector block. At the CN input, a suppression of at least 65dB relative to the wanted signal is recommended. Note that the third-harmonic suppression of the modulator improves with increasing frequency, therefore a high intermediate frequency is advisable. The voltage divider formed by R_1 and R_2 allows CN to be driven with a low impedance, which reduces cross-talk from E, without excessively damping the resonant circuit in the filter. The bandwidth of the filter must be wide enough to allow the loop to lock for maximum and minimum values of the initial VCO frequency.

4.7 Modulation Inputs

The modulator generates the upper sideband if A lags B by 90° and the lower sideband if A leads B by 90°. In the loop, the VCO is modulated so as to cancel the modulation in the modulator, so A should lead B if the upper sideband is required, and A should lag B if the lower sideband is required.

The allowed range of the DC level at the modulation inputs depends on the the voltage swing, the supply voltage and whether the drive is single-ended or balanced. The DC level and swing must be such that the instantaneous voltage at each input pin is at least 0.75V away from the ground and supply rails at all times (see Operational Range).

The single-sideband suppression of the modulator can be maximised by connecting a resistor to ground at the ADJ pin. The required value of the resistor depends on the IF frequency, and varies from R_{ADJ_80MHz} (t.b.d.) at 80MHz to R_{ADJ_350MHz} (t.b.d.) at 350MHz. If ADJ is not shorted to ground, a decoupling capacitor is recommended.

Offset voltages at the modulation inputs affect the carrier suppression. For an ideal modulator with external offsets V_{oa} and V_{ob} at the A and B inputs, the carrier suppression in dB is given by

$$a_c = 20 \log_{10}\left(\frac{V_m}{2\sqrt{V_{oa}^2 + V_{ob}^2}}\right)$$

where V_m is the peak-to-peak swing at the modulation inputs. The real modulator contains internal offsets, which are added to the external offsets. To obtain the best possible carrier suppression, it is advisable to use the maximum input swing of $1V_{pp}$ (see Operational Range), which means $500mV_{pp}$ at each pin for balanced operation.

Amplitude and phase errors in the modulation input signals affect the single-sideband suppression. For an ideal modulator with external amplitude error α (amplitude ratio – 1) and phase error ϕ (phase difference – 90°), the single-sideband suppression in dB is

$$a_{SSB} = 20 \log_{10} \sqrt{\frac{1 + \left(\frac{\alpha}{\alpha + 2}\right)^2 \tan^2\left(\frac{\phi}{2}\right)}{\left(\frac{\alpha}{\alpha + 2}\right)^2 + \tan^2\left(\frac{\phi}{2}\right)}}$$

The real modulator has an internal amplitude mismatch and phase error, which are added to the external ones.

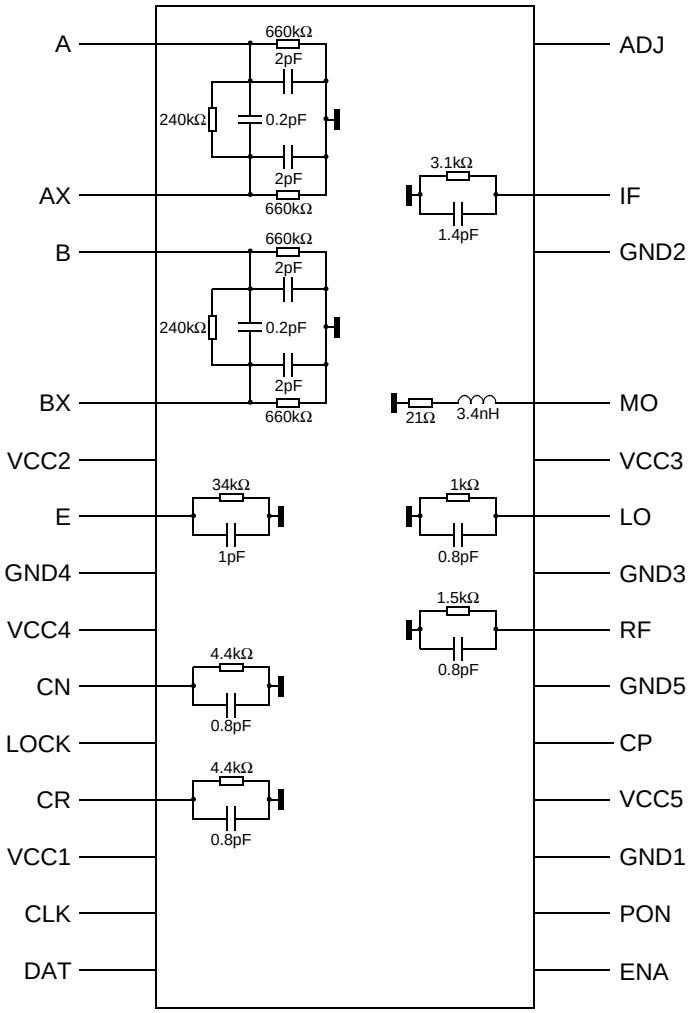
4.8 Charge Pump

The required charge pump polarity, which is set by the CPP bit in the control word (see Circuit Description), depends on the VCO characteristic. If the VCO frequency is an increasing function of the tuning voltage, CPP should be set to 1; if the VCO frequency is a decreasing function of the tuning voltage, CPP should be set to 0.

As the noise bandwidth is not important during capture, it is possible to reduce the capture time by increasing the charge pump current to its maximum value. This is done by switching the LOCK input to LOW (see Circuit Description). Once the loop is locked, LOCK is switched to HIGH, and the charge pump current has its lower, programmed value and a correspondingly lower supply current. The loop filter must be such that an adequate phase margin is maintained for both values of charge pump current. If the LOCK input is not needed, it can be connected to the supply voltage.

4.9 Input/Output Impedances

The AC equivalent circuits given below represent a best-fit approximation to the simulated small-signal impedances over the operational frequency range.



5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values min	Limit Values max	Unit	Remarks	Item
Supply voltage	$V_{CC1,2,3,4}$ V_{CC5}	-0.5 -0.5	5.0 6.0	V V		1
Voltage at any input or output except CP	V_{IO}	-0.5	V_{CC}+0.5 5.0	V V	$V_{CC} \leq 4.5V$ $V_{CC} > 4.5V$	2
Voltage at CP	V_{CP}	-0.5	V_{CC5}+0.5 5.5	V V	$V_{CC5} \leq 5V$ $V_{CC5} > 5V$	3
Differential input voltage	$V_I - V_{IX}$	-2	2	V		4
Output current	I_O		10	mA		5
Storage temperature	T_S	-55	125	°C		6
Thermal Resistance (junction to ambient)	R_{thJA}		152	K/W		7
ESD integrity Pins 21, 23: reduced ESD-integrity > +/-500V due to HF-performance	V_{ESD}	-1000	+1000	V		8

5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description.The AC/DC characteristic limits are not guaranteed.

Table 5-2 Operating Range

Parameter	Symbol	Limit Values min	Limit Values max	Unit	Test Conditions	L	Item
Ambient temperature	T_A	-30	85	°C			1
Supply voltage	$V_{CC1,2,3,4}$ V_{CC5}	2.7 2.7	4.5 5.5	V V			2
IF input frequency	f_{IF}	80	450(1;6)	MHz			3
IF input level	P_{IF}	-19(6)	0	dBm(2)			4
A, AX, B, BX input voltage(2)	V_A, V_B	0.75	V_{CC}– 0.75	V			5
A, AX, B, BX input frequency	f_m	0	10	MHz			6
A/AX, B/BX input level(3)	V_m		1	V_{pp}			7
LO input frequency	f_{LO}	800	2000	MHz			8
LO input level	P_{LO}		0	dBm(2)			9
RF input frequency	f_{RF}	800	2000	MHz			10
RF input level	P_{RF}		0	dBm(2)			11
MO output frequency	f_{MO}	0	450(1)	MHz			12
CN input frequency	f_{CN}	80	450(1;7)	MHz			13
CN input level	P_{CN}	-18(7)	0	dBm(2)			14
CR input frequency	f_{CR}	80	650	MHz			15
CR input level	P_{CR}	-15	0	dBm(2)			16
LOCK output frequency	f_{LOCK}	0	150	MHz	test mode		17
CP output voltage	V_{CP}	0.5	V_{CC5}– 0.8	V			18
CP output frequency	f_{CP}	10	150	MHz			19
LOW input voltage(4)	V_{IL}	0	0.8	V			20
HIGH input voltage(4)	V_{IH}	2.1	V_{CC}	V			21
Clock frequency	f_{CLK}		10	MHz			22
Clock pulse width	T_{CLK}	60		ns			23
Enable pulse width	T_{ENA}	60		ns			24
Data-to-clock set-up time	t_{DCS}	20		ns			25
Data-to-clock hold time	t_{DCH}	10		ns			26
Clock-to-enable set-up time	t_{CES}	20		ns			27
Enable-to-clock set-up time	t_{ECS}	20		ns			28

(1) In the locked state of the loop, f_{MO}, f_{IF} and f_{CN} may not exceed 350MHz. Frequencies between 350 and 450MHz may only occur during capture (see chapter 4).

(2) Power levels are referred to 50Ω.

(3) The limits apply to the instantaneous voltage at A, AX, B, BX relative to ground.

(4) The limit applies to the differential voltage between A and AX or between B and BX.

(5) For LOCK, CLK, DAT, ENA and PON

(6) In the locked state of the loop, the IF input level may not be lower than -15 dBm. Levels down to -17 dBm may only occur during capture. The specified Min. value of -17 dBm is guaranteed only up to 400 MHz. This reduces to -15dBm at 450 MHz.

(7) The specified Min. value of -18 dBm is guaranteed only up to 400 MHz. See also 5.4

5.1.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Table 5-3 AC/DC Characteristics with $V_{VCC1,2,3,4}$ = 2.7 to 4.5 V, V_{VCC5}= 2.7 to 5.5 V, T_A = 25 °C

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Supply current								
Bus	I_{CC1}	0.46	0.62	0.78	mA			1
Modulator	$I_{CC2}+I_E$	12.7	17	21.3	mA			2
Mixer	I_{CC3}	6.0	8.5	11	mA			3
Phase detector and counters	I_{CC4}	9.6	12.8	16.0	mA	T1=0		4
Charge pump(1)	I_{CC5}	4.5 7.7 11.0 14.2	6.0 10.3 14.6 18.9	7.5 12.9 18.2 23.6	mA mA mA mA	CP=00 (1mA) CP=01 (2mA) CP=10 (3mA) CP=11 (4mA)		5
Power down	ΣI_{CC}	0		10	µA	V_{PON}=0.8V		6
Logic inputs LOCK(2), DATA, CLK and ENA								
LOW input current	I_{IL}	-1	0	1	µA	V_{IL}=0.8V		7
HIGH input current	I_{IH}	0	1.4	2.8	µA	V_{IH}=2.1V		8

Table 5-3 AC/DC Characteristics with $V_{VCC1,2,3,4}$ = 2.7 to 4.5 V, V_{VCC5}= 2.7 to 5.5 V, T_A = 25 °C (continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Power-on input								
LOW input current	I_{PONL}	1	2	4	µA	V_{PON}=0.8V		9
HIGH input current	I_{PONH}	3.3	6.6	13.2	µA	V_{PON}=2.1V		10
Power-on delay(3),(6)	t_{PON}		350		ns			11
Modulator								
f_{IF}=180 and 330 MHz, P_{IF}=-8dBm; V_A=V_B=1.35V_{DC}, V_m=1V_{pp} (sine), f_m=10MHz, A lags B by 90°								
DC voltage at IF	V_{IF}	V_{CC}– 0.75	V_{CC}– 0.65	V_{CC}– 0.55	V			12
DC current at A, AX, B, BX	I_A, I_B	2.5	5	10	µA			13
DC offset current at A/AX, B/BX(4)	I_{OS}	-1.5		+1.5	µA			14
DC voltage at ADJ	V_{ADJ}	200	240	280	mV			15
DC current at E	I_E	3.0	4.0	5.0	mA			16
Settling time(5),(6)	t_{MOD}		1.5		µs	100pF at IF and ADJ		17
Output level (at f_{IF}+f_m)(12)	i_E	0.85 -14.4 0.74 -15.6	1.2 -11.4 1.05 -12.6	1.7 -8.4 1.5 -9.6	mA_{rms} dBm mA_{rms} dBm	@ 180 MHz @ 330 MHz		18
Carrier suppression (at f_{IF})	a_{CE}	32	40		dB			19
Single-sideband suppression (at f_{IF}–f_m)	a_{SSB}	35 35	40 40		dB dB	f_{IF}=180MHz, f_{IF}=330MHz, (R_{ADJ} = t.b.d.)		20
Suppression of 3rd-order intermodulation (at f_{IF}–3f_m)	a_{IM3}	44 46	54 56		dB dB	f_{IF}=180MHz f_{IF}=330MHz		21
Third-harmonic suppression (at 3f_{IF}–f_m)	a_{H3}	12 32	17 40		dB	f_{IF}=180MHz f_{IF}=330MHz		22
Phase noise(6),(7)	P_{NE}		126		dBc/ Hz	at f_{IF}+f_m± 400kHz		23
Mixer								
1.) f_{RF} = 900MHz, f_{LO} = 1230MHz *2.)* f_{RF} = 1.9GHz, f_{LO} = 1.72GHz P_{LO} = -10dBm, P_{RF} = -12dBm,								
DC voltage at RF	V_{RF}	V_{CC}– 0.9	V_{CC}– 0.75	V_{CC}– 0.6	V			24
DC voltage at LO	V_{LO}	V_{CC}– 0.75	V_{CC}– 0.65	V_{CC}– 0.55	V			25
DC voltage at MO	V_{MO}	V_{CC}– 1.7	V_{CC}– 1.5	V_{CC}– 1.3	V			26
Settling time(5),(6)	t_{MIX}		1.5		µs	100pF at RF and LO		27

Table 5-3 AC/DC Characteristics with $V_{VCC1,2,3,4}$ = 2.7 to 4.5 V, V_{VCC5}= 2.7 to 5.5 V, T_A = 25 °C (continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Output power into 50Ω(11)	P_{MO}	-12 -10	-9 -7	-6 -4	dBm dBm	condition1 condition2 at f_{RF}–f_{LO}		28
Carrier suppression	a_{CMO}		20		dB	at f_{LO}		29
1dB compression point	P_{RF1dB}	-15 -18	-12 -15	-9 -12	dBm dBm	condition1 condition2		30
Phase noise(6),(7)	P_{NMO}		126		dBc/ Hz	at f_{RF}–f_{LO}± 400kHz		31
Isolation of RF input from LO input(6),(7)	a_{RF}	30			dB			32
Phase detector block(8)								
DC voltage at CN, CR	V_{CN}, V_{CR}	V_{CC}– 0.86	V_{CC}– 0.76	V_{CC}– 0.66	V			33
HIGH output current at LOCK (test mode)	I_{LOCKH}	0.9	1.2	1.5	mA	T=10, N=001, V_{CN}=V_{CC}		34
LOW output current at LOCK (test mode)	I_{LOCKL}	2.3	3.15	4.0	mA	T=10, N=001, V_{CN}=V_{CC}–1.4V		35
Output current at CP in high-impedance state	I_{CPZ}			100	nA	V_{CP}=V_{CC}/2 CP=11		36
Output current in active (source and sink) states(9)	I_{CPA}	 0.8 1.6 2.4 3.2	 1.0 2.0 3.0 4.0	 1.2 2.4 3.6 4.8	 mA mA mA mA	V_{CP}=V_{CC}/2 CP=00 CP=01 CP=10 CP=11		37
Variation of output current with voltage(9)	a_{CPV}			5	%	V_{CP} over operational range		38
Variation of output current with temperature(6),(9)	a_{CPT}			5	%	T_A over operational		39
Source/sink mismatch	a_{CPM}			8	%	V_{CP}=V_{CC}/2		41
Output ripple at f_{CP} when loop is locked(6),(10)	i_{CP}		70		µAp	CP=11 f_{CP}=150MHz		42
Settling time(5),(6)	t_{PD}		1.5		µs	100pF at CN and CR		43
Propagation delay from CN to CP(6)	t_{CP}		1.4		ns			44

■ This value is only guaranteed in lab.

(1) The supply current of the charge pump is the same in the active and high-impedance states.

(2) T1=0.

(3) The bus is ready to receive data a time t_{PON} after the positive edge of PON.

(4) The offset current is the difference between the A and AX (or B and BX) input currents.

(5) The settling time of a block after a software power-up is the time interval between the positive edge of ENA and the point where the parameters of the block are within the specified range. Note that the settling time depends on the time required to charge the external capacitors.

(6) Not measured in production testing.

(7) Test circuit for lab measurement to be defined.

(8) The dynamic testing of the phase detector block is explained in Test Circuit 1.

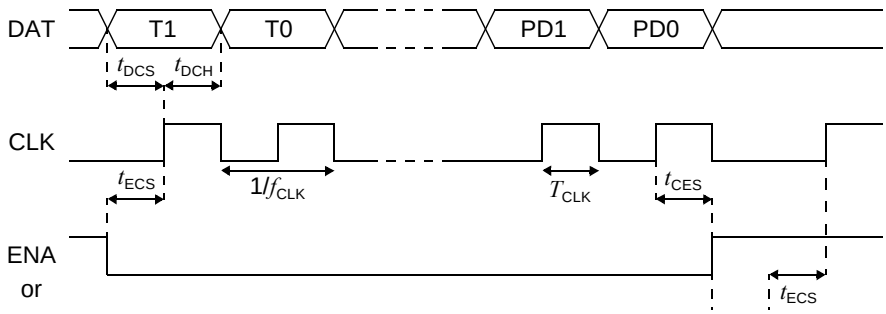
(9) The total variation of the output current (i.e. including production spread and dependence on temperature, supply voltage and output voltage) is $\leq \pm 25\%$.

(10) The output ripple is proportional to the programmed charge pump current.

(11) Mixer output power vs. temperature see 5.4.1

(12) Modulator output power vs. temperature see 5.4.2

5.2 Bus Timing



5.3 Programming Tables

Table 5-4

MSB	bit assignment in control word *) reserved bit												LSB
test		R-counter			N-counter			charge pump			power down		
T1	T0	R2	R1	R0	N2	N1	N0	CPP	CP1	CP0	PD2	PD1	*)

Table 5-5

T1	T0	test mode
0	X	normal operation
1	0	FN fed to LOCK
1	1	FR fed to LOCK

Table 5-6

N2 (R2)	N1 (R1)	N0 (R0)	frequency division ratio N (R)
0	0	0	8
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 5-7

CPP	polarity of charge pump output current
0	current sourced if FN has higher frequency or FN leads
1	current sunk if FN has higher frequency or FN leads

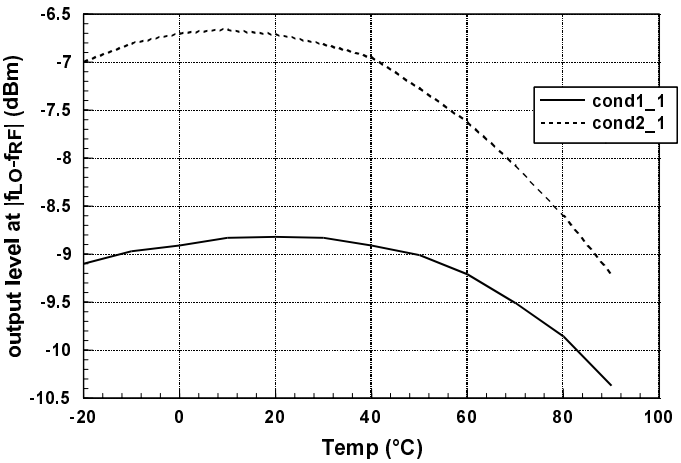
Table 5-8

CP1	CP0	charge pump output current
0	0	1mA
0	1	2mA
1	0	3mA
1	1	4mA

Table 5-9				
PON	**PD0**	**PD1**	**PD2**	**active blocks**
0	x	x	x	Power down
1	x	0	0	bus + mixer
1	x	1	0	bus + mixer + modulator
1	x	1	1	bus + mixer + modulator + phase detector block

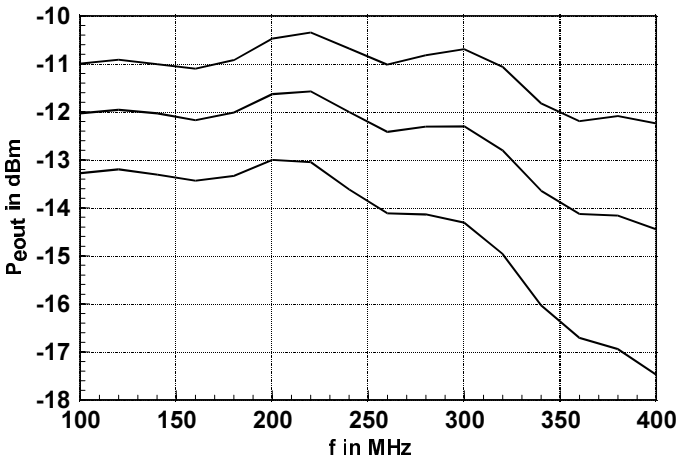
5.4 Typical Temperature Dependencies

1. Temperature Dependence of Mixer Output Level



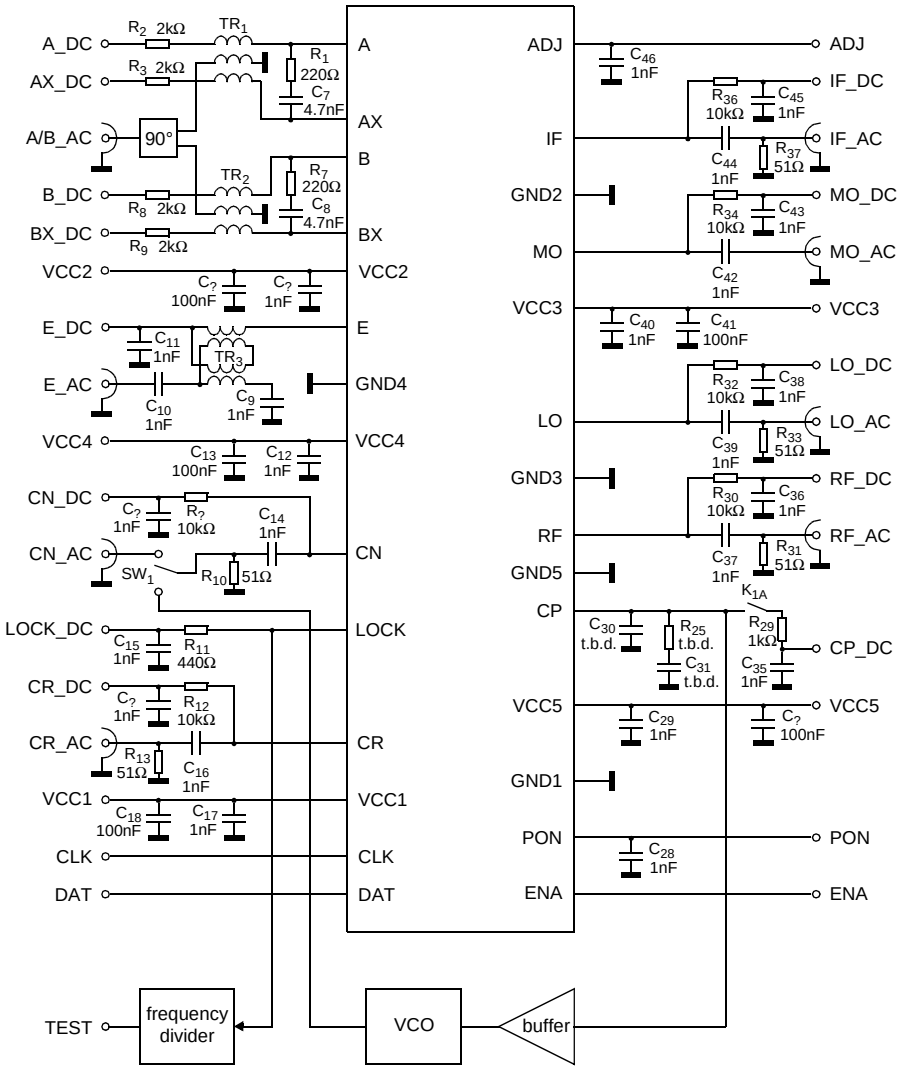
condition 1: f_{RF}=900MHz, f_{LO}=1230MHz, P_{LO}=-10dBm, P_{RF}=-12dBm
condition 2: f_{RF}=1.9GHz, f_{LO}=1.72GHz, P_{LO}=-10dBm, P_{RF}=-12dBm

2. Temperature Dependence of Modulator Output Level



Output power of modulator vs IF frequency at -30°C, 30°C, 85°C from top
P_{IF}=-9dBm, V_A=V_B=1.8VDC, V_m=1V_{pp}, f_m=100kHz, V_{CC}=3.6V, R_{ADJ}=47kOhm

5.5 Test Circuit 1



Note: The dynamic testing of the phase detector block is performed by feeding the output of the VCO to the CN input, so as to form a closed phase-locked loop, and measuring the output frequency of the N-counter (in test mode).