

PIIPM15P12D007

Programmable Isolated IPM

PI-IPM Features:

■ Power Module:

- NPT IGBTs 15A, 1200V
- 10us Short Circuit capability
 - Square RBSOA
 - Low $V_{ce(on)}$ (2.46Vtyp @ 15A, 25°C)
 - Positive $V_{ce(on)}$ temperature coefficient
- Gen III HexFred Technology
 - Low diode V_F (1.86Vtyp @ 15A, 25°C)
 - Soft reverse recovery
- 10mΩ sensing resistors on all phase outputs
 - Thermal coefficient < 50ppm/°C

■ Embedded driving board

- Programmable 40 Mips DSP
- Current sensing feedback from two phases
- Full protection from ground and line to line faults
- UVLO, OVLO on DCbus voltage
- Embedded flyback smps for floating stages (single 15Vdc @ 300mA input required)
- Asynchronous isolated 2.5Mbps serial port for DSP communication and/or programming
- Synchronous isolated 10Mbps serial port for DSP communication and/or programming
- IEEE standard 1149.1 (JTAG port interface) for program downloading and debugging
- Separated turn on / turn off outputs for IGBTs di/dt control
- Hall effect sensors, sin/cos and quadrature encoder interfaces
- On board 64kbits I²C EEPROM

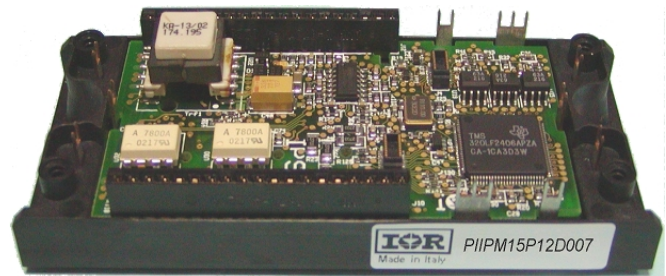
Description

The PIIPM15P12D007 is a fully integrated Intelligent Power Module for high performances Servo Motor Driver applications.

The device core is a state of the art DSP, the TMS320LF2406A at 40 Mips, interfaced with a full set of peripherals designed to handle all analog feedback and control signals needed to correctly manage the power section of the device. A 64kbits EEPROM is also available to store calibration data.

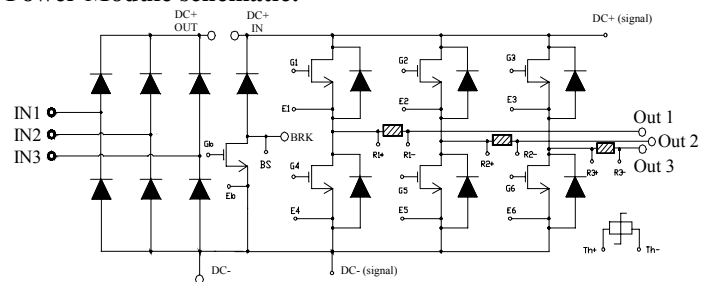
The PIIPM has been designed and tailored to implement internally all functions needed to close the current loop of a high performances servo motor driver, a basic software is already installed in the DSP and the JTAG allows the user to easily develop and download its own proprietary algorithm.

Package:



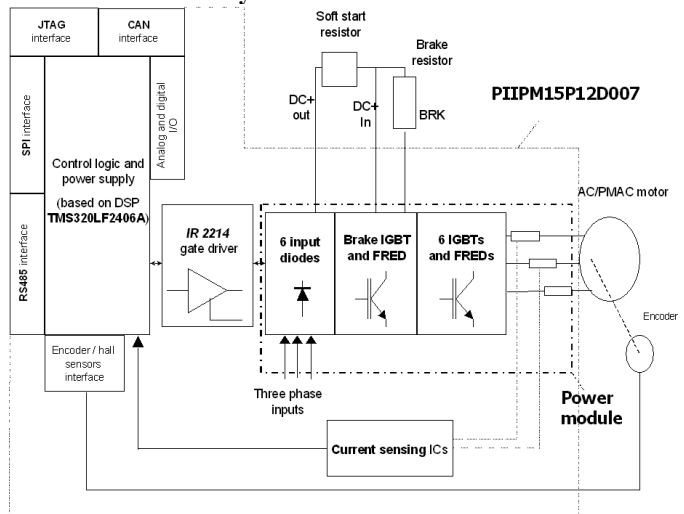
PIIPM – BBI (EconoPack 2 outline compatible)

Power Module schematic:



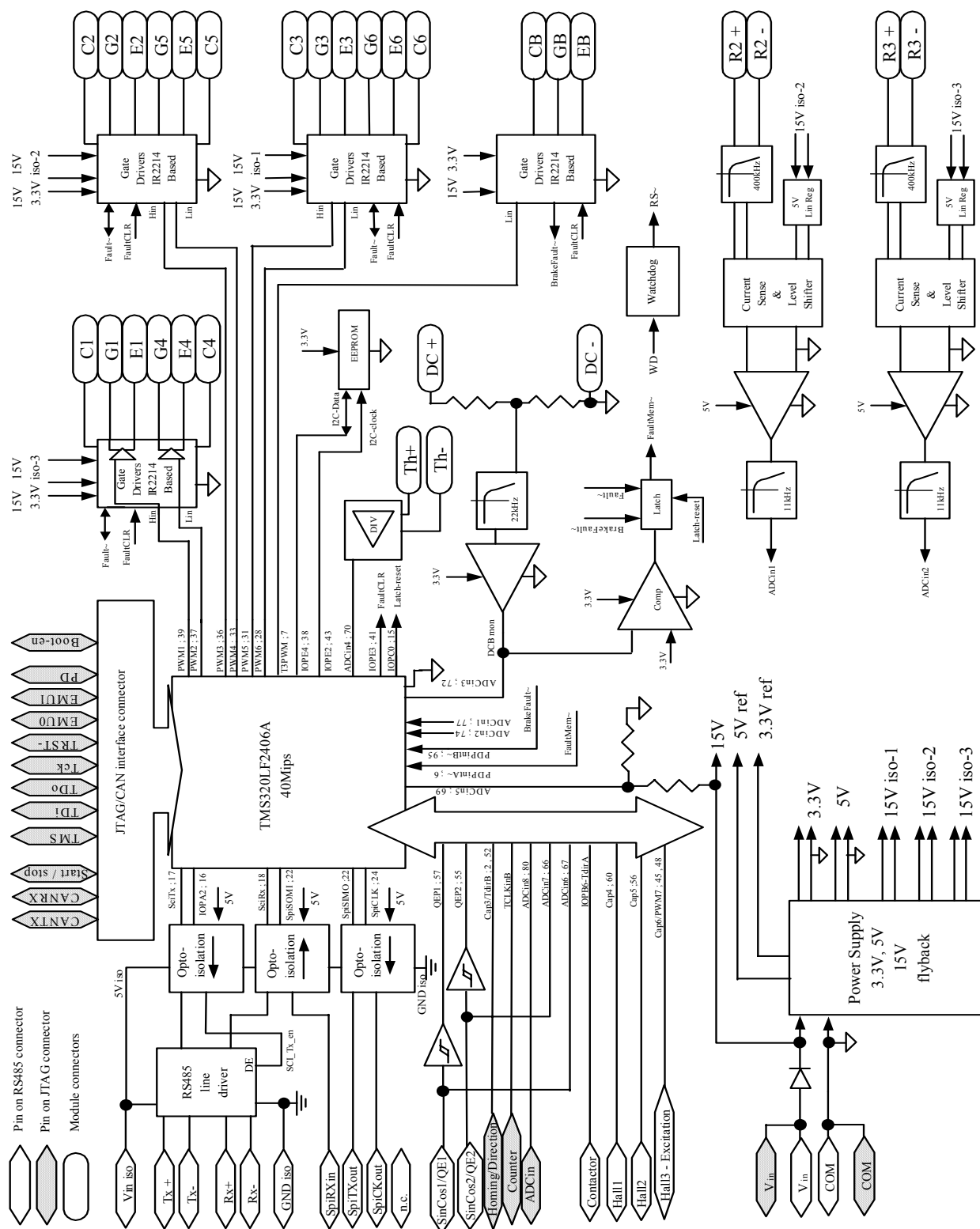
Input bridge, brake and three phases inverter (BBI) with current sensing resistors on all output phases and thermistor

PIIPM15P12D007 System Block Schematic:



The device comes in the EMPTM package, fully compatible in length, width and height with the popular EconoPack 2 outline.

Embedded driving board block schematic



Signal pins on RS485 connector

Symbol	Lead Description	State	Connector pin number
Tx+	RS485 Trasmmitter Non inverting Driver Output	Output	1
Tx-	RS485 Trasmmitter Inverting Driver Output	Output	2
Rx-	RS485 Receiver Inverting Driver Input	Input	3
Rx+	RS485 Receiver Non inverting Driver Input,	Input	4
SpiCKout	SPI clock output (GND iso referenced)	Output	5
Vin iso	External 5V supply voltage for opto-couplers and line driver supply	Input	6
GND iso	Extenal 5V supply ground reference for opto-couplers and line driver supply	Input	7
SpiTXout	SPI transmitter output (GND iso referenced)	Output	8
SpiRXin	SPI receiver input (GND iso referenced)	Input	10
SinCos1 / QE1	SinCos encoder input 1 / Quadrature encoder input 1	Input	11
SinCos2 / QE2	SinCos encoder input 2 / Quadrature encoder input 2	Input	12
Contactor	General purpose I/O	I/O	13
Hall1	Hall effect sensor input 1	Input	14
Hall2	Hall effect sensor input 2	Input	15
Hall3 / Excitation	Hall effect sensor input 3 / Resolver excitation	I/O	16
Vin	External 15V supply voltage. Internally referred to DC bus minus pin (DC -)	Input	17-18
COM	External 15V supply ground reference. This pin is directly connected to DC -	Input	19-20

Signal pins on IEEE1149.1 JTAG connector

CAUTION: DO NOT APPLY DC BUS VOLTAGE WHEN JTAG INTERFACE IS CONNECTED, SEVER DAMAGE MAY OCCUR ON POWER MODULE AND ON YOUR EQUIPMENT!

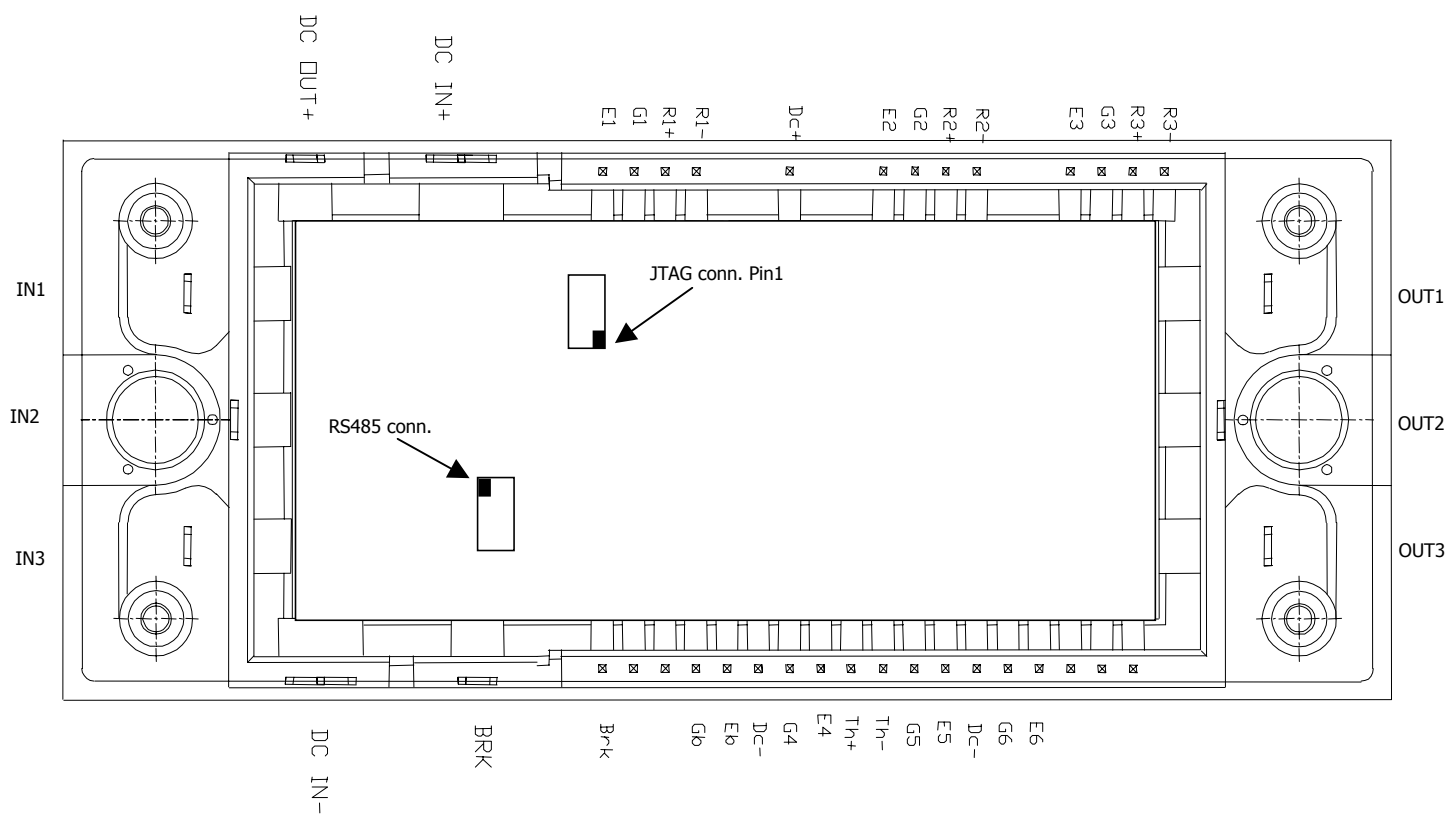
Symbol	Lead Description	State	Connector pin number
PD	Presence detect. Indicates that the emulation cable is connected and that the PIIPM logic is powered up. PD is tied to the DSP 3.3V supply through a 1k resistor.	Output	3
Homing / Direction	Homing signal / Counter direction	Input	4
Start/Stop	Start/Stop signal	Input	5
CAN Tx	CAN transmitter signal	Output	6
CAN Rx	CAN receiver signal	Input	7
EMU1/OFF~	Emulation pin 1	I/O	8

Counter	Counter signal	Output	9
EMU0	Emulation pin 0	I/O	10
TRST~	JTAG test reset	Input	13
TMS	JTAG test mode select	Input	14
TDO	JTAG test data output	Output	15
TDI	JTAG test data input	Input	16
TCKRET	JTAG test clock return. Test clock input to the emulator. Internally short circuited to TCK.	Output	17
TCK	JTAG test clock. TCK is a 10MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Input	18
Boot-En	Boot ROM enable. This pin is sampled during DSP reset, pulling it low enables DSP boot ROM (Flash versions only). 47k internal pull up.	Input	19
ADCin	General purpose analog input	Input	20
COM	External 15V supply ground reference. This pin is directly connected to DC -	input	1-11
Vin	External 15V supply voltage. Internally referred to DC bus minus pin (DC-)	Input	2-12

Following pins are intended for signal communication between driving board and power module only, though here described for completeness, they are on purpose not available to the user.

Symbol	Lead Description	Pin number
DC +	DC Bus plus input signal	Lateral connectors on embedded driving board
DC -	DC Bus minus input signal (internally connected to COM)	
Th +	Thermal sensor positive input	
Th -	Thermal sensor negative input (internally connected to COM)	
G1/2/3	Gate connections for high side IGBTs	
E1/2/3	Emitter connections for high side IGBTs (Kelvin points)	
R1/2/3 +	Output current sensing resistor positive input (IGBTs emitters 1/2/3 side, Kelvin points)	
R1/2/3 -	Output current sensing resistor negative input (Motor side, Kelvin points)	
G4/5/6	Gate connections for low side IGBTs	
E4/5/6	Emitter connections for low side IGBTs (Kelvin points)	
Gb	Gate connections for brake IGBT	
Eb	Emitter connection for brake IGBT (Kelvin point)	
Brk	Collector connection for brake IGBT (Kelvin point)	

Power Module Frame Pins Mapping



Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$)

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur.

All voltage parameters are absolute voltages referenced to V_{DC-} , all currents are defined positive into any lead.

Thermal Resistance and Power Dissipation ratings are measured at still air conditions.

	Symbol	Parameter Definition		Min.	Max.	Units
Inverter	V_{DC}	DC Bus Voltage		0	1000	V
	V_{CES}	Collector Emitter Voltage		0	1200	
	$I_C @ 100^{\circ}\text{C}$	IGBTs continuous collector current ($T_C = 100^{\circ}\text{C}$, fig. 1)			15	A
	$I_C @ 25^{\circ}\text{C}$	IGBTs continuous collector current ($T_C = 25^{\circ}\text{C}$, fig 1)			30	
	I_{CM}	Pulsed Collector Current (Fig. 3, Fig. CT.5)			60	
	$I_F @ 100^{\circ}\text{C}$	Diode Continuous Forward Current ($T_C = 100^{\circ}\text{C}$)			15	
	$I_F @ 25^{\circ}\text{C}$	Diode Continuous Forward Current ($T_C = 25^{\circ}\text{C}$)			30	
	I_{FM}	Diode Maximum Forward Current			60	
	V_{GE}	Gate to Emitter Voltage		-20	+20	V
	$P_D @ 25^{\circ}\text{C}$	Power Dissipation (One transistor)			140	W
	$P_D @ 100^{\circ}\text{C}$	Power Dissipation (One transistor, $T_C = 100^{\circ}\text{C}$)			55	
Bridge	V_{RRM}	repetitive peak reverse voltage ($T_J = 150^{\circ}\text{C}$)			1400	V
	V_{RSM}	non repetitive peak reverse voltage			1500	
	I_o	Diode Continuous Forward Current ($T_C = 100^{\circ}\text{C}$, 120° Rect conduction angle)			45	A
	I_{FSM}	One-cycle forward. Non-repetitive on state surge current ($t=10\text{ms}$, Initial $T_J = T_{J\text{MAX}}$)	100% V_{RRM} reapplied		225	
			No voltage reapplied		270	
	I^2t	Current I^2t for fusing ($t=10\text{ms}$, Initial $T_J = T_{J\text{MAX}}$)	100% V_{RRM} reapplied		253	A^2s
			No voltage reapplied		365	
	$I^2\sqrt{t}$	Current $I^2\sqrt{t}$ for fusing ($t=0.1$ to 10ms , no voltage reapplied, Initial $T_J = T_{J\text{MAX}}$)			3650	$\text{A}^2\sqrt{\text{s}}$
Embedded Driving Board	V_{in}	Non isolated supply voltage (DC- referenced)		-20	20	V
	V_{in-iso}	Isolated supply voltage (GND iso referenced)		-5	5.5	
	R_x	RS485 Receiver input voltage (GND iso referenced)		-7	12	
	T_{A-EDB}	Operating Ambient Temperature Range		-25	+70	$^{\circ}\text{C}$
	$T_{STG-EDB}$	Board Storage Temperature Range		-40	+125	
	$V_{ISO-CONT R485}$	Input-Output Continuous Withstand Voltage ($RH \leq 50\%$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$)		AC DC	800 1000	V
	$V_{ISO-TEMP RS485}$	Input-Output Momentary Withstand Voltage ($RH \leq 50\%$, $t = 1 \text{ min}$, $T_A = 25^{\circ}\text{C}$)	RMS	2500		
Power Module	MT	Mounting Torque			3.5	Nm
	T_J	Operating Junction Temperature		-40	+150	$^{\circ}\text{C}$
	T_{STG}	Storage Temperature Range		-40	+125	
	V_{c-iso}	Isolation Voltage to Base Copper Plate		-2500	+2500	V

Electrical Characteristics: Inverter

For proper operation the device should be used within the recommended conditions.

T_J = 25°C (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions	Fig.
V _{(BR)CES}	Collector To Emitter Breakdown Voltage	1200			V	V _{GE} = 0V, I _C = 250μA	
ΔV _{(BR)CES} / ΔT	Temperature Coeff. of Breakdown Voltage		+1.2		V/°C	V _{GE} = 0V, I _C = 1mA (25 - 125 °C)	
V _{CE(on)}	Collector To Emitter Saturation Voltage		2.46	2.66	V	I _C = 15A, V _{GE} = 15V	5, 6
			3.43	4.00		I _C = 30A, V _{GE} = 15V	7, 9
			2.98	3.35		I _C = 15A, V _{GE} = 15V, T _J = 125 °C	10, 11
V _{GE(th)}	Gate Threshold Voltage	4.0	5.0	6.0	V	V _{CE} = V _{GE} , I _C = 250μA	12
ΔV _{GE(th)} / ΔT _J	Temp. Coeff. of Threshold Voltage		-1.2		mV/°C	V _{CE} = V _{GE} , I _C = 1mA (25 - 125 °C)	
g _{fe}	Forward Trasconductance	8	10	12	S	V _{CE} = 50V, I _C = 7.5A, PW = 80μs	
I _{CES}	Zero Gate Voltage Collector Current			125	μA	V _{GE} = 0V, V _{CE} = 1200V	
			162	337		V _{GE} = 0V, V _{CE} = 1200V, T _J = 125 °C	
				1000		V _{GE} = 0V, V _{CE} = 1200V, T _J = 150 °C	
V _{FM}	Diode Forward Voltage Drop		1.86	2.17	V	I _C = 15A	8
			2.01	2.40		I _C = 15A, T _J = 125 °C	
I _{GES}	Gate To Emitter Leakage Current			±100	nA	V _{GE} = ± 20V	
R1/2/3	Sensing Resistors	9.9	10	10.1	mΩ		

Electrical Characteristics: Bridge

For proper operation the device should be used within the recommended conditions.

T_J = 25°C (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions	Fig.
V _{FM}	Forward Voltage Drop			1.45	V	t _p = 400μs, I _{pk} = 45A	24
			1.18			t _p = 400μs, I _{pk} = 15A	
V _{F(TO)}	Threshold voltage		0.78		V	T _J = 125 °C	
I _{rm}	Reverse Leakage Current			-	mA	T _J = 25 °C	
				5		T _J = 125 °C	

Switching Characteristics: Inverter

For proper operation the device should be used within the recommended conditions.

T_J = 25°C (unless otherwise specified)

Symbol	Parameter Definition	Min	Typ	Max	Units	Test Conditions	Fig.
Q _g	Total Gate Charge (turn on)		84	127	nC	I _C = 15A	23 CT1
Q _{ge}	Gate – Emitter Charge (turn on)		10	15		V _{CC} = 600V	
Q _{gc}	Gate – Collector Charge (turn on)		41	61		V _{GE} = 15V	
E _{on}	Turn on Switching Loss		Tbd	Tbd	μJ	I _C = 15A, V _{CC} = 600V, T _J = 25 °C	CT4
E _{off}	Turn off Switching Loss		Tbd	Tbd		V _{GE} = 15V, R _G = 10Ω, L = 200μH	WF1
E _{tot}	Total Switching Loss		Tbd	Tbd		Tail and Diode Rev. Recovery included	WF2
E _{on}	Turn on Switching Loss		Tbd	Tbd	μJ	I _C = 15A, V _{CC} = 600V, T _J = 125 °C	13, 15 CT4 WF1 WF2
E _{off}	Turn off Switching Loss		Tbd	Tbd		V _{GE} = 15V, R _G = 10Ω, L = 200μH	
E _{tot}	Total Switching Loss		Tbd	Tbd		Tail and Diode Rev. Recovery included	
td (on)	Turn on delay time		Tbd	Tbd	ns	I _C = 15A, V _{CC} = 600V, T _J = 125 °C V _{GE} = 15V, R _G = 10Ω, L = 200μH	14,16 CT4 WF1 WF2
Tr	Rise time		Tbd	Tbd			
td (off)	Turn off delay time		Tbd	Tbd			
Tf	Fall time		Tbd	Tbd			
C _{ies}	Input Capacitance		1100		pF	V _{CC} = 30V	22
C _{oes}	Output Capacitance		110			V _{GE} = 0V	
C _{res}	Reverse Transfer Capacitance		40			f = 1MHz	
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T _J = 150 °C, I _C = 60A, V _{GE} = 15V to 0V V _{CC} = 1000V, V _p = 1200V, R _G = 5Ω	4 CT2
SCSOA	Short Circuit Safe Operating Area	10			μs	T _J = 150 °C, V _{GE} = 15V to 0V V _{CC} = 1000V, V _p = 1200V, R _G = 5Ω	CT3 WF4
E _{REC}	Diode reverse recovery energy		930	1200	μJ	T _J = 125 °C I _F = 15A, V _{CC} = 600V, V _{GE} = 15V, R _G = 10Ω, L = 200μH	17,18 19,20 21 CT4 WF3
T _{rr}	Diode reverse recovery time		300		ns		
I _{rr}	Peak reverse recovery current		12	15	A		
R _{thJ-C-T}	Each IGBT to copper plate thermal resistance			0.9	°C/W	See also fig. 25, 26	25,26
R _{thJ-C-D}	Each Diode to copper plate thermal resistance			1.54	°C/W		
R _{thC-H}	Module copper plate to heat sink thermal resistance. Silicon grease applied = 0.1mm			0.03	°C/W		
P _{diss}	Total Dissipated Power		Tbd		W	I _C = 1.5A, V _{DC} = 530V, f _{sw} = 8kHz, T _C = 55 °C	PD1
			Tbd			I _C = 3A, V _{DC} = 530V, f _{sw} = 8kHz, T _C = 55 °C	PD2
			Tbd			I _C = 3A, V _{DC} = 530V, f _{sw} = 16kHz T _C = 55 °C,	PD3
			Tbd			I _C = 7A, V _{DC} = 530V, f _{sw} = 4kHz, T _C = 55°C	

Electrical Characteristics: Embedded Driving Board (EDB) communication ports

For proper operation the device should be used within the recommended conditions.

V_{in} = 15V, V_{in-iso} = 5V, T_A = 0 to 55°C, T_C = 75°C (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions	Type	Conn.
V _{in}	EDB Input supply Voltage	12	15	18	V		Non isolated Supply	RS485
I _{supp}	EDB Input Supply Current		150	250	mA	V _{DC} = 600V, f _{PWM} = 16kHz		
V _{in iso}	EDB isolated supply voltage	4.5	5	5.5	V		Isolated supply	
I _{q. iso}	EDB isolated quiescent supply current		9	15	mA	R _{x+} = +5V, R _{x-} = 0V SPIR _{xIn} open		
I _{supp. iso}	EDB isolated supply current	10	15	22	mA	SPIR _{xIn} low R _{x+} = 0V, R _{x-} = +5V Tx+ and Tx- open		
		50	55	62	mA	SPIR _{xIn} low R _{x+} = 0V, R _{x-} = +5V Tx+ and Tx- on 120Ω		
V _{DO-TX}	Differential Driver Output Voltage	2			V	Rload = 120 Ω	RS485 port	
V _{CO-TX}	Driver Common mode output voltage			3	V			
V _{DI-RX}	Receiver Input Differential Threshold Voltage	- 0.2		0.2	V	- 7V ≤ V _{CM} ≤ +12V		
R _{IN-RX}	Receiver Input Resistance		120		Ω			
f _{MAX}	RS485 maximum data rate			2.5	Mbps			
SpiR _{xIn}	Logic High Input Voltage	3.8			V		SPI port	
	Logic Low Input Voltage			1.0	V			
	Logic Low Input Current			-5	mA			
SpiT _x Out SpiC _k Out	Logic Low Output Voltage			0,8	V	I _{out} = -510μA		
				1,2	V	I _{out} = -1,2mA		
	Logic High Output Voltage	2.4			V	I _{out} = 3mA		
TMS,TDI,TDO TCK,TRST- EMU0 EMU1/OFF~ PD	JTAG interface pins (CAUTION: DO NOT APPLY DC BUS VOLTAGE WHEN JTAG INTERFACE IS CONNECTED, SEVER DAMAGE MAY OCCUR ON POWER MODULE AND ON YOUR EQUIPMENT!)	Please see TMS320LF2406A datasheet from Texas Instruments and V _{PD} specifications				Directly connected from DSP to connector pins. EMU0 and EMU1 with 4.7k internal pull up.	JTAG	JTAG
V _{PD}	Presence detect voltage	3.2	3.3	3.4	V	I _{PD} = -100μA	JTAG	
V _{Boot En}	Boot ROM enable input voltage			0.5	V	Active low	JTAG	
I _{Boot-En}	Boot ROM enable input current			- 100	μA			
CAN Tx	Logic Low Output Voltage			0.8	V	I _{out} = - 780μA	CAN port	
	Logic High Output Voltage	2.4			V	I _{out} = 860μA		
CAN Rx	Logic Low Input Voltage			0.8	V			
	Logic High Input Voltage	2.4			V			

~ indicates active low signals

AC Electrical Characteristics: Embedded Driving Board (EDB)

DSP pins mapping

For proper operation the device should be used within the recommended conditions.

V_{in} = 15V, V_{in-iso} = 5V, T_A = 0 to 55°C, T_C = 75°C (unless otherwise specified)

Symbol	Parameter Definition		Min.	Typ.	Max.	Units	Test Conditions	DSP name; pin N
V _{DCgain}	DC bus voltage feedback partition coefficient		2.39	2.44	2.49	mV/V		ADCIN03 ; 72
V _{DCpole}	DC bus voltage feedback second order filter		-	22	-	kHz		
V _{DC-OVth}	DC bus voltage over-voltage threshold		870	920	970	V		PDPINTA~ ; 6
V _{TH25C}	Thermal sensor voltage feedback at 25 °C (Fig. TF1)		2.65	2.75	2.85	V		ADCIN04 ; 70
V _{TH100C}	Thermal sensor voltage feedback at 100 °C (Fig. TF1)		1.04	1.09	1.14	V		
V _{in-gain}	Input voltage feedback partition coefficient		125	128	131	mV/V		ADCIN05 ; 69
V _{in-pole}	Input voltage feedback filter pole		1600	1700	1800	Hz		
I _{ph-GAIN}	Current feedback gain		78	80	82	mV/A	all two phases	ADCIN01: 77 ADCIN02: 74
I _{ph-pole}	Current feedback filter pole		9.8	10.9	12	kHz		
I _{ph-LAT}	Current feedback signal delay				5	μs		
I _{ph-Zero}	Zero current input voltage level		1.62	1.65	1.68	V		
V _{ce_sc}	Vce Short Circuit Threshold detection			7.4		V	all phases	PDPINTA~ ; 6
I _{SC-DEL}	Short Circuit detection delay time			3	6	μs		
WD	External watchdog timeout (see also RS~ signal), please see WD internal signal for more details		0.9			Sec		IOPC1 ; 85
ADCin	Generic purpose analog Input		0		3.3	V		ADCIN08 ; 80
	Generic purpose analog input filter pole			4.13		kHz		
SinCos1/QE1	Analog input 1 for sincos resolver		0		3.3	V	See also QEP1 internal signal	ADCIN06 ; 67
	Analog input for sincos resolver filter pole			4.13		kHz		
	QEP1: internal digital signal of QE1	High level threshold	2,4			V		QEP1 ; 57
		Low level threshold			1	V		
SinCos2/QE2	Analog input 2 for sincos resolver		0		3.3	V	See also QEP2 internal signal	ADCIN07;66
	Analog input for sincos resolver filter pole			4.13		kHz		
	QEP2: internal digital signal of QE1	High level threshold	2,4			V		QEP2 ; 55
		Low level threshold			1	V		
COM	DSP Ground		3, 5, 13, 14, 19, 26, 27, 29, 32, 34, 46, 53,55, 58, 63, 65, 68, 71, 73, 75, 76, 78,79, 81, 84, 90, 97					
3.3V	DSP 3.3V supply		4, 10, 20, 30, 35, 47, 54, 59, 64, 91, 98					
Floating	Not connected to anything		12, 23, 88, 25, 42, 44, 51					

~ indicates active low signals

Other DSP pins mapping to the connector

Symbol	Signal Definition	DSP name ; pin N	Comments	Connector
Hall1	Hall effect sensor input 1	CAP4/QEP3/IOPE7 ; 60	Digital Input. See elec. characteristic of I/O pins	RS485
Hall2	Hall effect sensor input 2	CAP5/QEP3/IOPF0 ; 56	Digital Input. See elec. characteristic of I/O pins	
Hall3 / Excitation	Hall effect sensor input 3 / Resolver excitation	PWM7/IOPE1, CAP6/IOPF1 ; 45, 48	Digital I/O, Output is type G3. See electrical characteristics of I/O pins	
Contactor	General purpose I/O	IOPB6 ; 11	Digital I/O, Output is type G3. See electrical characteristics of I/O pins	
CAN Tx	CAN transmit data	CANTX ; 50		JTAG
CAN Rx	CAN receive data	CANRX ; 49		
Homing/Direction	Homing signal/ Counter direction	TDIRB/IOPF4, CAP3/IOPA5 ; 2, 52	Avoid electrical conflicts between these two pins	
Start/Stop	Start/Stop signal	IOPF6 ; 92	Digital Input. See elec. Characteristic of I/O pins	
Boot En~	Boot ROM enable signal	BOOT_EN~ ; 86	See also EDB electrical characteristics	
Counter	Counter signal	TCLKINB ; 89	Digital Input. See elec. Characteristics of I/O pins	

These signals are internal only

Symbol	Signal Definition	DSP name ; pin N	Comments
PWM1	Out 1 high side IGBT gate drive signal	PWM1 ; 39	DSP Event Manager A output
PWM2	Out 1 low side IGBT gate drive signal	PWM2 ; 37	DSP Event Manager A output
PWM3	Out 2 high side IGBT gate drive signal	PWM3 ; 36	DSP Event Manager A output
PWM4	Out 2 low side IGBT gate drive signal	PWM4 ; 33	DSP Event Manager A output
PWM5	Out 3 high side IGBT gate drive signal	PWM5 ; 31	DSP Event Manager A output
PWM6	Out 3 low side IGBT gate drive signal	PWM6 ; 28	DSP Event Manager A output
Brake	Brake IGBT gate drive signal	T3PWM ; 7	DSP Event Manager B output
SpiTXout	SpiTx output	SPISIMO ; 21	These signal are optically isolated. See also EDB electrical characteristics
SpiRXout	SpiRx input	SPISOMI ; 22	
SpiCKout	SpiClk output	SPICLK ; 24	
Ref3.3V	3.3V reference voltage	VREFHI, VCCA ; 82, 83	3.3V reference and supply voltage for ADC converter
5V supp.	Flash programming voltage pin	VCCP ; 40	Supplied by the embedded flyback regulator
Tx	SCI transmit data	SCITXD ; 17	Drives Tx+ and Tx- through the opto-isolator and the line driver
Rx	SCI receive data	SCIRXD ; 18	Driven by Rx+ and Rx- through the opto-isolator and the line driver
SCI_Tx_en	SCI transmitter enable	IOPA2 ; 16	Enable the SCI line driver through an opto-isolator
Latch-reset	System general fault output reset signal	IOPC0 ; 15	LFAULT Reset signal, to be activated via software after a fault or system boot
FaultCLR		IOPE3 ; 41	Gate driver reset, to be activated via software after a short-circuit or system boot

RS~	DSP reset input signal (see also WD signal)	RS~ ; 93	Forces a DSP reset if WD signal holds too long (see also EDB electrical char.)
Xtal1	PLL oscillator input pin	XTAL1 ; 87	A 10Mhz oscillator at 100ppm frequency stability feeds this pin.
PLLF1	PLL filter input 1	PFFL ; 9	PLL filter for 40Mhz DSP clock frequency
PLLF2	PLL filter input 2	PLLF2 ; 8	PLL filter for 40Mhz DSP clock frequency
FaultMem~	System general fault input	PDPINTA~ ; 6	Activated by short circuits on output phases or brake IGBT and by DC bus over-voltage comparator. Latched signal, see also Latch-reset
BrakeFault~	Brake Protection Interrupt signal	PDPINTB~ ; 95	Activated by short circuits on brake
QEP1	Square wave of SinCos1/QE1	QEP1 ; 57	Internal Schmitt trigger, see also AC electrical characteristic
QEP2	Square wave of SinCos2/QE2	QEP2 ; 55	Internal Schmitt trigger, see also AC electrical characteristic
WD	Output signal for external watchdog	IOPC1 ; 85	WD = high impedance, external watchdog is disabled
			WD = high or WD = low, external watchdog is enabled and WD has to be periodically triggered by positive or negative transition. When the supervising system fails to retrigger the ext. watchdog within the time shown on AC electrical Characteristics, RS~ signal becomes active.

~ indicates active low signals

64kbits I²C EEprom (please see Microchip 24LC4 for more specifications)

Symbol	Signal Definition	DSP name ; pin N	Comments
I ² C - Clock	I ² C - Clock	IOPE2 ; 43	Connected to the I ² C EEPROM
I ² C - Data	I ² C - Clock	IOPE4 ; 38	Connected to the I ² C EEPROM

Electrical characteristic of digital inputs and outputs.

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions
Input: VIH	Logic high, generic input voltage	2.4			V	
Input: VIL	Logic low, generic input voltage			0.8	V	
Output Type G1	VOH	2.4			V	I _{out} = 700μA
	VOL			0.8	V	I _{out} = - 700μA
Output Type G2	VOH	2.4			V	I _{out} = 850 μA
	VOL			0.8	V	I _{out} = - 850 μA
Output Type G3	VOH	2.4			V	I _{out} = 950 μA
	VOL			0.8	V	I _{out} = -950 μA

Fig. 1 – Maximum DC collector Current vs. case temperature

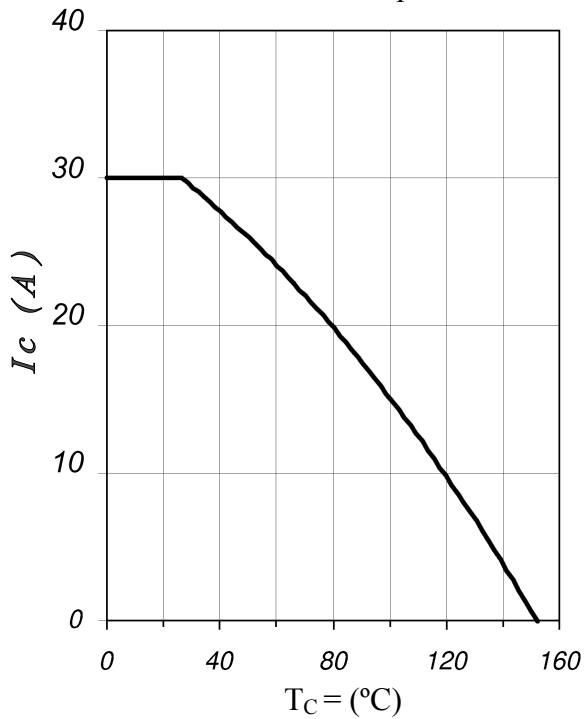


Fig. 2 – Power Dissipation vs. Case Temperature

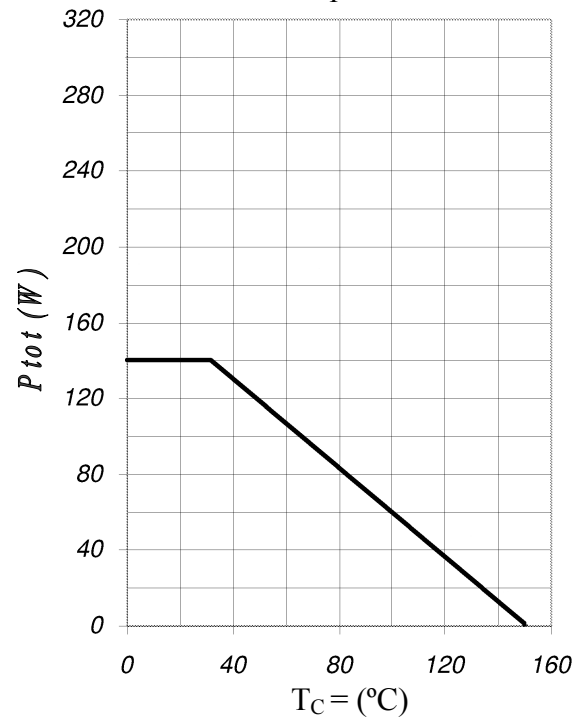


Fig. 3 – Forward SOA
 $T_C = 25^{\circ}\text{C}$; $T_j \leq 150^{\circ}\text{C}$

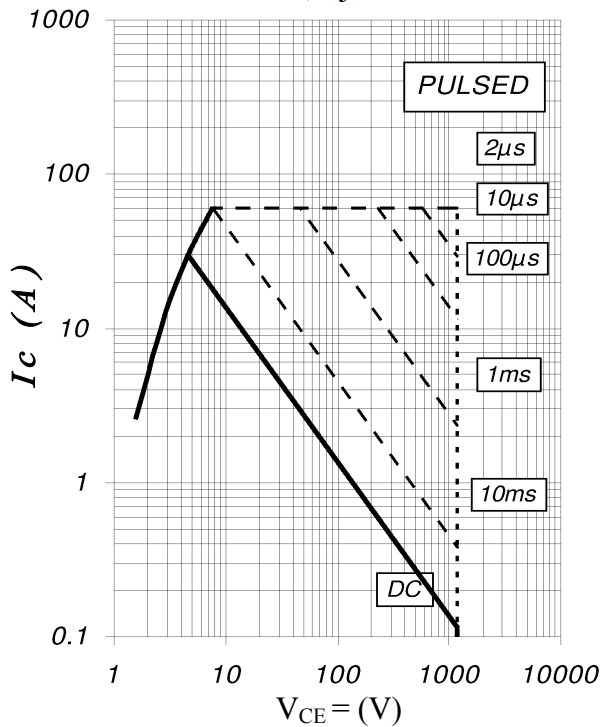


Fig. 4 – Reverse Bias SOA
 $T_j = 150^{\circ}\text{C}$, $V_{GE} = 15\text{V}$

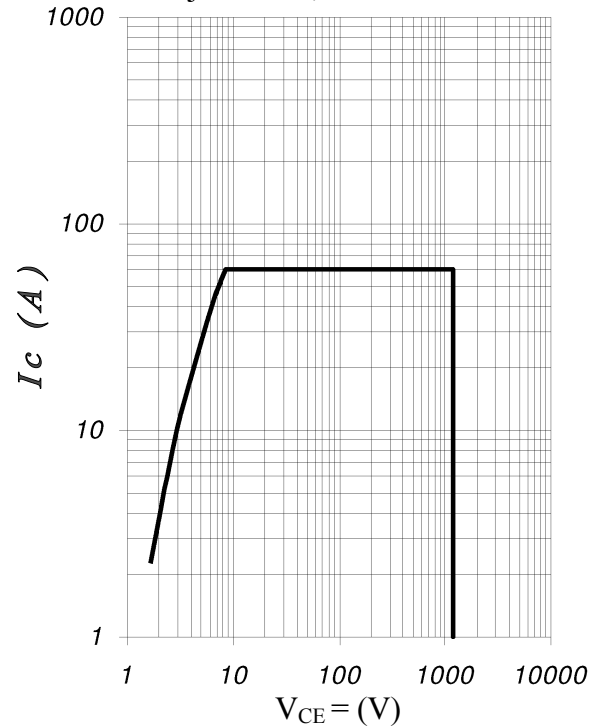


Fig. 5 – Typical IGBT Output Characteristics
 $T_j = -40^{\circ}\text{C}$; $t_p = 300\mu\text{s}$

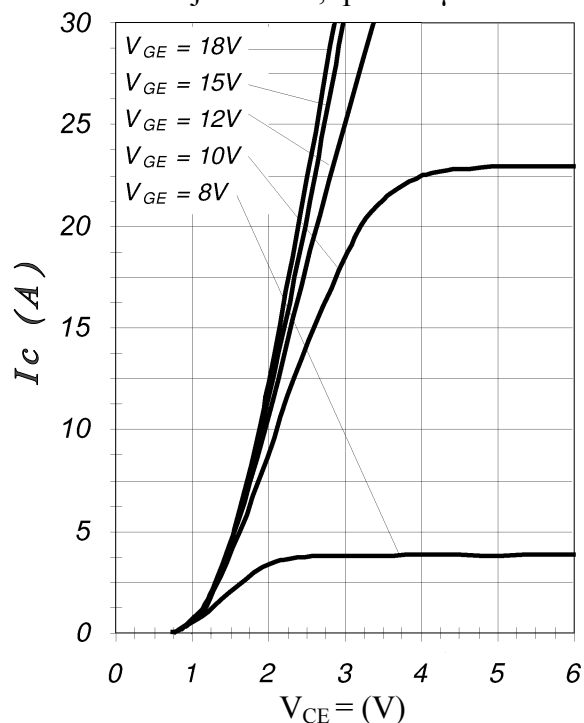


Fig. 6 – Typical IGBT Output Characteristics
 $T_j = 25^{\circ}\text{C}$; $t_p = 300\mu\text{s}$

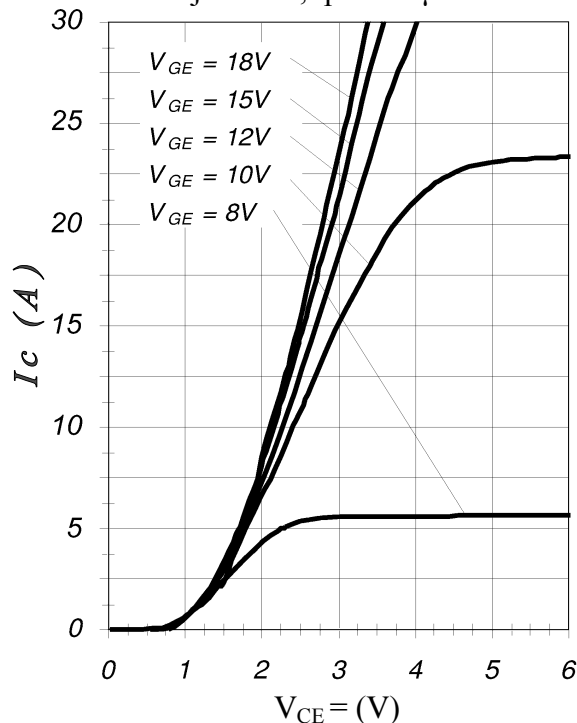


Fig. 7 – Typical IGBT Output Characteristics
 $T_j = 125^{\circ}\text{C}$; $t_p = 300\mu\text{s}$

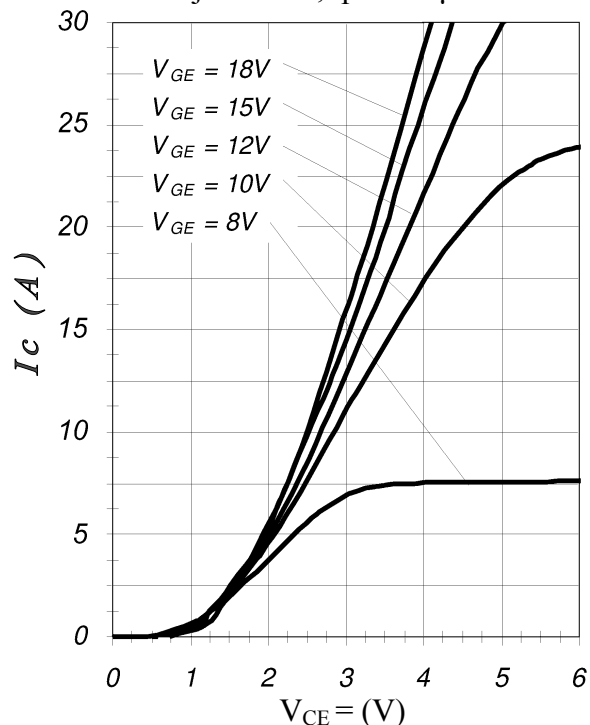


Fig. 8 – Typical Diode Forward Characteristics
 $t_p = 300\mu\text{s}$

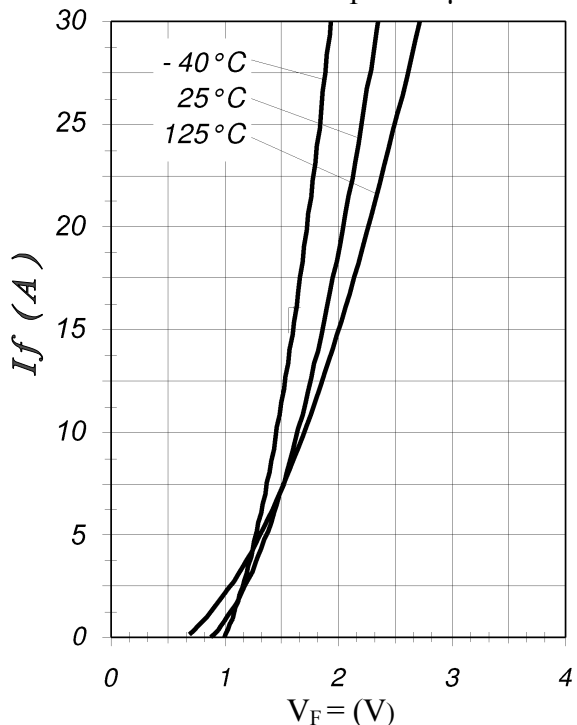


Fig. 9 – Typical V_{CE} vs. V_{GE}
 $T_j = -40^\circ\text{C}$

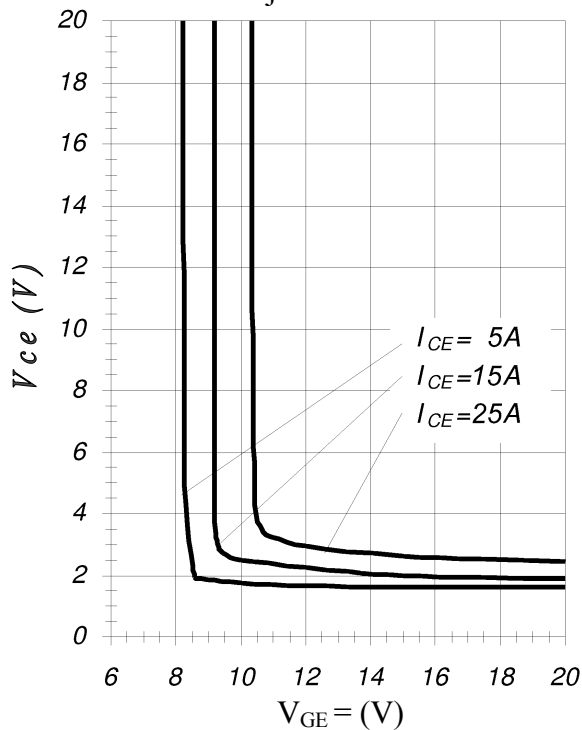


Fig. 10 – Typical V_{CE} vs. V_{GE}
 $T_j = 25^\circ\text{C}$

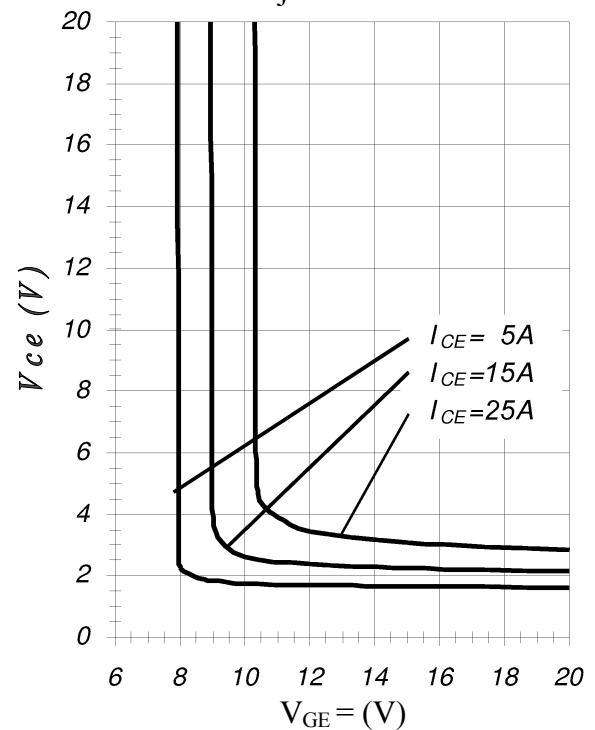


Fig. 11 – Typical V_{CE} vs. V_{GE}
 $T_j = 125^\circ\text{C}$

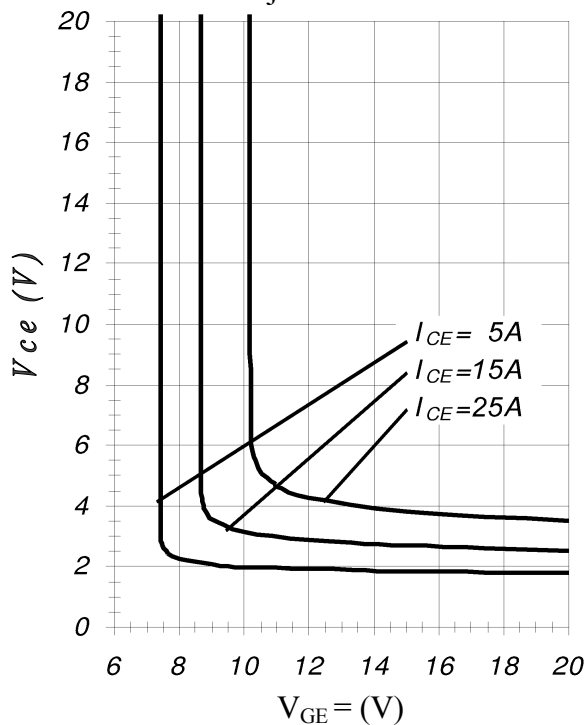


Fig. 12 – Typical Transfer Characteristics
 $V_{CE} = 20\text{V}$; $t_p = 20\mu\text{s}$

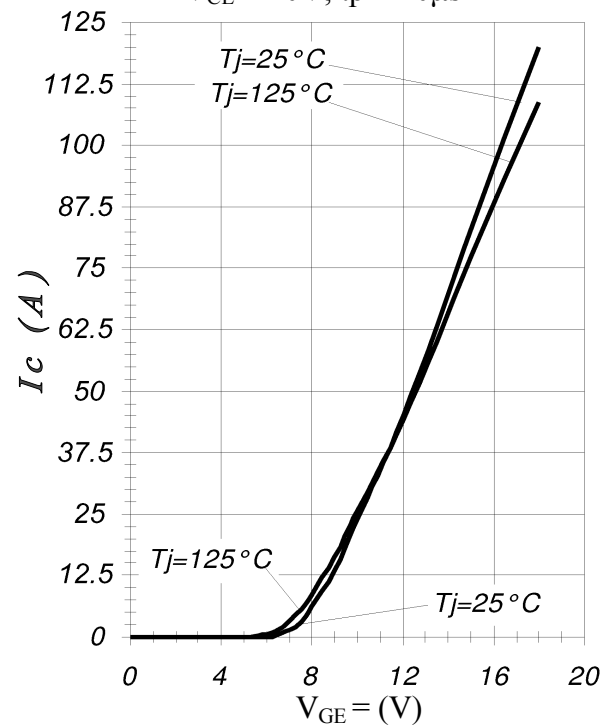


Fig. 13 – Typical Energy Loss vs. I_C
 $T_j = 125^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 600\text{V}$;
 $R_g = 10\Omega$; $V_{GE} = 15\text{V}$

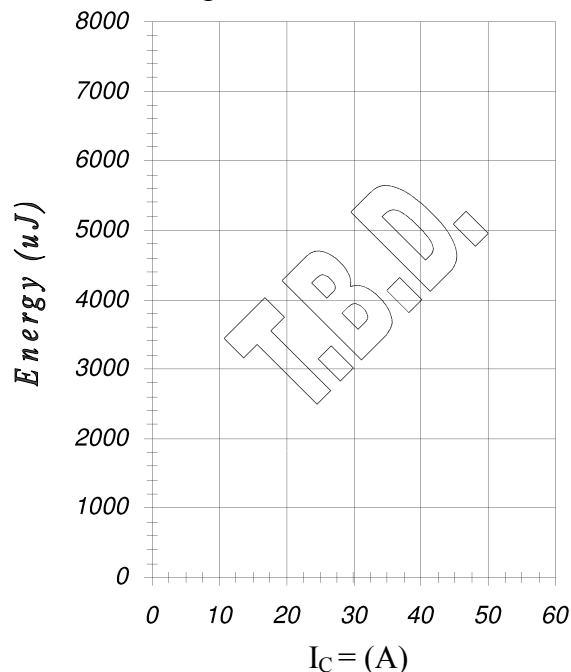


Fig. 14 – Typical Switching Time vs. I_C
 $T_j = 125^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 600\text{V}$;
 $R_g = 10\Omega$; $V_{GE} = 15\text{V}$

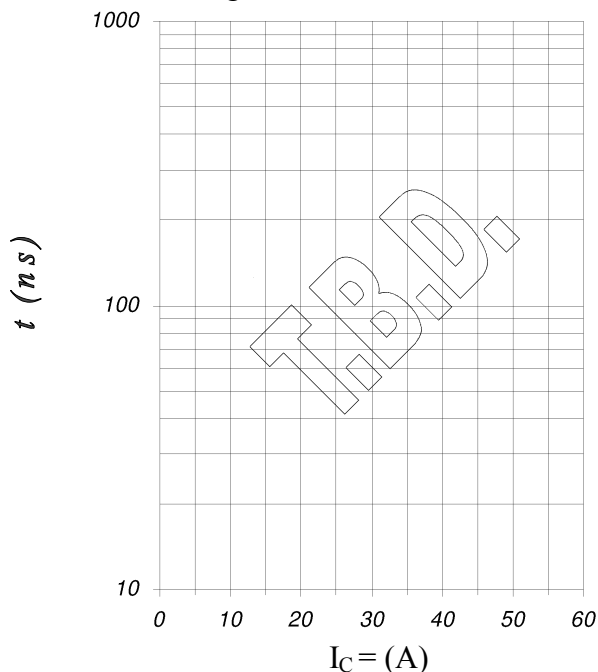


Fig. 15 – Typical Energy Loss vs. R_g
 $T_j = 125^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 600\text{V}$;
 $I_{CE} = 15\text{A}$; $V_{GE} = 15\text{V}$

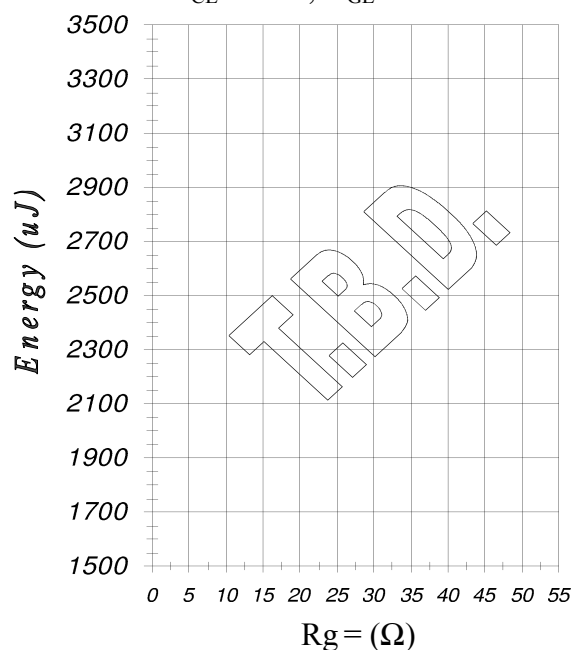


Fig. 16 – Typical Switching Time vs. R_g
 $T_j = 125^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 600\text{V}$;
 $I_{CE} = 15\text{A}$; $V_{GE} = 15\text{V}$

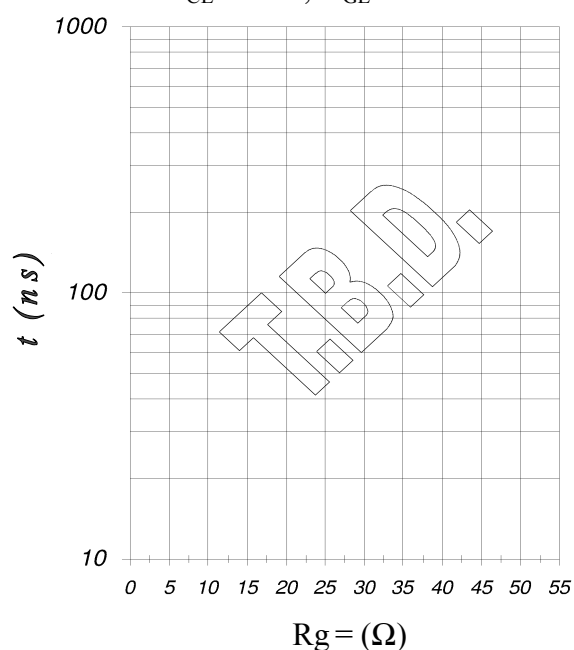


Fig. 17 – Typical Diode I_{RR} vs. I_F
 $T_j = 125^\circ\text{C}$

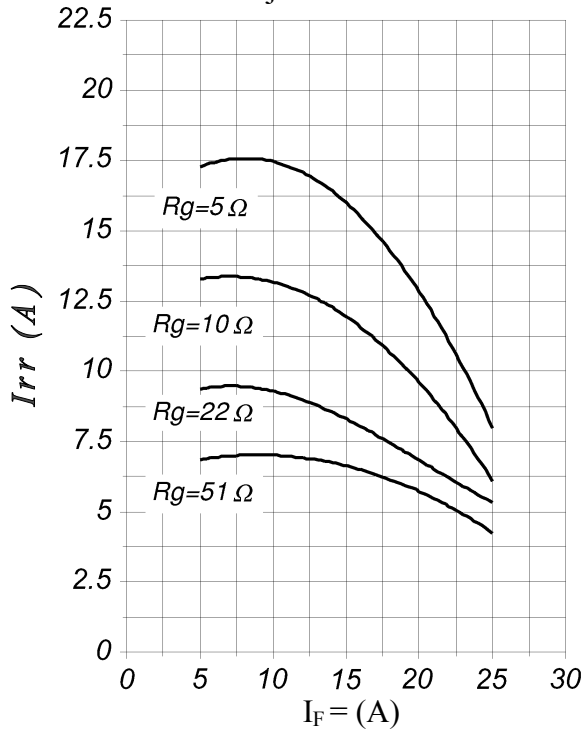


Fig. 18 – Typical Diode I_{RR} vs. R_g
 $I_F = 15\text{A}$; $T_j = 125^\circ\text{C}$

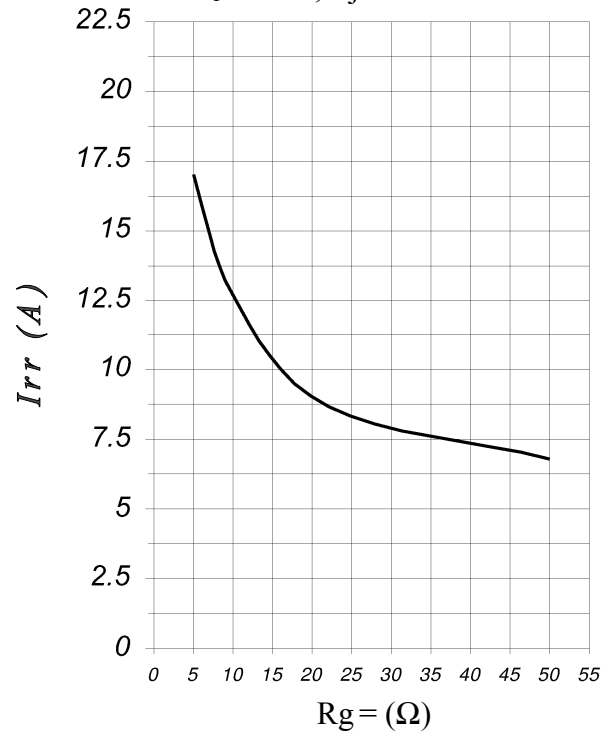


Fig. 19 – Typical Diode I_{RR} vs. dI_F/dt
 $V_{DC} = 600\text{V}$; $V_{GE} = 15\text{V}$; $I_F = 15\text{A}$; $T_j = 125^\circ\text{C}$

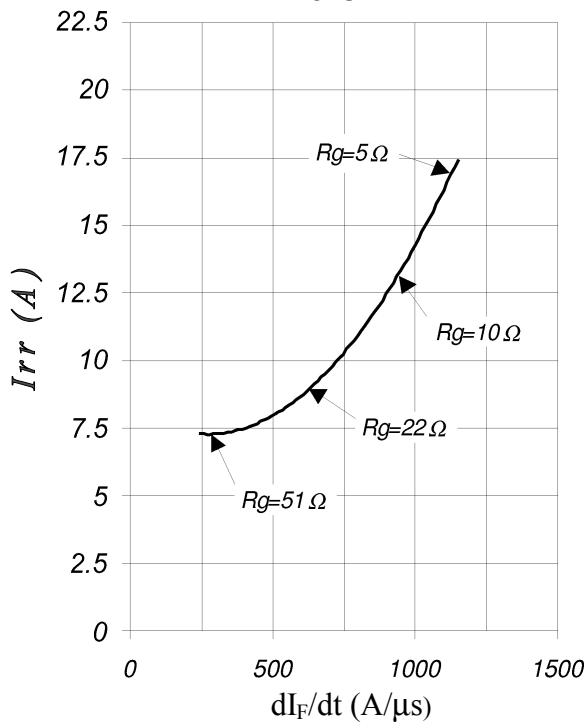


Fig. 20 – Typical Diode Q_{RR}
 $V_{DC} = 600\text{V}$; $V_{GE} = 15\text{V}$; $T_j = 125^\circ\text{C}$

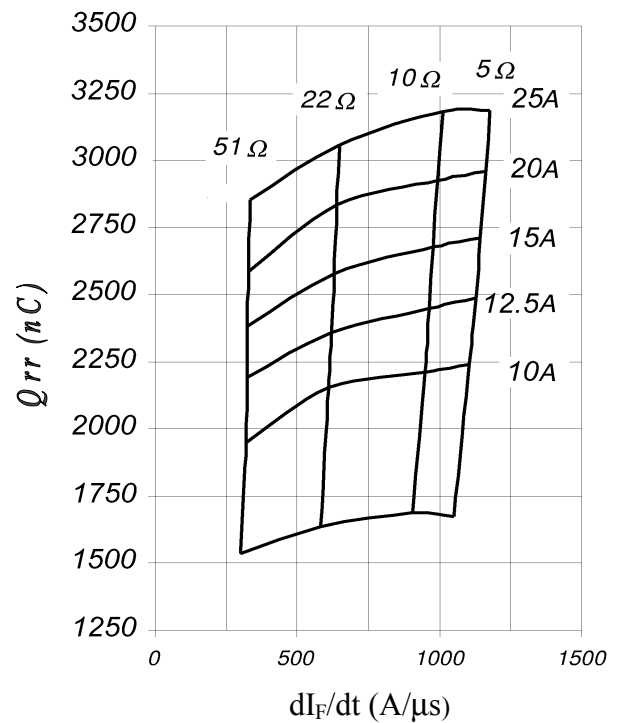


Fig. 21 – Typical Diode E_{REC} vs. I_F
 $T_J = 125^\circ\text{C}$

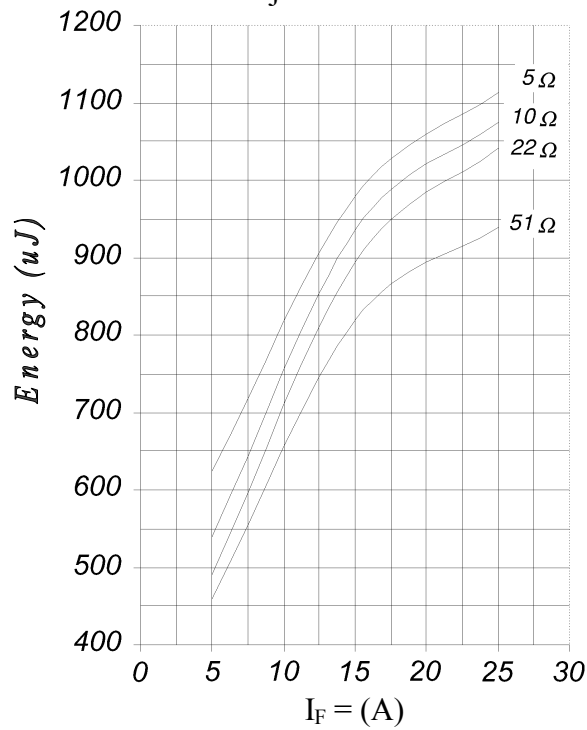


Fig. 22 – Typical Capacitance vs. V_{CE}
 $V_{GE} = 0\text{V}$; $f = 1\text{MHz}$

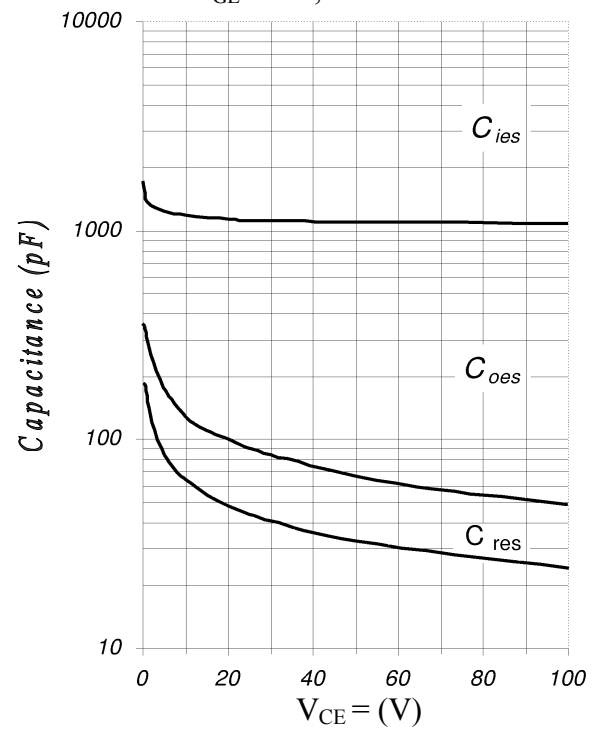


Fig. 23 – Typical Gate Charge vs. V_{GE}
 $I_C = 15\text{A}$; $L = 600\mu\text{H}$; $V_{CC} = 600\text{V}$

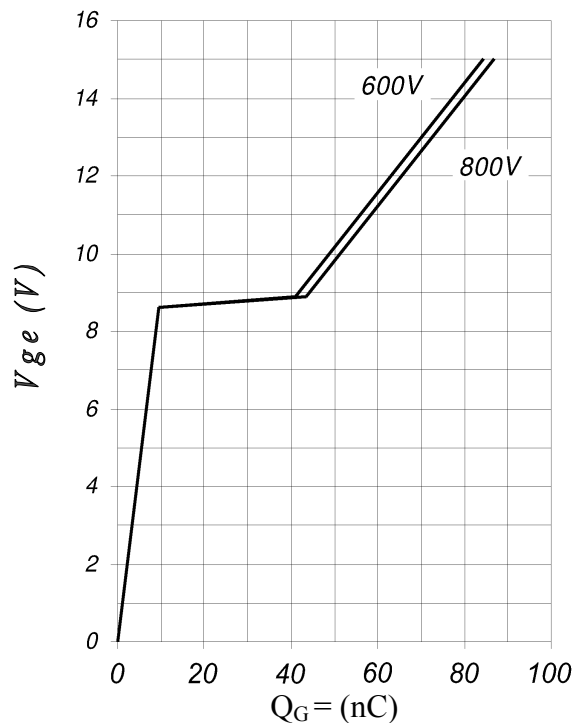


Fig. 24 – On state Voltage Drop characteristic V_{FM} vs I_F

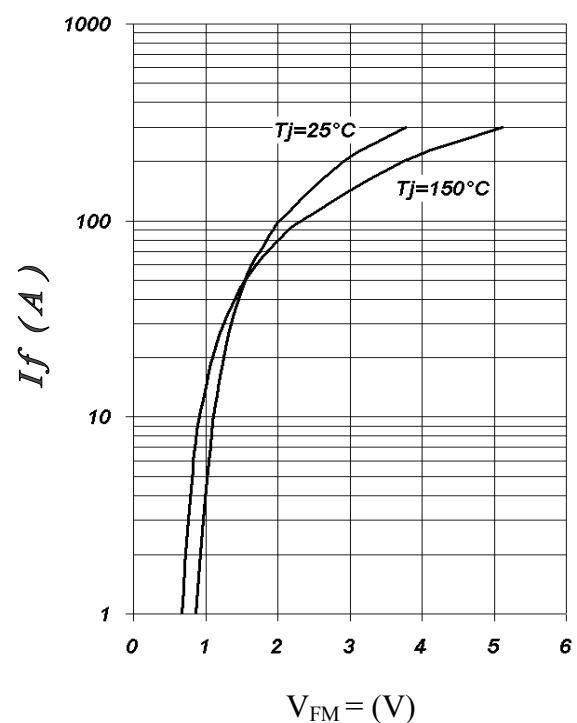


Fig. 25 – Normalized Transient Thermal Impedance, Junction-to-copper plate (IGBTs)

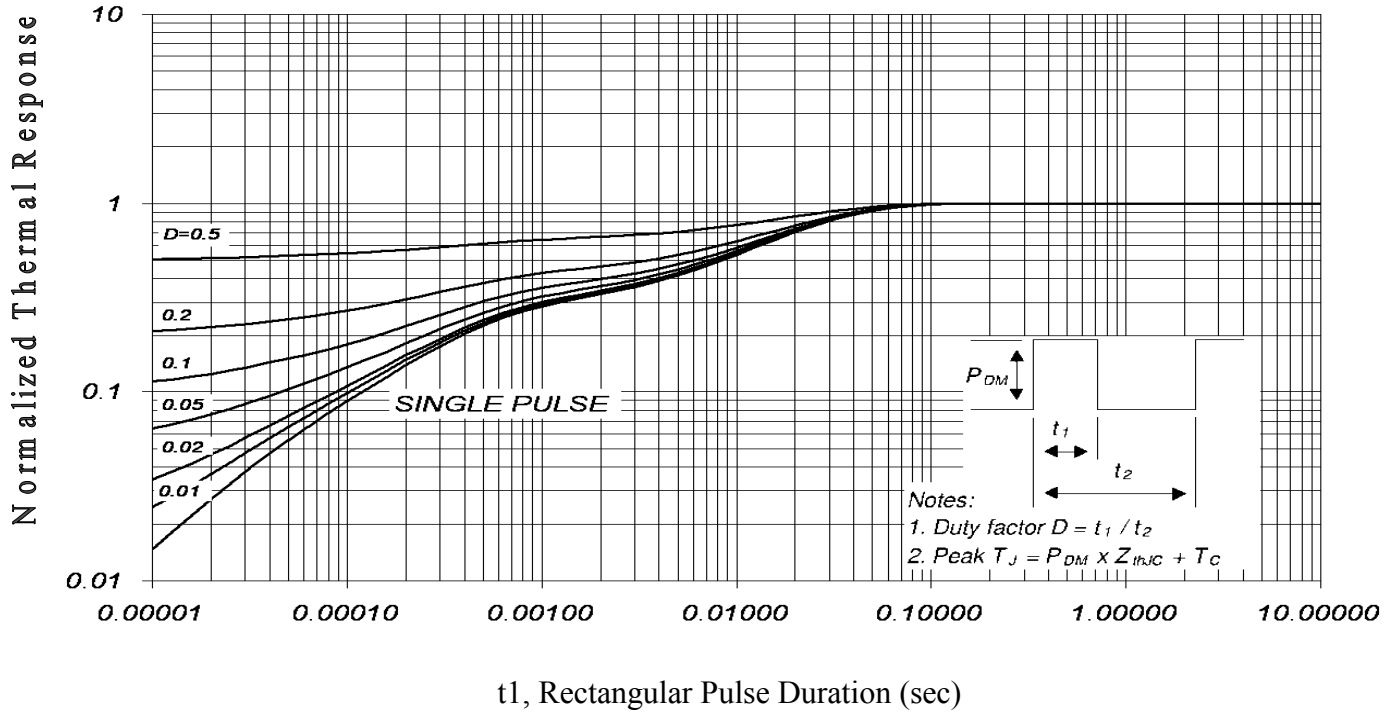


Fig. 26 – Normalized Transient Impedance, Junction-to-copper plate (FRED diodes)

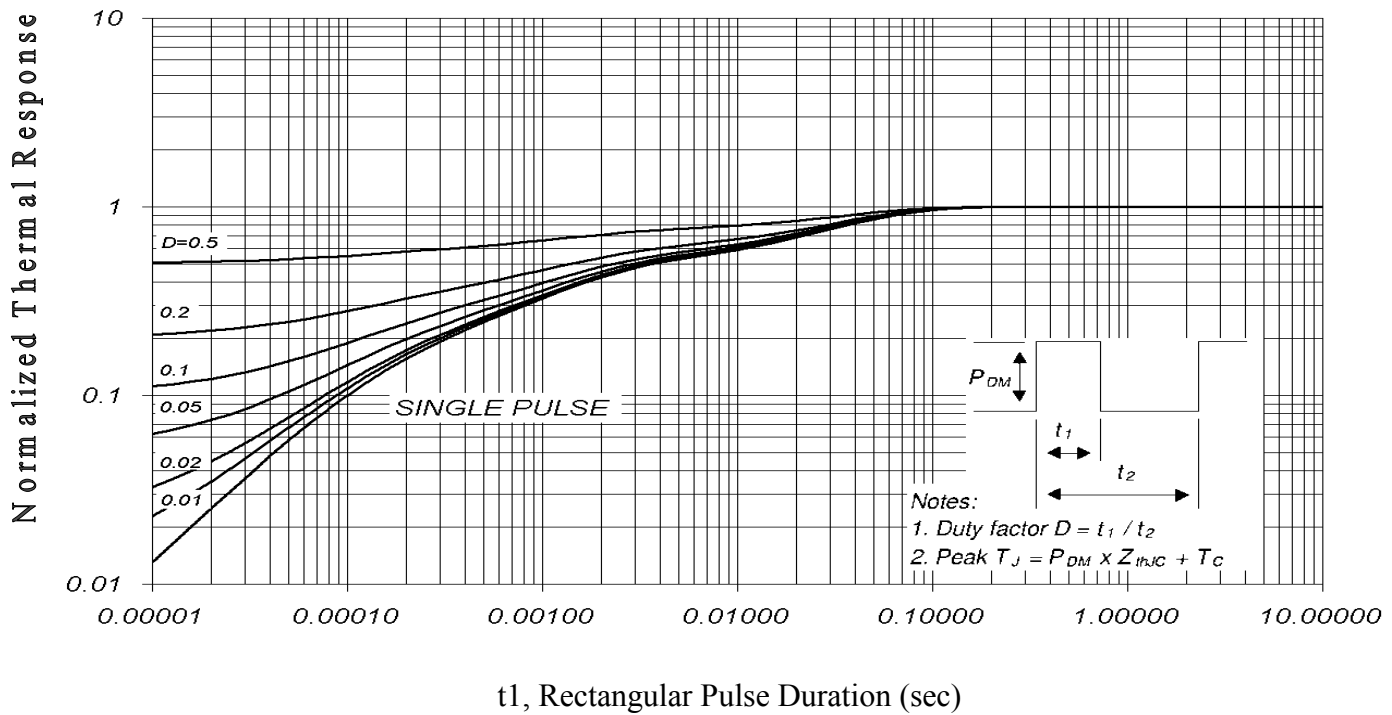


Fig. CT.1 - Gate Charge Circuit (turn-off)

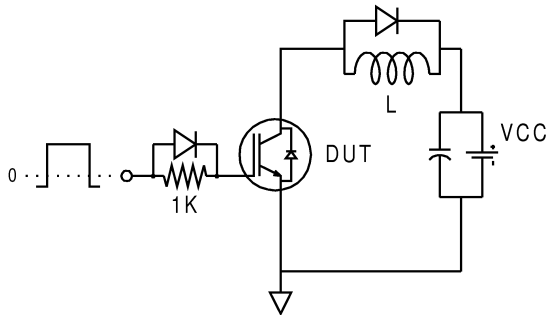


Fig. CT.2 - RBSOA Circuit

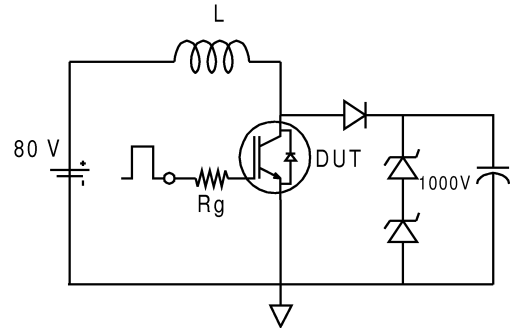


Fig. CT.3 - S.C. SOA Circuit

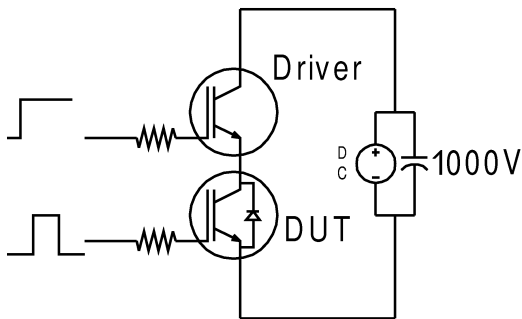


Fig. CT.4 - Switching Loss Circuit

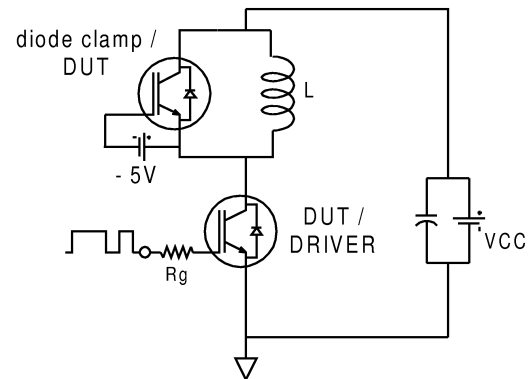


Fig. CT.5 - Resistive Load Circuit

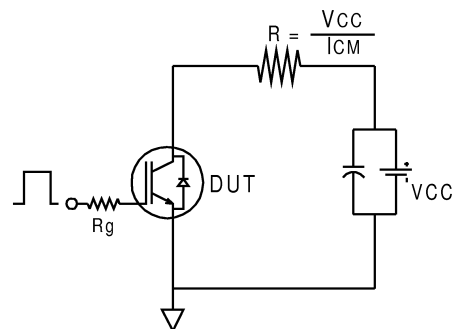


Fig. PD1 – Total Dissipated Power vs. f_{sw}
 $I_{outRMS} = 1.5A$, $V_{DC} = 530V$, $T_C = 55^\circ C$

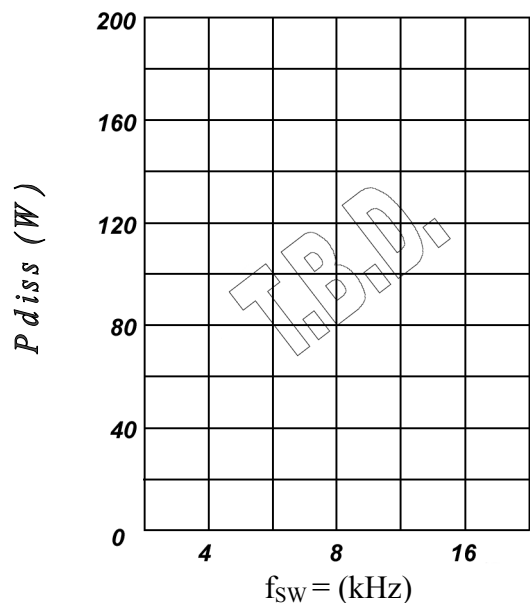


Fig. PD2 – Total Dissipated Power vs. f_{sw}
 $I_{outRMS} = 3A$, $V_{DC} = 530V$, $T_C = 55^\circ C$

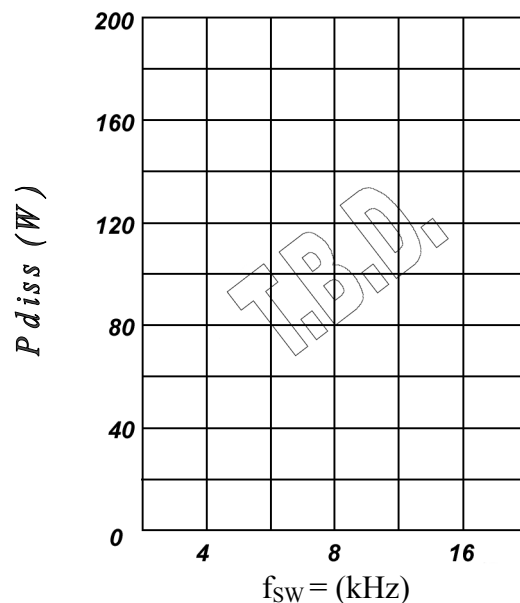


Fig. PD3 – Total Dissipated Power vs. f_{sw}
 $I_{outRMS} = 7A$, $V_{DC} = 530V$, $T_C = 40^\circ C$

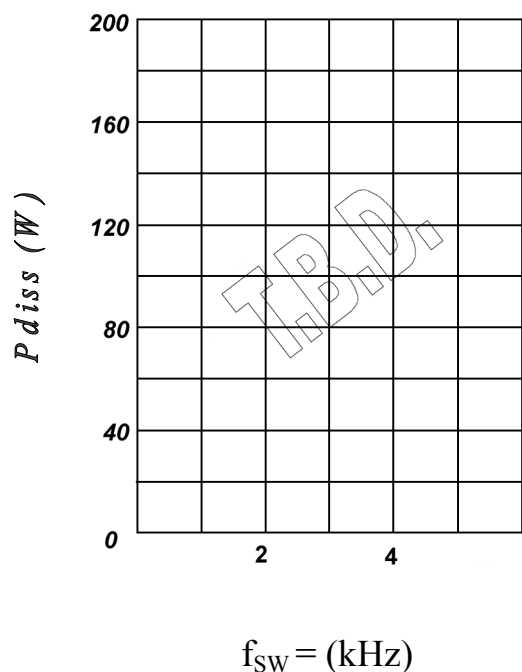
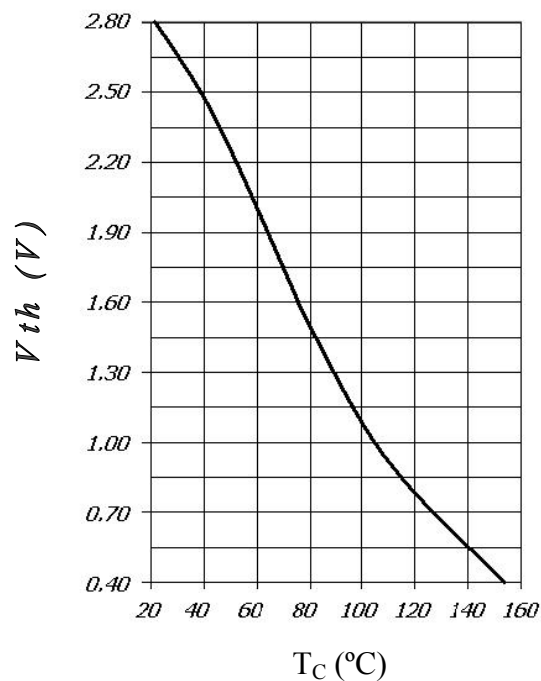
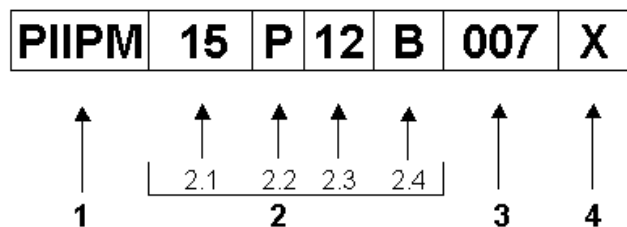


Fig. TF1 – Thermal Sensor Voltage Feedback vs. Base-plate Temperature



PIIPM family part number identification



1- Device type (**P**rogrammable **I**solated **I**ntelligent **P**ower **M**odule)

2- Power package code

2.1- Current rating Code [A]

2.2- Sensing Resistors configuration

P = on 3 phases

Q = on 2 phases (*)

R = on 1 phase (only for Matrix config.) (*)

E = on 3 emitters

F = on 2 emitters (*)

G = on 1 emitter (*)

2.3- Voltage rating Code [V/100]

06 = 600V

12 = 1200V

2.4- Power Module configuration code

A = Bridge brake (*)

B = Inverter

C = Inverter + brake

D = BBI (Bridge Brake Inverter)

M = Matrix (*)

3- EDB configuration code

See detailed Block Diagram

4- Status code

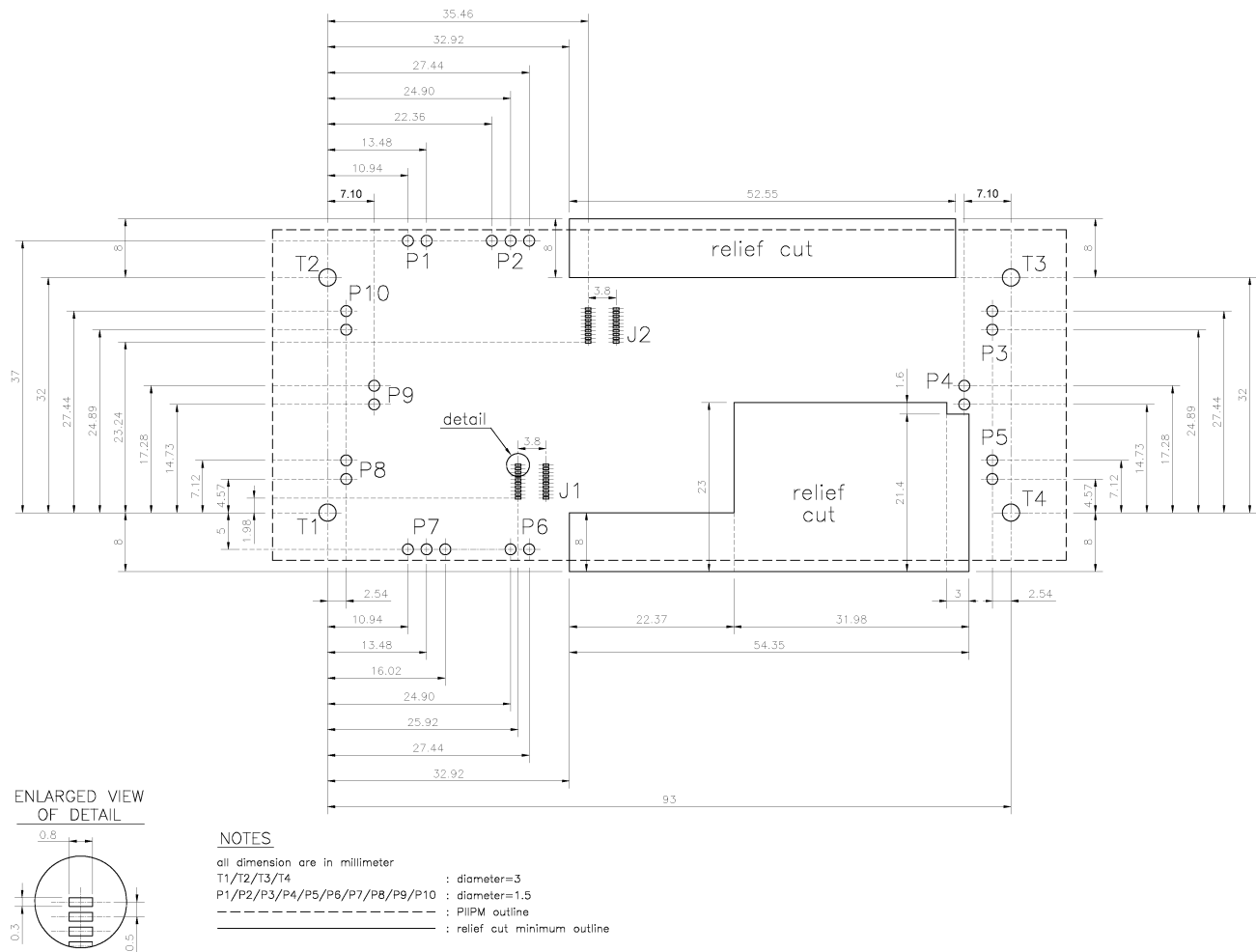
X = Sample (product with pre-qualification approval)

blank = Fully qualified product

note: * = contact factory for availability

Top board suggested footprint

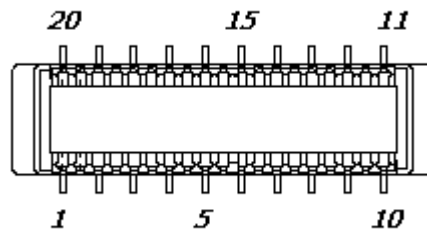
(top view)



RS485 and JTAG Connectors

Top view

These connectors do not have any orientation tag; please check their Pin 1 position on Power Module Frame Pins Mapping before inserting mate part.



Molex 53916-0204
mates with 54167-0208 or 52991-0208

[illegible]

International
IOR Rectifier

24