

DATA SHEET

PCF8524

**512 × 8-bit CMOS EEPROM
with I²C-bus interface**

Preliminary specification
File under Integrated Circuits, IC12

1996 Jan 22

**512 × 8-bit CMOS EEPROM
with I²C-bus interface****PCF8524**

| | | |
|---|------|---|
| CONTENTS | 12 | SOLDERING |
| 1 FEATURES | 12.1 | Introduction |
| 2 APPLICATIONS | 12.2 | Soldering by dipping or by wave |
| 3 GENERAL DESCRIPTION | 12.3 | Repairing soldered joints |
| 4 ORDERING INFORMATION | 13 | DEFINITIONS |
| 5 BLOCK DIAGRAM | 14 | LIFE SUPPORT APPLICATIONS |
| 6 PINNING | 15 | PURCHASE OF PHILIPS I ² C COMPONENTS |
| 7 FUNCTIONAL DESCRIPTION | | |
| 7.1 Pinning information | | |
| 7.1.1 Serial clock (SCL) | | |
| 7.1.2 Serial data (SDA) | | |
| 7.1.3 Address pins (A1 and A2) | | |
| 7.1.4 Write control (WC) | | |
| 7.2 Endurance and data retention | | |
| 7.3 Characteristics of the I ² C-bus | | |
| 7.3.1 General description | | |
| 7.3.2 Input data protocol | | |
| 7.3.3 START and STOP conditions. | | |
| 7.4 Device operation | | |
| 7.4.1 Acknowledge (ACK) | | |
| 7.4.2 Slave address byte | | |
| 7.4.3 Bank Select bit | | |
| 7.4.4 Read/write bit | | |
| 7.5 Write operations | | |
| 7.5.1 Byte write | | |
| 7.5.2 Page write | | |
| 7.5.3 Acknowledge polling | | |
| 7.6 Read operations | | |
| 7.6.1 Current address byte read | | |
| 7.6.2 Random address byte read | | |
| 7.6.3 Sequential read | | |
| 8 LIMITING VALUES | | |
| 9 DC CHARACTERISTICS | | |
| 10 AC CHARACTERISTICS | | |
| 11 PACKAGE OUTLINE | | |



512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

1 FEATURES

- Low power CMOS:
 - operating current: <2 mA
 - standby current: <2 µA
- Hardware write protection:
 - Write Control (WC) pin
- Operation supply voltage 2.7 to 5.5 V
- Extended temperature range –40 to +85 °C
- Internally organized as two banks (each 256 × 8-bit)
- I²C interface (bidirectional data transfer protocol)
- Sixteen-byte page-write mode (minimizes total write time per byte)
- Automatic word address incrementing (sequential register read)
- Self-timed write cycle
- High reliability:
 - endurance: 100 000 cycles
 - data retention: 10 years
- DIP8 or SO8 package (8 pins).

2 APPLICATIONS

The PCF8524 is ideal for applications requiring low voltage and low power consumption.

Typical applications include:

- Alarm devices
- Electronic locks
- Measuring devices
- Keys
- Pagers
- Cellular phones.

3 GENERAL DESCRIPTION

The PCF8524 is a cost effective 4096 bit (2 × 256 × 8-bit) serial Electrical Erasable Programmable Read Only Memory (EEPROM). The device is fabricated using advanced CMOS EEPROM technology. This IC operates from a single supply voltage within the range of 2.7 to 5.5 V.

The PCF8524 is internally organized as two 256 × 8-bit memory banks. It features an I²C-bus serial interface and software protocol allowing operation on a 2-wire bus.

Up to four PCF8524s may be connected to the 2-wire bus establishing their device addresses using the address input pins (A1 and A2).

4 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|---------|
| | NAME | DESCRIPTION | VERSION |
| PCF8524P | DIP8 | plastic dual in-line package; 8 leads (300 mil) | SOT97-1 |

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

5 BLOCK DIAGRAM

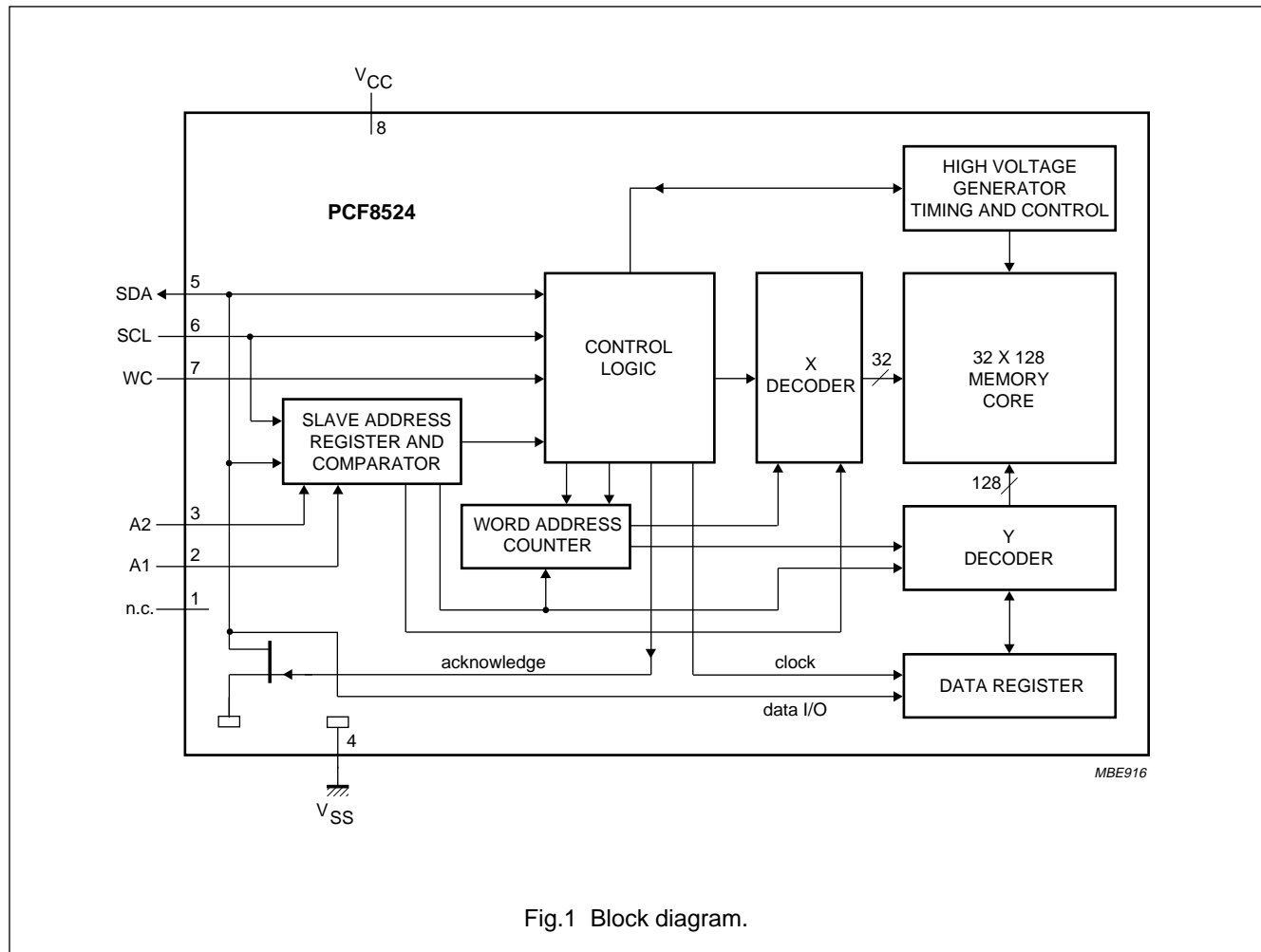


Fig.1 Block diagram.

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

6 PINNING

| SYMBOL | PIN | DESCRIPTION |
|-----------------|-----|--------------------------------|
| n.c. | 1 | not connected |
| A1 | 2 | address 1 input |
| A2 | 3 | address 2 input |
| V _{SS} | 4 | ground |
| SDA | 5 | serial data input/output (I/O) |
| SCL | 6 | serial clock input |
| WC | 7 | write control input |
| V _{CC} | 8 | supply voltage |

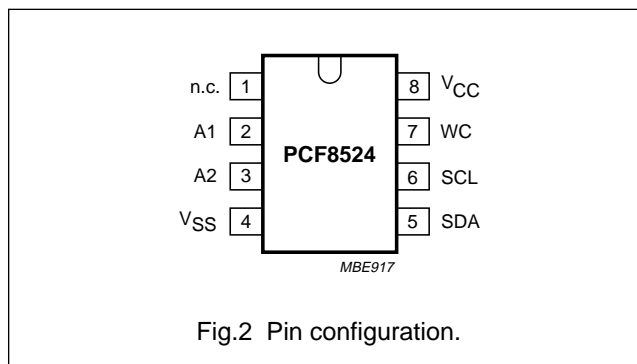


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Pinning information

7.1.1 SERIAL CLOCK (SCL)

The SCL input is used to clock data into and out of the device. In the write mode, data must remain stable when SCL is HIGH. In the read mode, data is clocked out on the falling edge of SCL.

7.1.2 SERIAL DATA (SDA)

The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may only change when SCL is LOW, except START and STOP conditions. It is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs.

7.1.3 ADDRESS PINS (A1 AND A2)

The address inputs are used to set the 2-bit device address of the PCF8524 which will identify it on the I²C-bus. The address pins may be tied HIGH or LOW, or they may be actively driven. These inputs allow up to four PCF8524 devices to be distinguished on the I²C-bus.

7.1.4 WRITE CONTROL (WC)

The write control input pin is used to disable the write circuitry to the memory. If WC = HIGH the write function is disabled, to protect previously written data. If WC = LOW the write function is enabled.

7.2 Endurance and data retention

The PCF8524 is designed for applications requiring up to 100000 write cycles and unlimited number of read cycles. It provides 10 years of secure data retention, with or without supply voltage applied, after the execution of 100000 write cycles.

7.3 Characteristics of the I²C-bus

7.3.1 GENERAL DESCRIPTION

The I²C-bus is designed for two-way, 2-line serial communication for different integrated circuits. The 2-lines are:

1. Serial Data line (SDA).
2. Serial Clock Line (SCL).

The SDA line must be connected to the positive supply voltage by a pull-up resistor, located somewhere on the I²C-bus (see Fig.3). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (I²C-bus is not busy).

7.3.2 INPUT DATA PROTOCOL

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while the clock is HIGH, because changes on the data line, while SCL is HIGH will be interpreted as a START or STOP condition (see Fig.4).

7.3.3 START AND STOP CONDITIONS.

When both data (SDA) and clock (SCL) lines are HIGH, the I²C-bus is referred to as 'not busy'. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (see Fig.5).

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

7.4 Device operation

The device supports the I²C-bus bidirectional data transmission protocol. The protocol defines any device that sends data onto the I²C-bus as a 'transmitter' and the receiving device as the 'receiver'. The device controlling the data transmission is the 'master' and the controlled device is the 'slave'. In all events the PCF8524 will be a 'slave' device because it never initiates any data transfers.

Up to four PCF8524s can be connected to the I²C-bus and can be selected by the A1 and A2 device addresses. A0 and A2 must be connected to either V_{CC}, V_{SS} or they may be actively driven. A0 and A2 define the address of the device. Other devices may be connected to the I²C-bus but each device needs its own device identification code.

7.4.1 ACKNOWLEDGE (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the I²C-bus after transmitting 8-bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it has received 8-bits of data (see Fig.6).

The PCF8524 will respond with an acknowledge after recognition of a START condition and its slave address byte. If both the device and a write operation have been selected, the PCF8524 will respond with an acknowledge after the receipt of each subsequent 8-bit word.

In the read mode, the PCF8524 transmits 8-bits of data, then releases the SDA line, and monitors the line for an acknowledge signal. If an acknowledge is detected, and no STOP condition is generated by the master, the PCF8524 will continue to transmit data. If an acknowledge is not detected, the PCF8524 terminates further data transmissions and awaits a STOP condition before returning to the standby power mode.

7.4.2 SLAVE ADDRESS BYTE

Following a START condition, the master must output the address to be accessed. The most significant 4 bits of the slave address are the 'device type identifier'. For a PCF8524 the address identifier is 1010 (see Table 1).

The next 2 bits are device address, addressing a particular device. Using this addressing scheme, a system may cascade up to four PCF8524 devices on the I²C-bus. The device address is defined by the state of the A1 and A2 input pins.

7.4.3 BANK SELECT BIT

The next bit of the serial stream is the Bank Select bit (BS). It is used by the host to toggle between the two 2 kbit banks of memory. It is, in effect, the most significant bit of the word address, or A8.

7.4.4 READ/WRITE BIT

The last bit of the slave address defines the operation to be performed. When $R/\overline{W} = 1$, a read operation is selected. If $R/\overline{W} = 0$, a write operation is selected (see Table 1).

Table 1 Slave address byte

| DEVICE TYPE IDENTIFIER | | | | DEVICE ADDRESS | | | R/ \overline{W} |
|------------------------|---|---|---|----------------|----|----|-------------------|
| 1 | 0 | 1 | 0 | A2 | A1 | BS | note 1 |

Note

- This is the read/write bit:
 - When $R/\overline{W} = 1$, a read operation is selected.
 - When $R/\overline{W} = 0$, a write operation is selected.

512 × 8-bit CMOS EEPROM
with I²C-bus interface

PCF8524

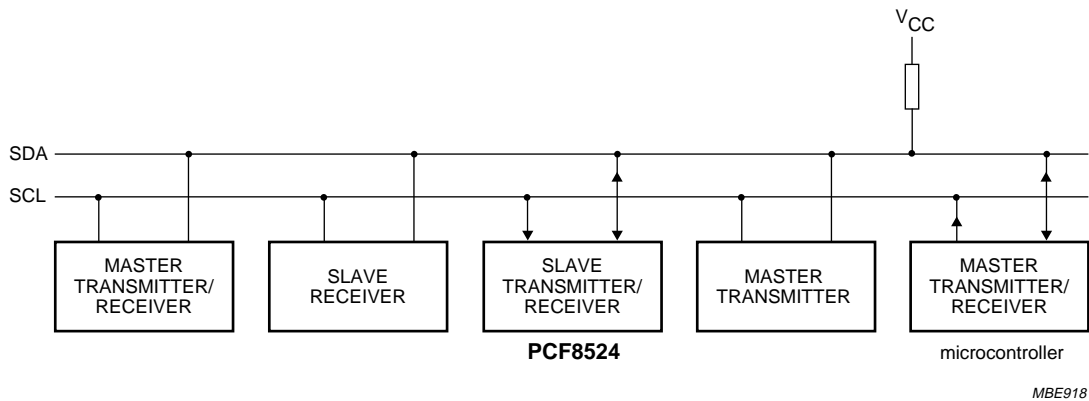


Fig.3 System configuration.

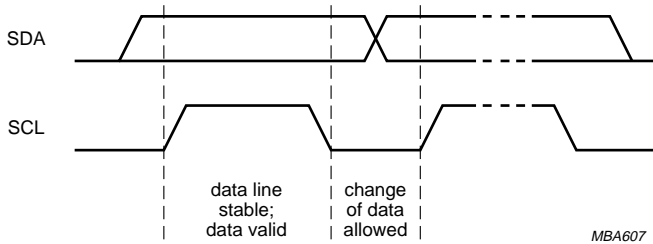


Fig.4 Input data protocol.

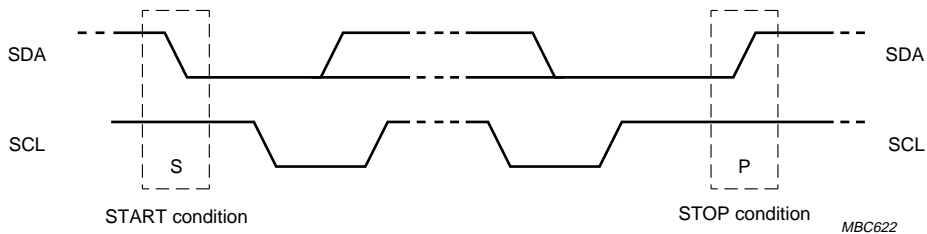


Fig.5 Definition of START and STOP conditions.

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

7.5 Write operations

The PCF8524 allows two types of write operations:

- Byte write operation; this operation writes a single byte during the nonvolatile write period (t_{WR}).
- Page write operation; this operation allows up to 16 bytes in the same page to be stored during t_{WR} .

7.5.1 BYTE WRITE

After the slave address is sent (to identify the slave device, select the bank and specify a read or write operation), a second byte is transmitted which contains the word address of any one of the 256 words in the bank selected by the slave address byte.

Upon receipt of the word address, the PCF8524 responds with an acknowledge, and waits for the next 8 bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a STOP condition, at which time the PCF8524 begins the internal write cycle.

While the internal write cycle is in progress, the PCF8524 inputs are disabled, and the device will not respond to any requests from the master. Figure 7 shows an overview of the address, acknowledge and data transfer sequence.

7.5.2 PAGE WRITE

The PCF8524 has the capability to perform a 16 bytes page write operation. It is initiated in the same way as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to 15 more words. After the receipt of each word, the PCF8524 will respond with an acknowledge.

The device automatically increments the address for subsequent data words. After the receipt of each word, the two low order address bits are internally incremented by one. The high order 5 bits of the address remain constant. If the master should transmit more than 16 words, prior to generating the STOP condition, the address counter will 'roll over', and the previously written data will be overwritten. In the same way as during a byte write operation, all inputs are disabled during the internal write cycle. Figure 7 shows an overview of the address, acknowledge and data transfer sequence.

7.5.3 ACKNOWLEDGE POLLING

When the PCF8524 is performing an internal write operation, it will not recognize a START condition. Since the device will only return an acknowledge after it accepts the START condition, the part can be continuously queried until an acknowledge is issued, indicating that the internal write cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a write operation (see Fig.8).

7.6 Read operations

Read operations are initiated with setting the R/\overline{W} bit of the slave address byte to logic 1. There are four different read operations:

1. Current address byte read.
2. Random address byte read.
3. Current address sequential read.
4. Random address sequential read.

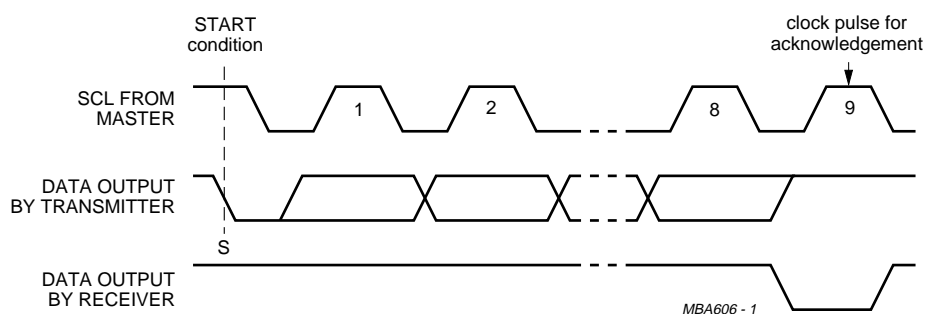
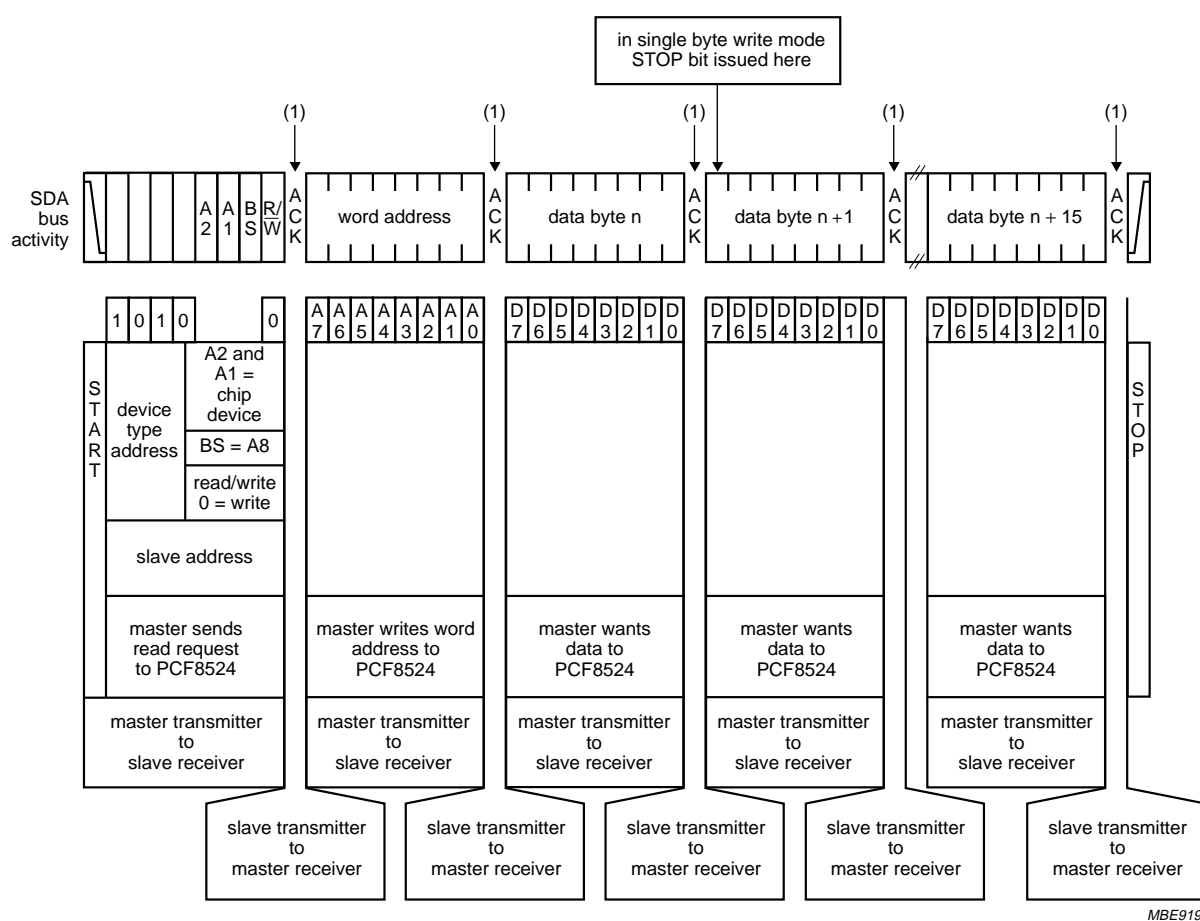
7.6.1 CURRENT ADDRESS BYTE READ

The PCF8524 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or a write operation) was to address location n , the next read operation would access data from address $n + 1$, and update the current address pointer. When the PCF8524 receives the slave address field with the R/\overline{W} bit set to logic 1, it issues an acknowledge signal and transmits the 8-bit word stored at address $n + 1$.

The current address read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a STOP condition. At this point, the PCF8524 discontinues the transmission (see Fig.9 for the address, acknowledge and data transfer sequence).

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

Fig.6 Acknowledge signal on the I²C-bus.

(1) Acknowledges transmitted from PCF8524 to master receiver.

Fig.7 Byte write and page write mode.

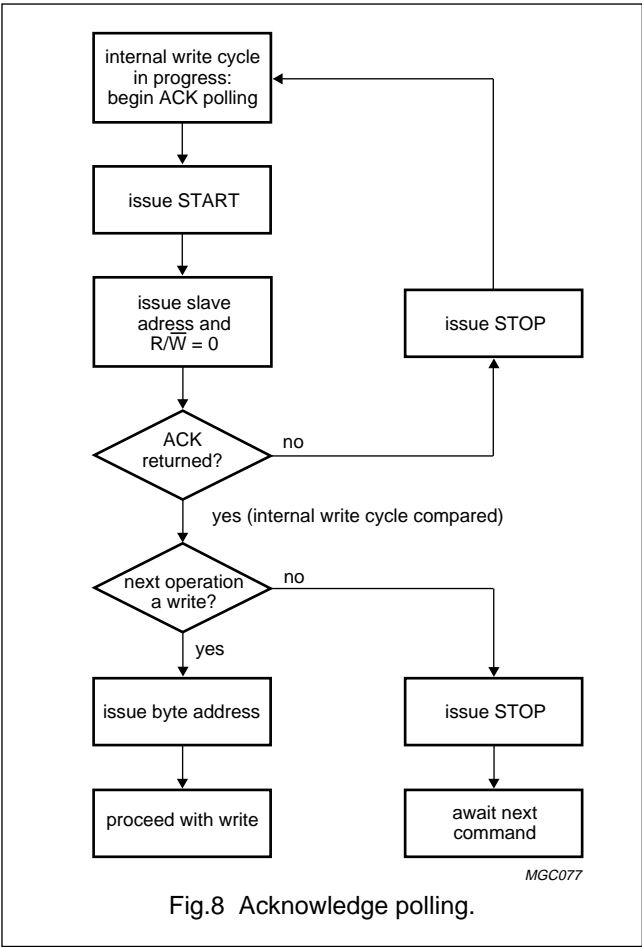
512 × 8-bit CMOS EEPROM
with I²C-bus interface

PCF8524

7.6.2 RANDOM ADDRESS BYTE READ

Random address read operations allow the master to access any memory location at random. This operation involves a two-step process. First the master issues a write command which includes the START condition and the slave address field (with the R/W bit set to write), followed by the address of the word it is to read. This procedure sets the internal address counter of the PCF8524 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a START condition followed by another slave address field with the R/W bit set to read. The PCF8524 will respond with an acknowledge and transmits the 8 data bits stored in the addressed location. At this point, the master does not acknowledge the transmission, but generates the STOP condition. The PCF8524 discontinues the data transmission and reverts to its standby power mode (see Fig.10 for the address, acknowledge and data transfer sequence).



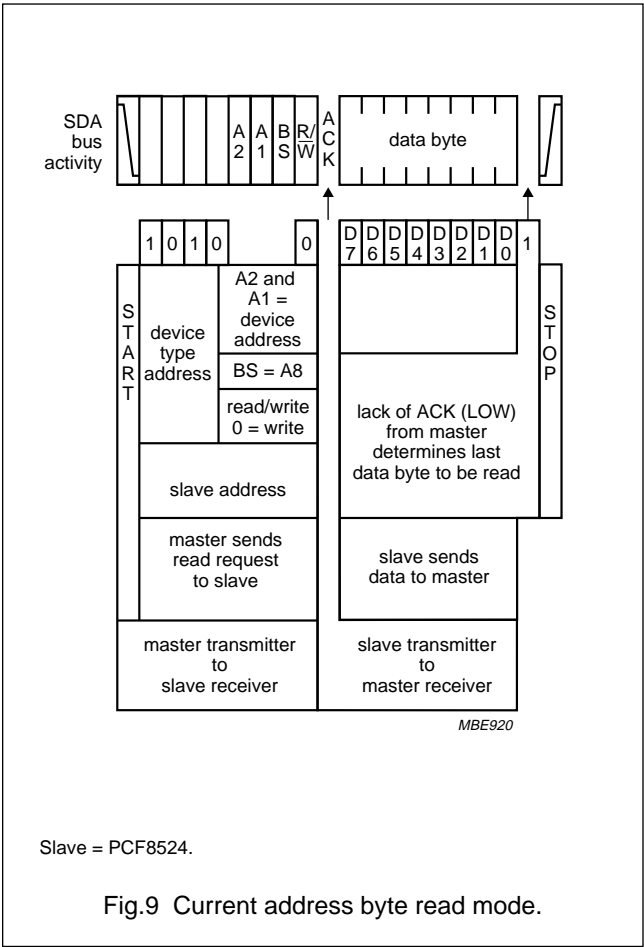
7.6.3 SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random address read. The first word is transmitted in the same way as during the other byte read modes (current address byte read or random address byte read), but in this event the master responds with an acknowledge signal, indicating that it requires additional data from the PCF8524.

The PCF8524 continues to output data for each received acknowledge signal. The master terminates the sequential read operation by not responding with an acknowledge signal, and issues a STOP condition.

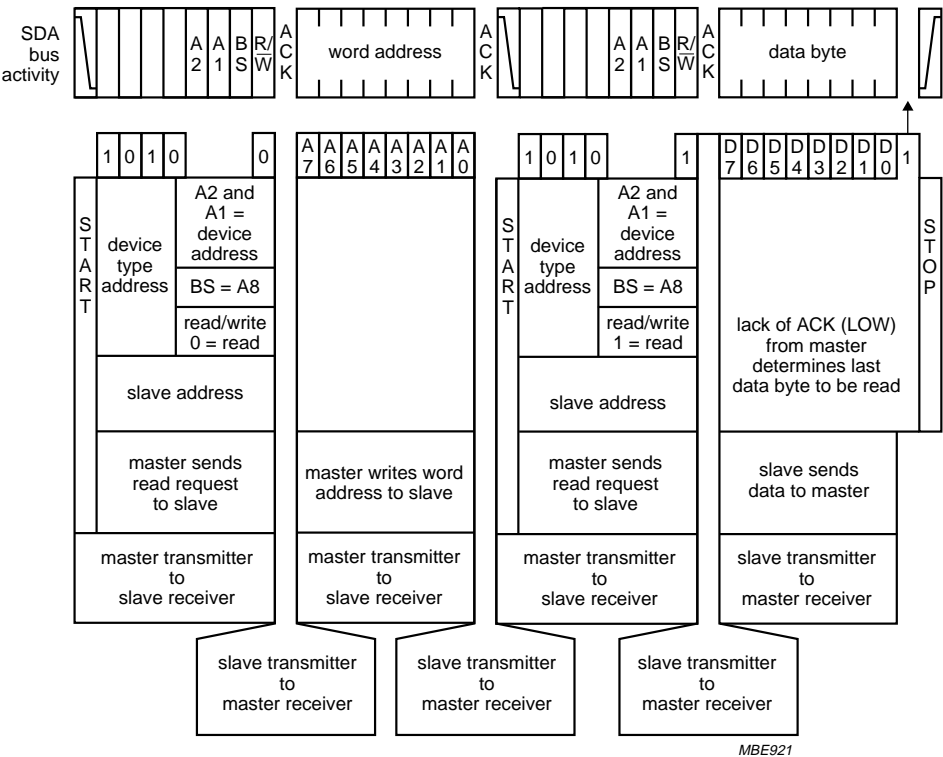
During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command.

When the counter reaches the top of the array, it will 'roll over' to the bottom of the array and continue to transmit data for each acknowledge bit it receives (see Fig.11).



512 × 8-bit CMOS EEPROM
with I²C-bus interface

PCF8524

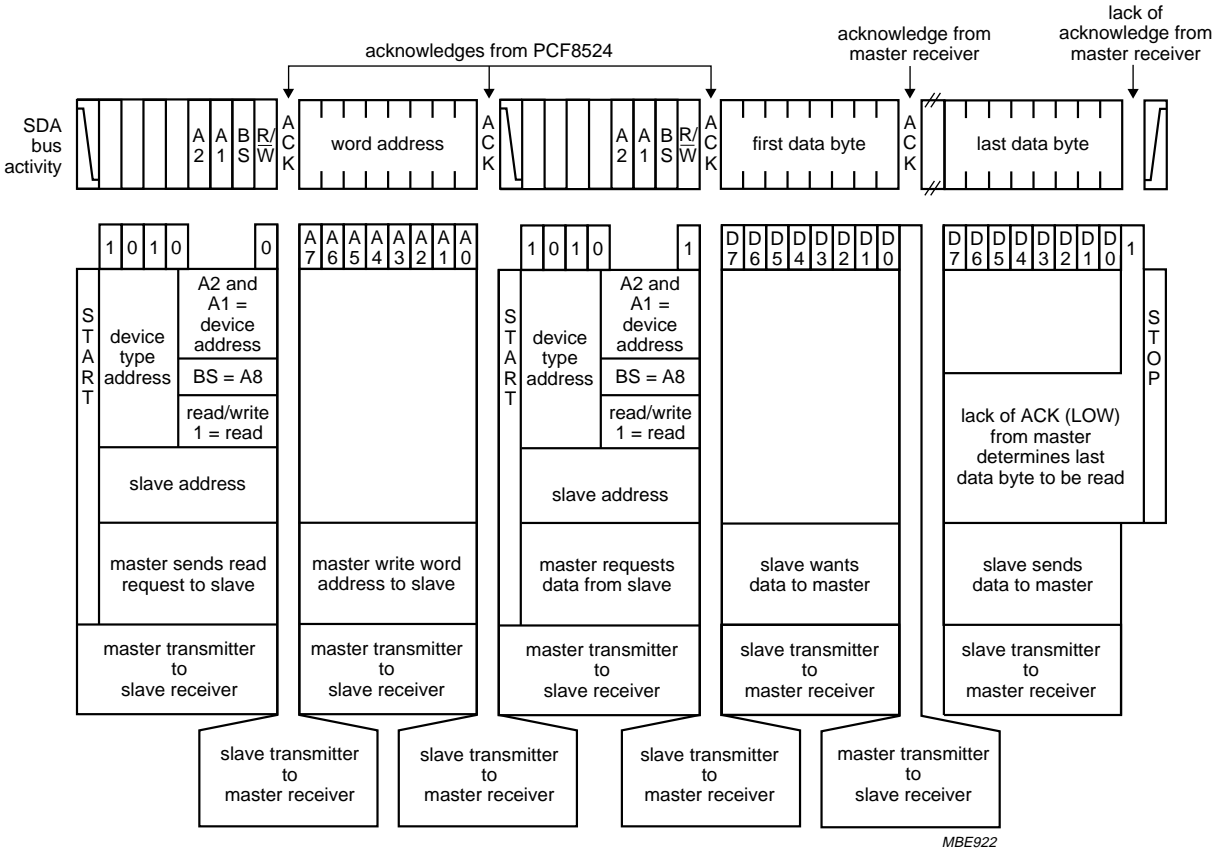


Slave = PCF8524.

Fig.10 Random address byte read mode.

512 × 8-bit CMOS EEPROM
with I²C-bus interface

PCF8524



MBE922

Slave = PCF8524.

Fig.11 Sequential read operation (starting with a random address read).

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|-------------------------------|--------------|-------|-----------------------|------|
| V _{CC} | supply voltage | | 0 | 6.5 | V |
| V _n | voltage on any pin | | −0.5 | V _{CC} + 0.5 | V |
| I _O | output current | | − | 5 | mA |
| T _{sol} | soldering temperature | <10 s | − | 300 | °C |
| T _{stg} | storage temperature | | −65 | +125 | °C |
| T _{amb} | operating ambient temperature | | −40 | +85 | °C |
| V _{es} | electrostatic handling | JEDEC method | −2000 | +2000 | V |

9 DC CHARACTERISTICS

V_{CC} = 2.7 to 5.5 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------|--|---|--------------------|--------------------|------|
| I _{CC} | supply current (CMOS) | V _{CC} = 5 V ±10%; note 1 | − | 2 | mA |
| | | V _{CC} = 3 V ±10%; note 1 | − | 1 | mA |
| I _{stb} | standby current (CMOS) | SCL = SDA = V _{CC} ; note 2 | − | 2 | μA |
| I _{LI} | input leakage current | V _I = 0 to V _{CC} | − | 10 | μA |
| I _{LO} | output leakage current | V _O = 0 to V _{CC} | − | 10 | μA |
| V _{IL} | LOW level input voltage pins A0 to A2, SCL and SDA | | − | 0.3V _{CC} | V |
| V _{IH} | HIGH level input voltage pins A0 to A2, SCL and SDA | | 0.7V _{CC} | − | V |
| V _{OL} | LOW level output voltage | I _{OL} = 3 mA | − | 0.4 | V |
| C _I | input capacitance | T _{amb} = 25 °C; f _{SCL} = 100 kHz | − | 5 | pF |
| C _O | output capacitance | T _{amb} = 25 °C; f _{SCL} = 100 kHz | − | 8 | pF |

Notes

- f_{SCL} = 100 kHz; SDA = open-circuit; all other inputs connected to ground (V_{SS}) or V_{CC}.
- All other inputs connected to ground (V_{SS}) or V_{CC}.

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

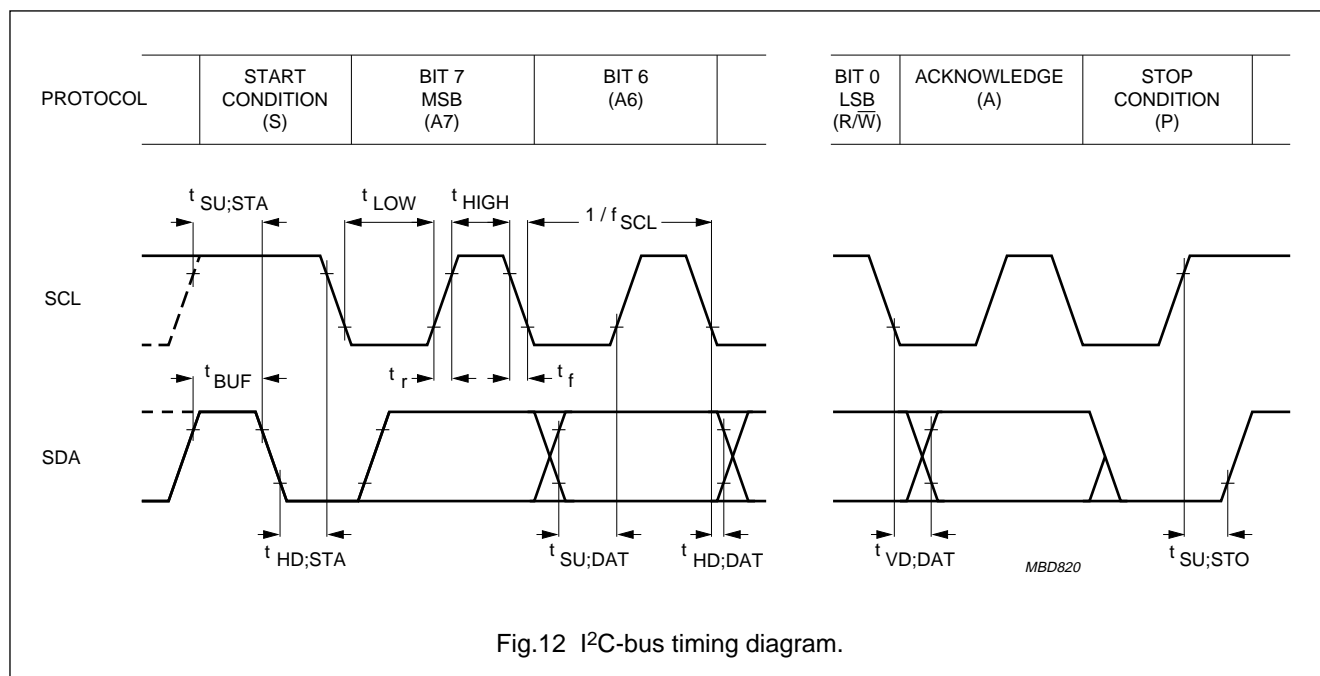
10 AC CHARACTERISTICS

$V_{CC} = 2.7$ to 5.5 V; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified (see Fig.12); note 1.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|--------------|-------------------------------|-----------------------------------|------|------|---------|
| f_{SCL} | SCL clock frequency | | 0 | 100 | kHz |
| t_{LOW} | SCL LOW time | | 4.7 | – | μ s |
| t_{HIGH} | SCL HIGH time | | 4.0 | – | μ s |
| t_{BUF} | bus free time | before new transmission | 4.7 | – | μ s |
| $t_{SU;STA}$ | START condition set-up time | | 4.7 | – | μ s |
| $t_{HD;STA}$ | START condition hold time | | 4.0 | – | μ s |
| $t_{SU;STO}$ | STOP condition set-up time | | 4.7 | – | μ s |
| $t_{VD;DAT}$ | SCL LOW-to-SDA data out valid | | 0.3 | 3.5 | μ s |
| $t_{HD;DAT}$ | data hold time | SCL LOW to SDA output data change | 0.3 | – | μ s |
| t_r | SCL and SDA rise time | | – | 1000 | ns |
| t_f | SCL and SDA fall time | | – | 300 | ns |
| $t_{SU;DAT}$ | input data set-up time | | 250 | – | ns |
| $t_{HD;DAT}$ | data hold time | | 0 | – | ns |
| t_{SP} | noise spike width | | – | 100 | ns |
| $T_{cy(w)}$ | write cycle time | $V_{CC} = 5\text{ V} \pm 10\%$ | – | 10 | ms |
| | | $V_{CC} = 3\text{ V} \pm 10\%$ | – | 25 | ms |

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure “The I²C-bus and how to use it”. This brochure may be ordered using the code 9398 393 40011.



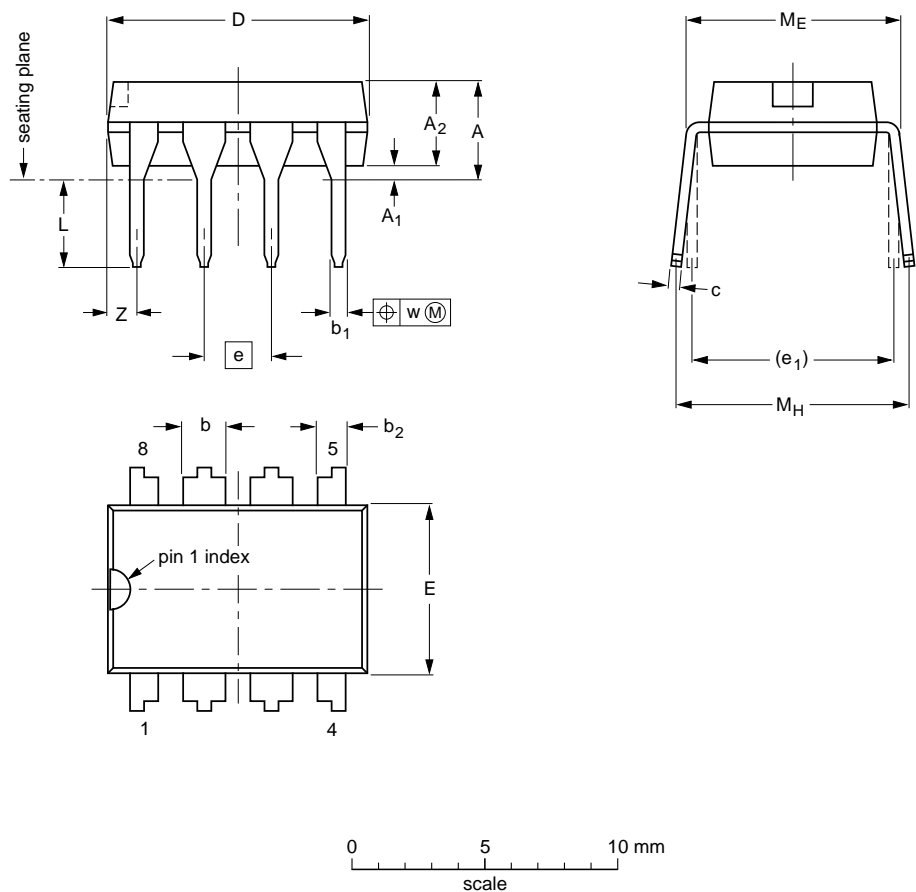
512 × 8-bit CMOS EEPROM
with I²C-bus interface

PCF8524

11 PACKAGE OUTLINE

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1

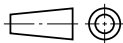


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | b ₂ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|-----------|------------------------|------------------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|--------------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.14 | 0.53 0.38 | 1.07 0.89 | 0.36 0.23 | 9.8 9.2 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 1.15 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.045 | 0.021 0.015 | 0.042 0.035 | 0.014 0.009 | 0.39 0.36 | 0.26 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.045 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|----------|------|--|---|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT97-1 | 050G01 | MO-001AN | | |  | 92-11-17 95-02-04 |

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

12 SOLDERING

12.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

12.2 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{\text{stg max}}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

12.3 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

512 × 8-bit CMOS EEPROM with I²C-bus interface

PCF8524

13 DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

14 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

15 PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

512 × 8-bit CMOS EEPROM
with I²C-bus interface

PCF8524

NOTES

512 × 8-bit CMOS EEPROM
with I²C-bus interface

PCF8524

NOTES

Philips Semiconductors – a worldwide company

Argentina: IEROD, Av. Juramento 1992 - 14.b, (1428)
BUENOS AIRES, Tel. (541)786 7633, Fax. (541)786 9367

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. (02)805 4455, Fax. (02)805 4466

Austria: Triester Str. 64, A-1101 WIEN, P.O. Box 213,
Tel. (01)60 101-1236, Fax. (01)60 101-1211

Belgium: Postbus 90050, 5600 PB EINDHOVEN, The Netherlands,
Tel. (31)40-2783749, Fax. (31)40-2788399

Brazil: Rua do Rocio 220 - 5th floor, Suite 51,
CEP: 04552-903-SÃO PAULO-SP, Brazil,
P.O. Box 7383 (01064-970),
Tel. (011)821-2333, Fax. (011)829-1849

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS:
Tel. (800) 234-7381, Fax. (708) 296-8556

Chile: Av. Santa Maria 0760, SANTIAGO,
Tel. (02)773 816, Fax. (02)777 6730

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. (852)2319 7888, Fax. (852)2319 7700

Colombia: IPRELENTO LTDA, Carrera 21 No. 56-17,
77621 BOGOTÁ, Tel. (571)249 7624/(571)217 4609,
Fax. (571)217 4549

Denmark: Prags Boulevard 80, PB 1919, DK-2300
COPENHAGEN S, Tel. (45)32 88 26 36, Fax. (45)31 57 19 49

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. (358)0-615 800, Fax. (358)0-61580 920

France: 4 Rue du Port-aux-Vins, BP317,
92156 SURESNES Cedex,
Tel. (01)4099 6161, Fax. (01)4099 6427

Germany: P.O. Box 10 51 40, 20035 HAMBURG,
Tel. (040)23 53 60, Fax. (040)23 53 63 00

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. (01)4894 339/4894 911, Fax. (01)4814 240

India: Philips INDIA Ltd, Shivsagar Estate, A Block,
Dr. Annie Besant Rd. Worli, Bombay 400 018
Tel. (022)4938 541, Fax. (022)4938 722

Indonesia: Philips House, Jalan H.R. Rasuna Said Kav. 3-4,
P.O. Box 4252, JAKARTA 12950,
Tel. (021)5201 122, Fax. (021)5205 189

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. (01)7640 000, Fax. (01)7640 200

Italy: PHILIPS SEMICONDUCTORS S.r.l.,
Piazza IV Novembre 3, 20124 MILANO,
Tel. (0039)2 6752 2531, Fax. (0039)2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. (03)3740 5130, Fax. (03)3740 5077

Korea: Philips House, 260-199 Itaewon-dong,
Yongsan-ku, SEOUL, Tel. (02)709-1412, Fax. (02)709-1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA,
SELANGOR, Tel. (03)750 5214, Fax. (03)757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TX 79905,
Tel. 9-5(800)234-7381, Fax. (708)296-8556

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. (040)2783749, Fax. (040)2788399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. (09)849-4160, Fax. (09)849-7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. (022)74 8000, Fax. (022)74 8341

Pakistan: Philips Electrical Industries of Pakistan Ltd.,
Exchange Bldg. ST-2/A, Block 9, KDA Scheme 5, Clifton,
KARACHI 75600, Tel. (021)587 4641-49,
Fax. (021)577035/5874546

Philippines: PHILIPS SEMICONDUCTORS PHILIPPINES Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. (63) 2 816 6380, Fax. (63) 2 817 3474

Portugal: PHILIPS PORTUGUESA, S.A.,
Rua dr. António Loureiro Borges 5, Arquiparque - Miraflores,
Apartado 300, 2795 LINDA-A-VELHA,
Tel. (01)4163160/4163333, Fax. (01)4163174/4163366

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. (65)350 2000, Fax. (65)251 6500

South Africa: S.A. PHILIPS Pty Ltd.,
195-215 Main Road Martindale, 2092 JOHANNESBURG,
P.O. Box 7430, Johannesburg 2000,
Tel. (011)470-5911, Fax. (011)470-5494

Spain: Balmes 22, 08007 BARCELONA,
Tel. (03)301 6312, Fax. (03)301 42 43

Sweden: Kottbygatan 7, Akalla. S-164 85 STOCKHOLM,
Tel. (08)632 2000, Fax. (08)632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. (01)488 2211, Fax. (01)481 77 30

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66, Chung Hsiao West
Road, Sec. 1. Taipei, Taiwan ROC, P.O. Box 22978,
TAIPEI 100, Tel. (886) 2 382 4443, Fax. (886) 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong,
Bangkok 10260, THAILAND,
Tel. (66) 2 745-4090, Fax. (66) 2 398-0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. (0212)279 27 70, Fax. (0212)282 67 07

Ukraine: Philips UKRAINE, 2A Akademika Koroleva str., Office 165,
252148 KIEV, Tel. 380-44-4760297, Fax. 380-44-4766991

United Kingdom: Philips Semiconductors LTD.,
276 Bath Road, Hayes, MIDDLESEX UB3 5BX,
Tel. (0181)730-5000, Fax. (0181)754-8421

United States: 811 East Arques Avenue, SUNNYVALE,
CA 94088-3409, Tel. (800)234-7381, Fax. (708)296-8556

Uruguay: Coronel Mora 433, MONTEVIDEO,
Tel. (02)70-4044, Fax. (02)92 0601

Internet: <http://www.semiconductors.philips.com/ps/>

For all other countries apply to: Philips Semiconductors,
International Marketing and Sales, Building BE-9,
P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands,
Telex 35000 phtcnl, Fax. +31-40-2724825

SCDS47 © Philips Electronics N.V. 1996

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

417041/1100/01/pp20
Document order number:

Date of release: 1996 Jan 22
9397 750 00582

Let's make things better.