MX29F805

8M-BIT [1Mx8/512Kx16] CMOS FLASH MEMORY

FEATURES

- 1,048,576 x 8/524,288 x 16 switchable
- Dual power supply operation
  - 5.0V only operation for read, 10.0V for erase and program operations
- Fast access time: 90/120ns
- Low power consumption
  - 30mA maximum active current
  - 1uA typical standby current
- Command register architecture
  - Word Programming (14us typical)
- Auto Erase and Auto Program
  - Automatically program and verify data at specified address
- Status Reply
  - Data polling & Toggle bit for detection of program and erase cycle completion.
- 100 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 42-pin PDIP

GENERAL DESCRIPTION

The MX29F805 is a 8-mega bit Flash memory organized as 1M bytes of 8 bits or 512K words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F805 is packaged in 42-pin PDIP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29F805 offers access time as fast as 90ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F805 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

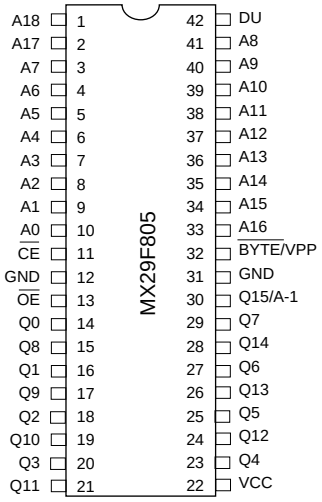
MXIC's Flash memories augment EPROM functionality with electrical erasure and programming. The MX29F805 uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX29F805 needs 10V power supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

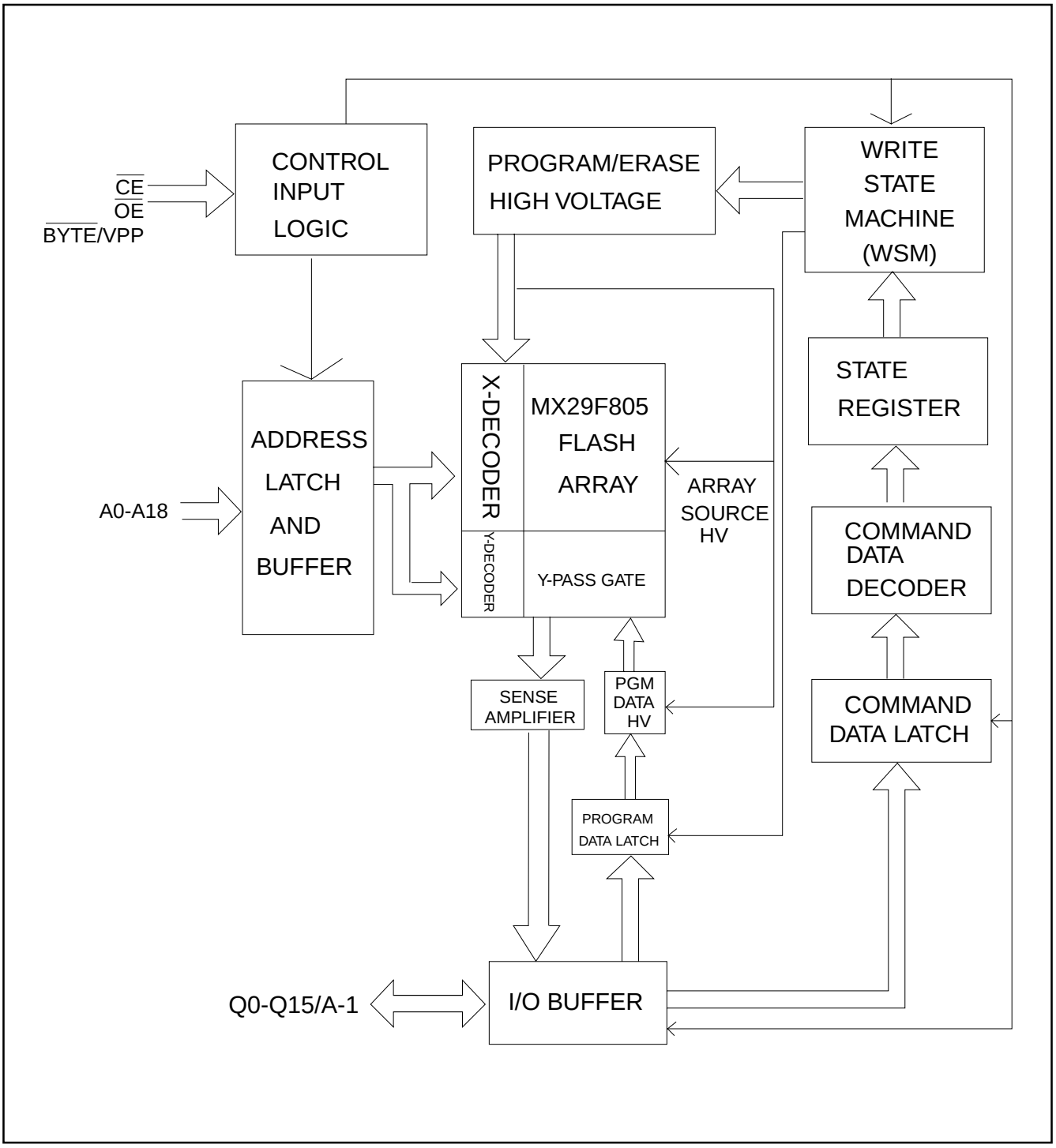
42 PDIP(600 mil)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode, for read operation only)
$\overline{CE}$	Chip Enable Input
$\overline{BYTE}$/VPP	Word/Byte Selction input, for read operation only. VPP=VHH for Erase/Program operation.
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin (+5V)
GND	Ground Pin
DU	Do Not Use

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX29F805 is word programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29F805 is less than 4 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 4 second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to DATA polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of $\overline{CE}$.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F805 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set.

TABLE1. SOFTWARE COMMAND DEFINITIONS($\overline{BYTE}$/VPP=VHH)

Command		Bus Cycle	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset		1	XXXH	F0H										
Read		1	RA	RD										
Read Silicon ID	Word	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
Porgram	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H

Legend:

1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacture code,A1=0, A0 = 1 for device code. A2 to A18=Do not care. (Refer to table 3)
   DDI = Data of Device identifier : C2H for manufacture code, B4H for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
   PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.

Note:

1. The system should generate the following address patterns: 555H or 2AAH to Address A10~A0 in word mode. Address bit A11~A18=X=Don't care for all address commands except for Program Address (PA). Write Sequence may be initiated with A11~A18 in either state.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register command sequences.

TABLE 2. MX29F805 BUS OPERATION

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$/VPP	A0	A1	A6	A9	Q0 ~ Q15
Read Silicon ID Manfacturer Code(1)	L	L	H/L	L	L	X	V_{ID}(2)	C2H (Byte mode) 00C2H (Word mode)
Read Silicon ID Device Code(1)	L	L	H/L	H	L	X	V_{ID}(2)	B4H (Byte mode) 22B4H (Word mode)
Read	L	L	H/L	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H/L	X	X	X	X	HIGH Z
Write(6)	L	H	VHH	A0	A1	A6	A9	D_{IN}(3)
Reset	X	X	X	X	X	X	X	HIGH Z

NOTES:
1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage(VID). However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F805 contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H/00C2H. A read cycle with A1=VIL, A0=VIH returns the device code of for MX29F805.

SET-UP AUTOMATIC CHIP ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last $\overline{CE}$ pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 3. EXPANDED SILICON ID CODE

Pins		A0	A1	Q15~Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	Word	VIL	VIL	00H	1	1	0	0	0	0	1	0	00C2H
	Byte	VIL	VIL	X	1	1	0	0	0	0	1	0	C2H
Device code	Word	VIH	VIL	22H	1	1	0	1	0	1	1	0	22B4H
for MX29F805	Byte	VIH	VIL	X	1	1	0	1	0	1	1	0	B4H

Table 4. Write Operation Status

Status	Operation	Q7	Q6	Q5	Q3	Q2
In Progress	Byte Program in Auto Program Algorithm	$\overline{Q7}$	Toggle	0	N/A	No Toggle
	Auto Erase Algorithm	0	Toggle	0	1	Toggle
Exceeded Time Limits	Byte Program in Auto Program Algorithm	$\overline{Q7}$	Toggle	1	N/A	No Toggle
	Program/Erase in Auto Erase Algorithm	0	Toggle	1	1	Toggle

Notes:
1.Performing successive read operations from any address will cause Q6 to toggle while in program/erase mode.
2.Reading the byte address being programmed will indicate No Toggle at the Q2 bit.

SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next $\overline{CE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the $\overline{CE}$ pulse. The rising edge of $\overline{CE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program opetation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode(no program verify command is required).

$\overline{DATA}$ POLLING-Q7

The MX29F805 also features $\overline{Data}$ Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The $\overline{Data}$ Polling feature is valid after the rising edge of the fourth $\overline{CE}$ pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The $\overline{Data}$ Polling feature is valid after the rising edge of the sixth $\overline{CE}$ pulse of six write pulse sequences for automatic chip/sector erase.

The $\overline{Data}$ Polling feature is active during Automatic Program/Erase algorithm

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete. Toggle Bit I may be read at any address, and is valid after the rising edge of the final CE pulse in the command sequence(prior to the program or erase operation).

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE or CE to control the read cycles. When the operation is complete, Q6 stops toggling.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether the device is actively eraseing (that is, the Automatic Erase alorithm is in process), or whether that sector is erase-suspended. Toggle Bit I is valid after the rising edge of the final CE pulse in the command sequence.

Q2 toggles when the device is in erase operation. (The system may use either OE or CE to control the read cycles.) Refer to Table 4 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfuly completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits(internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad.

If this time-out condition occurs during the byte programming operation, it specifies that byte is bad and maynot be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

DATA PROTECTION

The MX29F805 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{CE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or BYTE/VPP=VIH/VIL To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

POWER-UP SEQUENCE

The MX29F805 powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9,$\overline{OE}$	-0.5V to 13.5V
$\overline{BYTE}$/VPP	-0.5V to 10.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			8	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V±10%

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			± 1	uA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	$\overline{CE}$ = VIH
ISB2			0.2	5	uA	$\overline{CE}$ = VCC + 0.3V
ICC1	Operating VCC current			30	mA	IOUT = 0mA, f=1MHz
ICC2				50	mA	IOUT= 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH1	Output High Voltage(TTL)	2.4			V	IOH = -2mA
VOH2	Output High Voltage(CMOS)	VCC-0.4			V	IOH = -100uA, VCC=VCC MIN.

NOTES:
1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

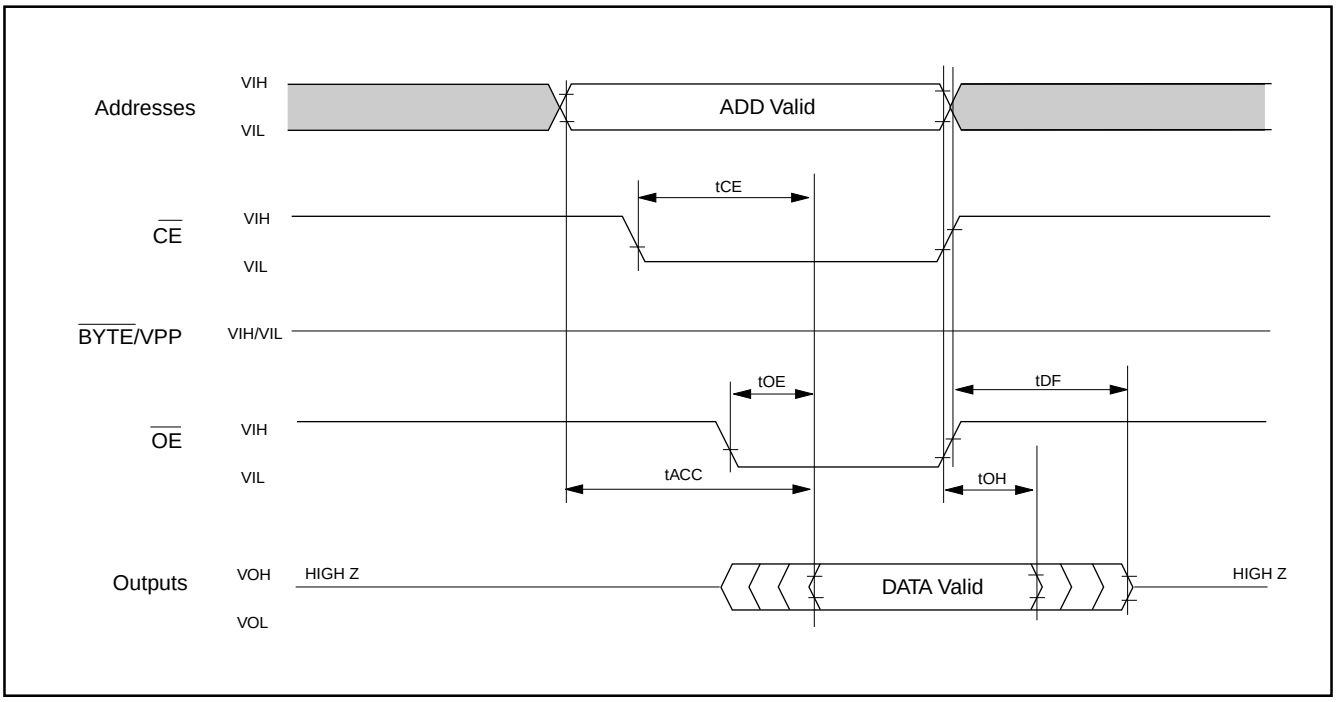
		29F805-90		29F805-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		90		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		90		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		40		50	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	0	30	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times is equal to or less than 10ns
- Output load: 1 TTL gate + 100pF (Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

NOTE:
1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

READ TIMING WAVEFORMS



COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

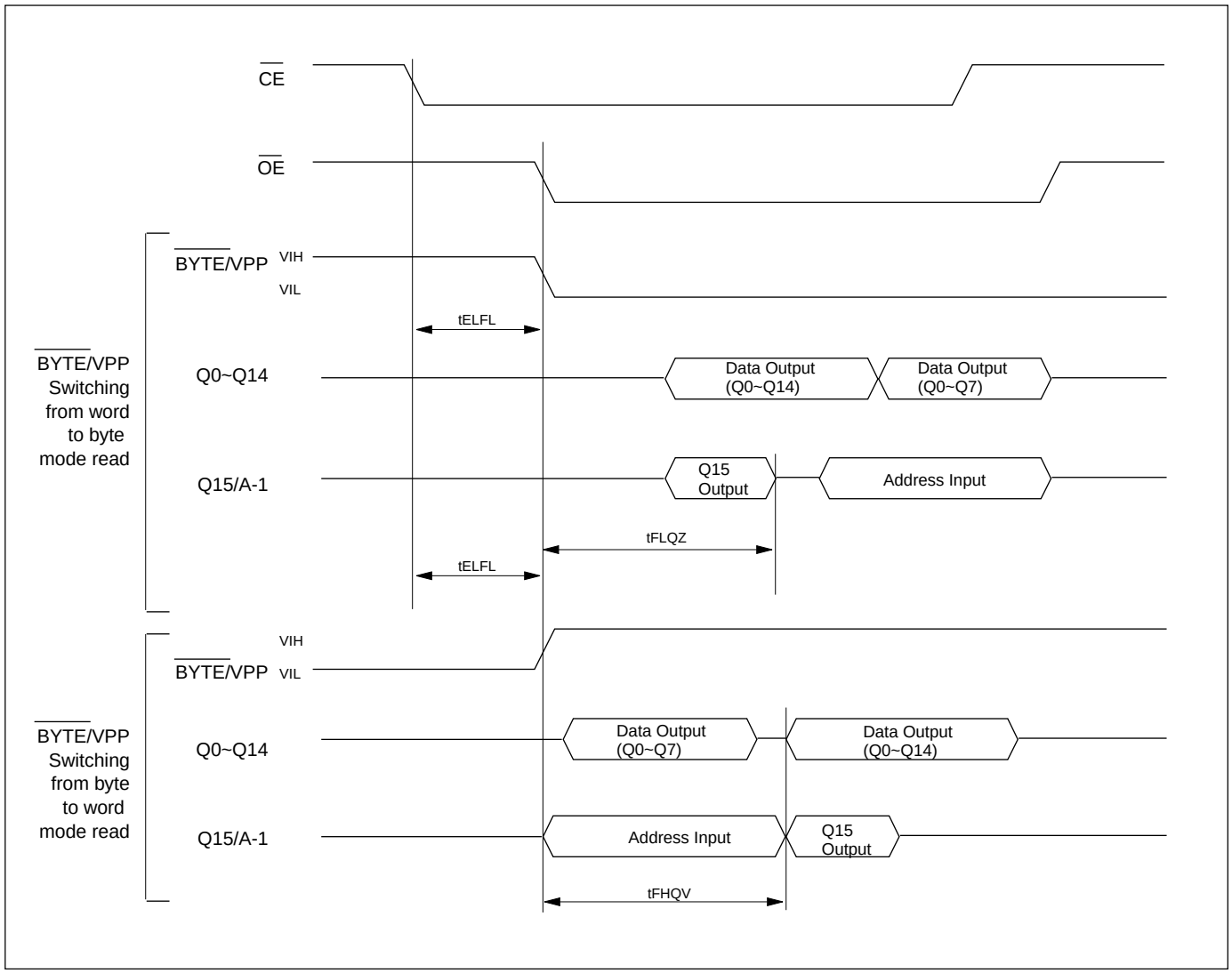
SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ICC1 (Read)	Operating VCC Current			30	mA	IOUT=0mA, f=1MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	$\overline{CE}$=VIH, Erase Suspended

NOTES:
1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.

AC CHARACTERISTICS—WORD/BYTE CONFIGURATION ($\overline{BYTE}$/VPP)

SYMBOL	Description		Speed Options		unit
			90	120	
tELFL/tELFH	$\overline{CE}$ to $\overline{BYTE}$/VPP Switching Low or High	MAX	5	5	ns
tFLQZ	$\overline{BYTE}$/VPP Switching Low to Output HIHG Z	Max	30	30	ns
tFHQV	$\overline{BYTE}$/VPP Switching High to Output Active	Min	90	120	ns

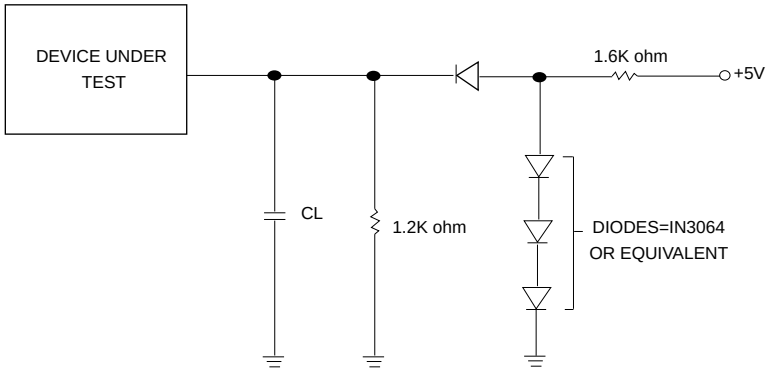
Figure 6. $\overline{BYTE}$/VPP TIMING WAVEFORMS



AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

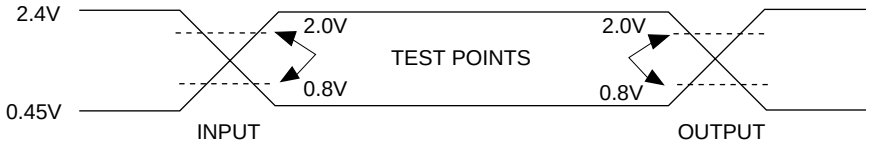
		29F805-90		29F805-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tOES	$\overline{OE}$ setup time	50		50		ns	
tCWC	Command programming cycle	90		120		ns	
tAS	Address setup time	0		0		ns	
tAH	Address hold time	45		50		ns	
tVPS	$\overline{BYTE}$/Vpp Setup Time	2		2		us	
tVPH	$\overline{BYTE}$/Vpp Hold Time	2		2		us	
tCESC	CE setup time before command write	0		0		ns	
tAETC	Total erase time in auto chip erase	8(TYP.)		8(TYP.)		s	
tAVT	Total programming time in auto verify (word program time)	14(TYP.)		14(TYP.)		us	
tCH	$\overline{CE}$ Hold Time	0		0		ns	
tCS	$\overline{CE}$ setup to $\overline{WE}$ going low	0		0		ns	
tVLHT	Voltge Transition Time	4		4		us	
tOESP	$\overline{OE}$ Setup Time to $\overline{BYTE}$/VPP Active	4		4		us	

SWITCHING TEST CIRCUITS



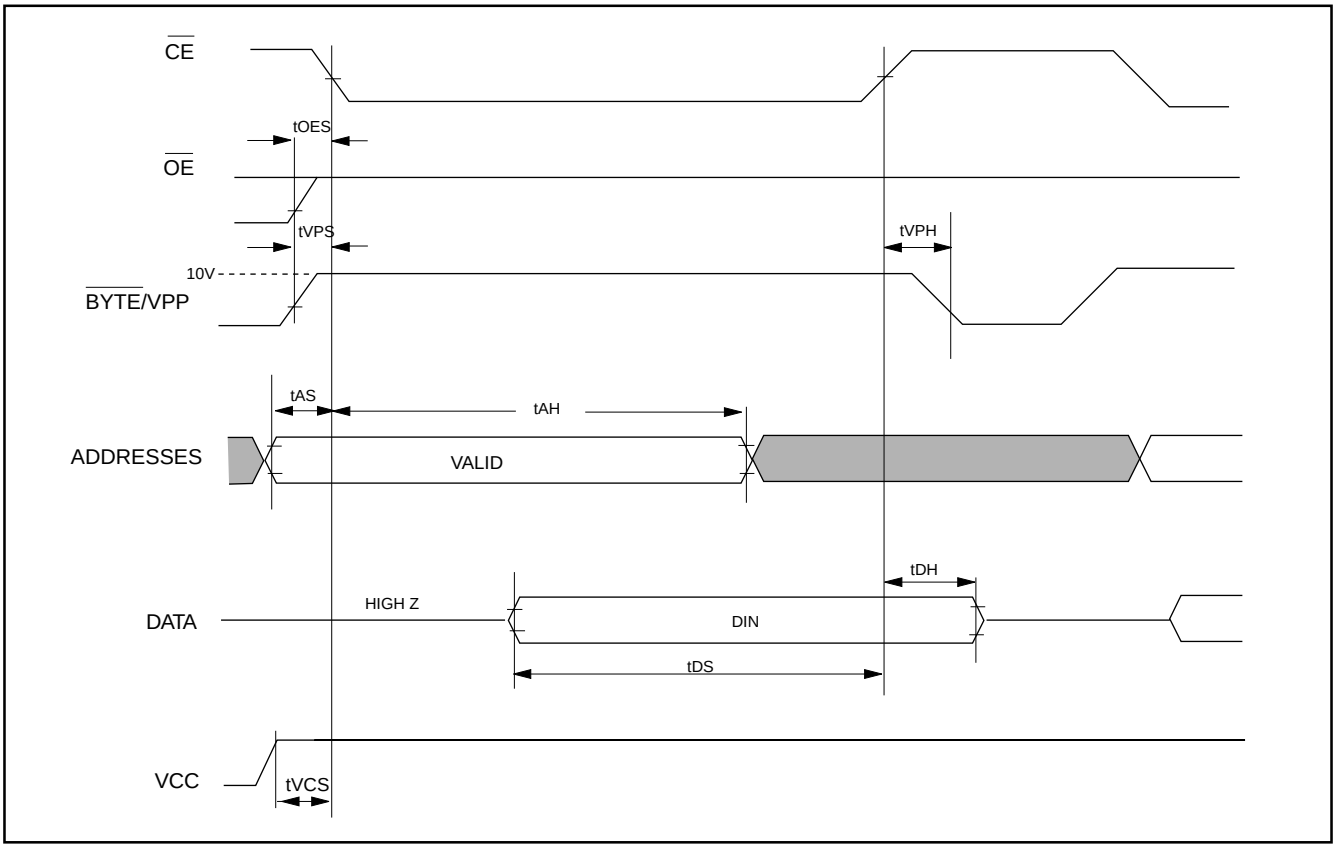
CL=100pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are <20ns.

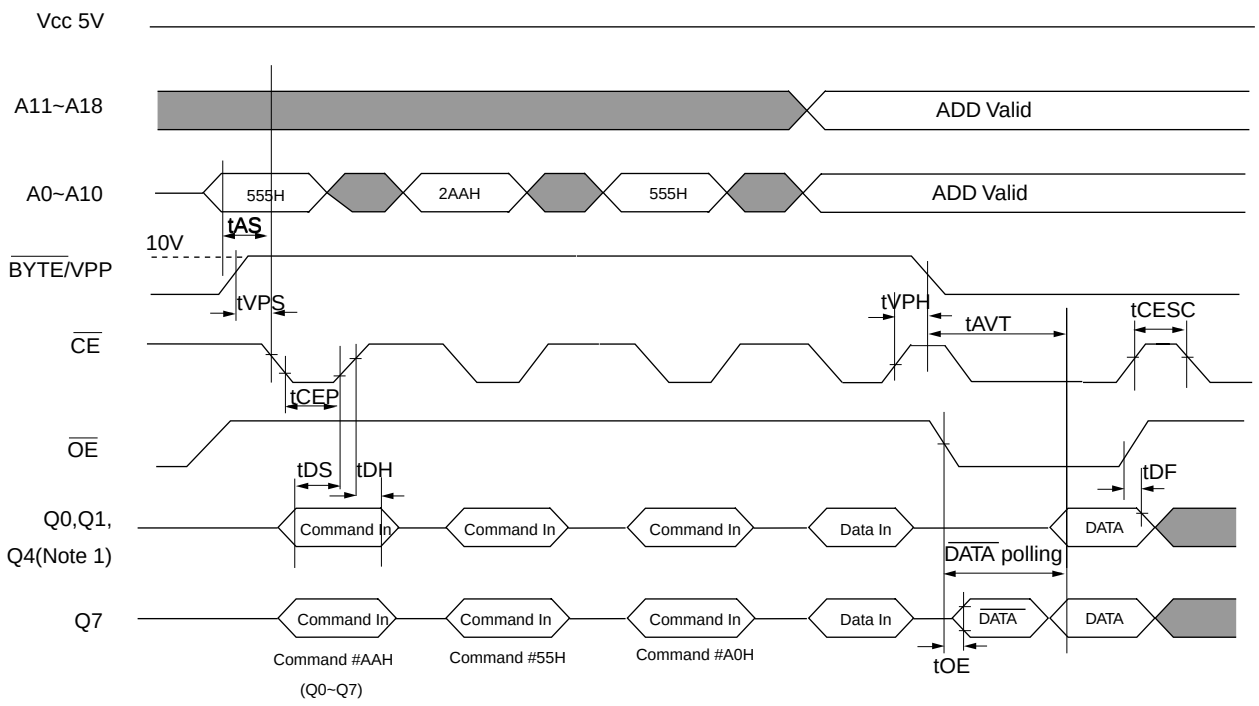
COMMAND WRITE TIMING WAVEFORM



AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic verification starts. Device outputs $\overline{DATA}$ during programming and DATA after programming on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

AUTOMATIC PROGRAMMING TIMING WAVEFORM (WORD MODE)

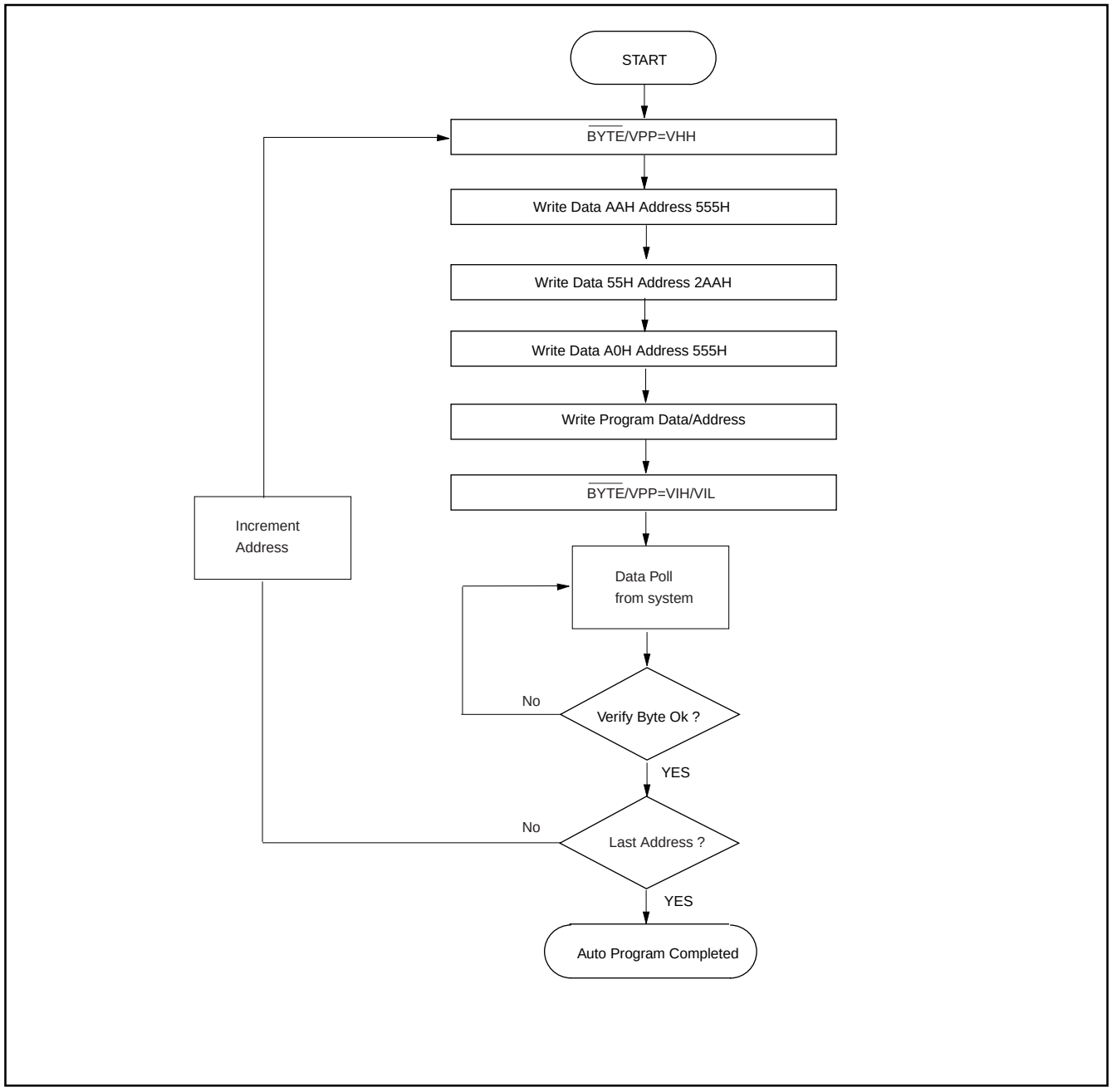


Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q2: Toggle bit

(2). $\overline{BYTE}$/VPP must not be VHH while reading status.

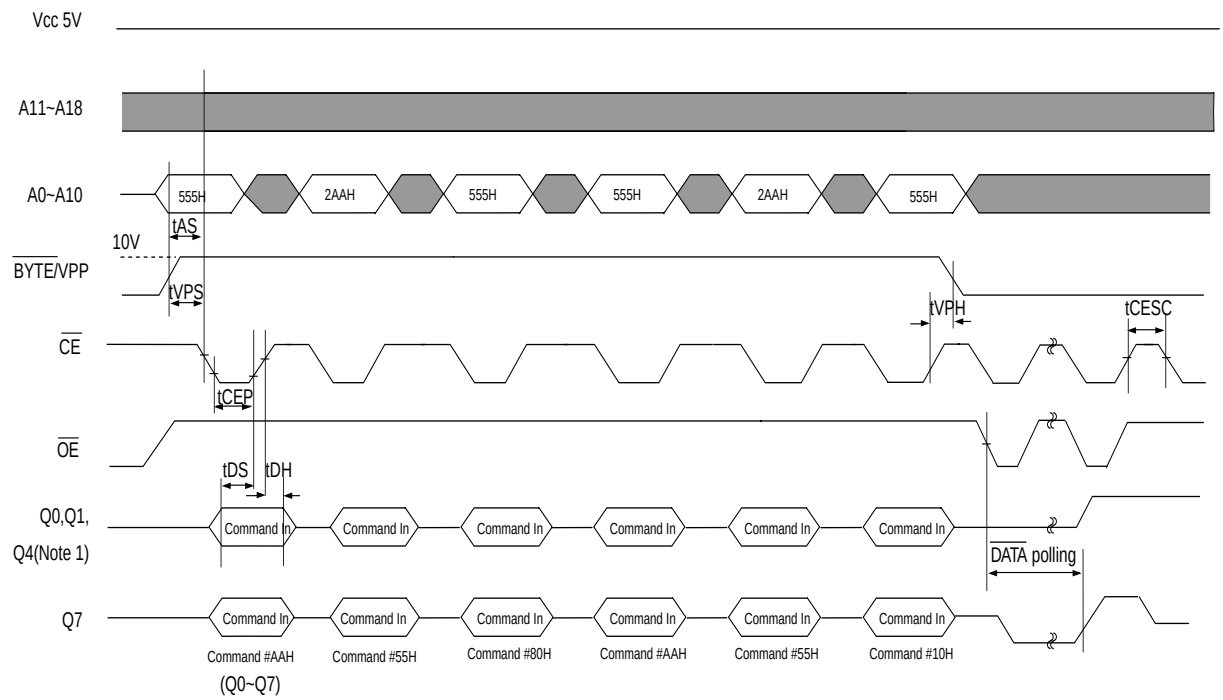
AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART (WORD MODE)



AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

AUTOMATIC CHIP ERASE TIMING WAVEFORM (WORD MODE)

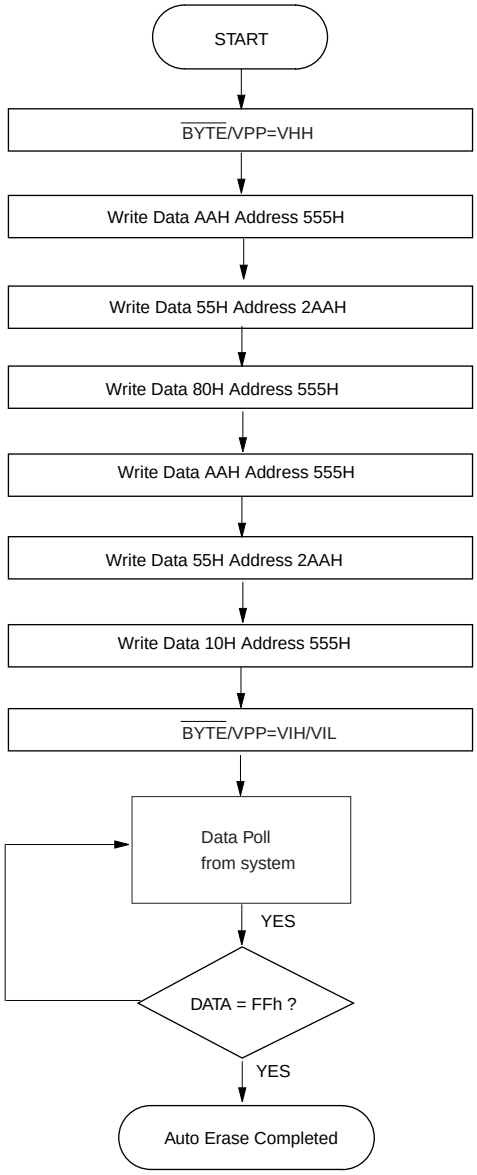


Notes:

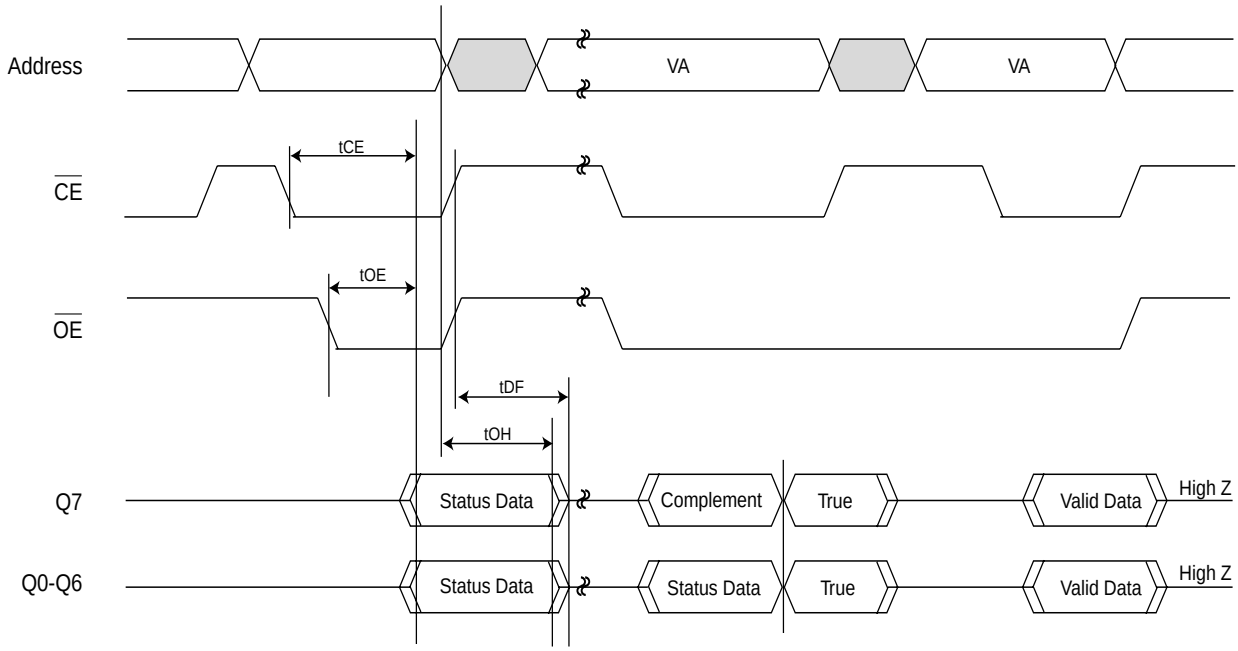
(1). Q6:Toggle bit, Q5:Timing-limit bit, Q2: Toggle bit

(2). BYTE/VPP must not be VHH while reading status.

AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART (WORD MODE)



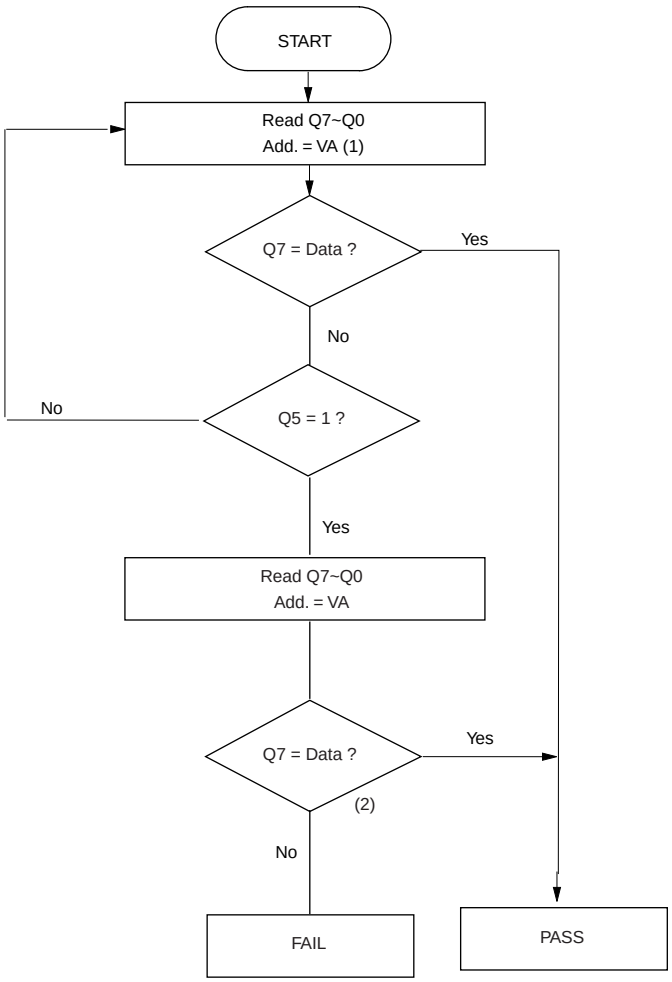
$\overline{\text{DATA}}$ POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



NOTES:

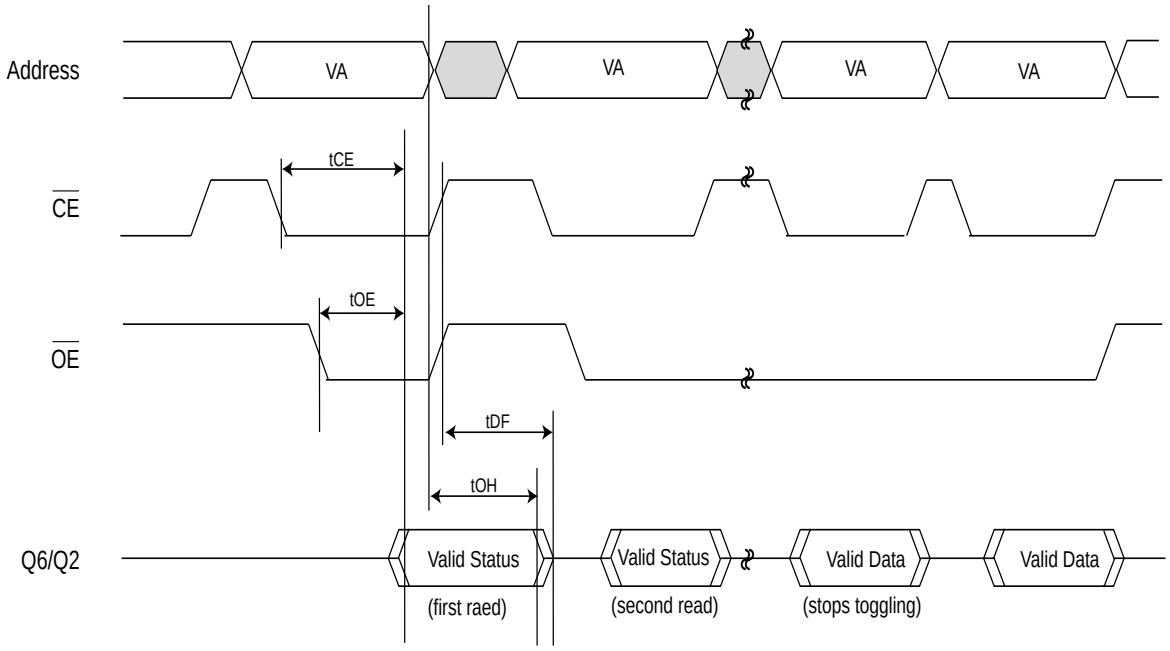
VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data raed cycle.

$\overline{\text{Data}}$ Polling Algorithm



Notes:
1. VA=valid address for programming.
2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

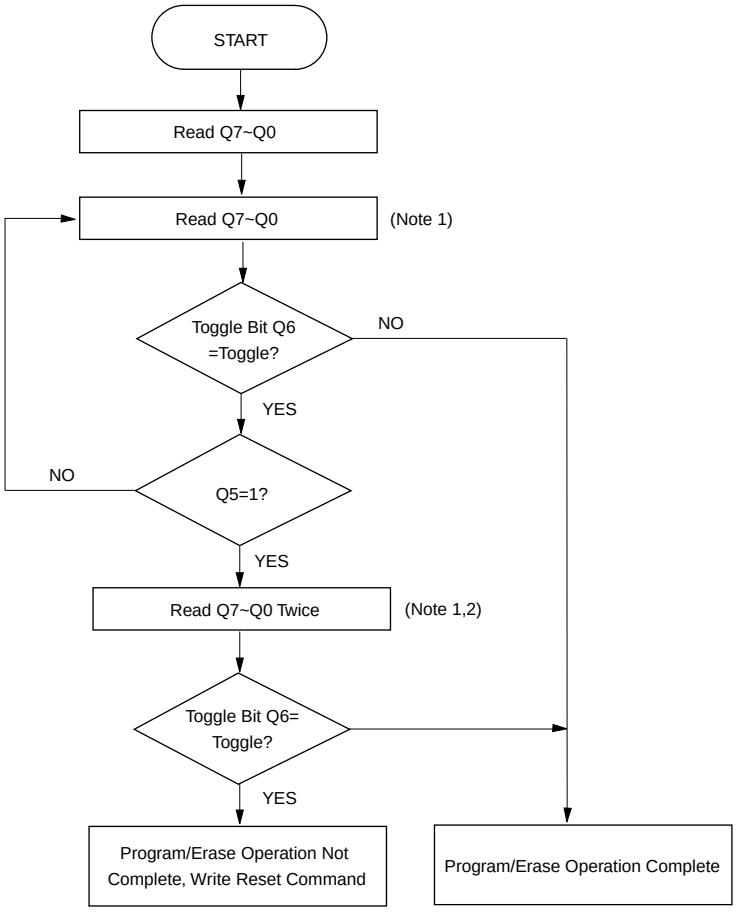
TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALOGRITHMS)



NOTES:

VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

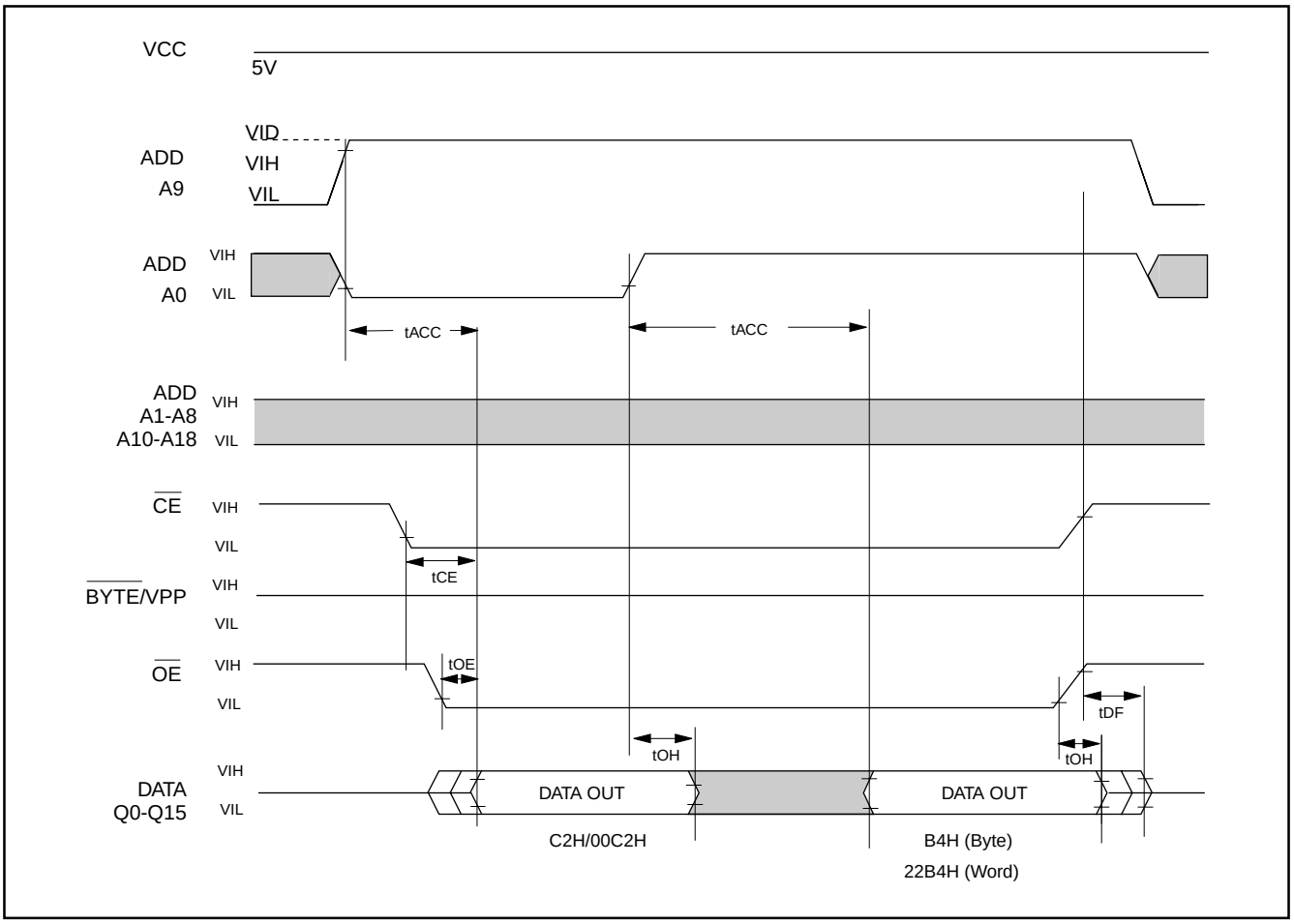
Toggle Bit Algorithm



Note:

1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

ID CODE READ TIMING WAVEFORM



ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA, at10MHz)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29F805PC-90	90	50	5	42 Pin PDIP
MX29F805PC-12	120	50	5	42 Pin PDIP

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Chip Erase Time		16	128	sec
Word Programming Time		14	21	us
Chip Programming Time		7	21	sec
Erase/Program Cycles	100			Cycles

LATCHUP CHARACTERISTICS

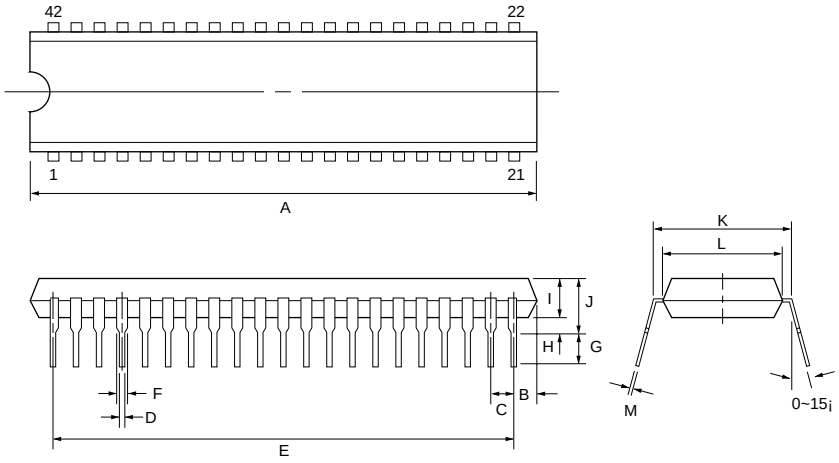
	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

PACKAGE INFORMATION

42-PIN PLASTIC DIP(600 mil)

ITEM	MILLIMETERS	INCHES
A	52.54 max.	2.070 max.
B	0.76 [REF]	.030 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.018 [Typ.]
E	50.76	2.000
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± . 25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± . 25	.155 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .010
L	13.97± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



REVISION HISTORY

Revision	Description	Page	Date
0.1	Remove sector-related features of sector structure, sector protect/unprotect, sector erase suspend/resume, and top/bottom boot block	P1~10, 12~14 P17, 20~30, 32	OCT/06/1999
	Add Data polling and toggle bit timing waveforms and flowcharts	P21, 22	
	Change device ID to B4H	P5, 6, 7, 25	

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