Advance Information

TMOS E-FET™ Power Field Effect Transistors D²PAK for Surface Mount Logic Level TMOS (L²TMOS™)

N–Channel Enhancement–Mode Silicon Gate

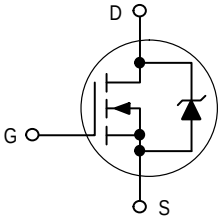
MTB50N06EL

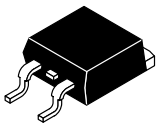
Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
50 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.028 OHM

These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers. This Logic Level Series part is specified to operate with level logic gate–to–source voltage of 5 volt and 4 volt.

- Silicon Gate for Fast Switching Speeds
- Low R_{DS}(on) — 0.028 Ω max
- Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous	V_{GS}	±15	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	50 28 142	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vpk, I_L = 50 Apk, L = 0.32 mH, R_G = 25 Ω)	E_{AS}	400	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Thermal Clad is a trademark of the Bergquist Company

Preferred devices are Motorola recommended choices for future use and best overall value.

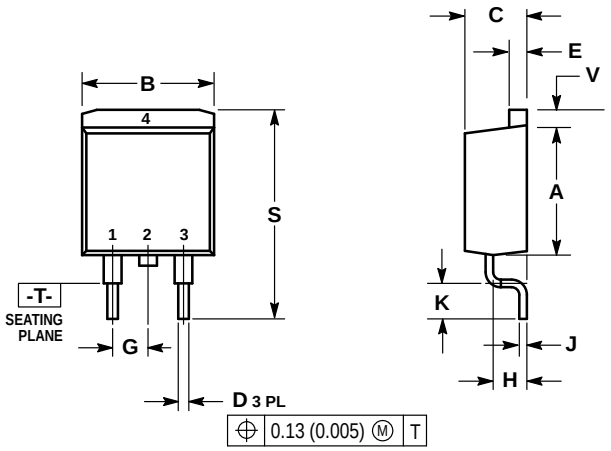
REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	64	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	—	2.0	Vdc
Temperature Coefficient (Negative)			—	4.78	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 25 Adc)		$R_{DS(on)}$	—	—	0.028	Ohm
(V_{GS} = 4.0 Vdc, I_D = 25 Adc)			—	—	0.039	
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 50 Adc)		$V_{DS(on)}$	—	—	1.68	Vdc
(I_D = 25 Adc, T_J = 125°C)			—	—	1.40	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 25 Adc)		g_{FS}	17	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3100	4340	pF
Output Capacitance		C_{oss}	—	1065	1491	
Reverse Transfer Capacitance		C_{rss}	—	260	520	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 25 Vdc, I_D = 50 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	21	42	ns
Rise Time		t_r	—	365	730	
Turn–Off Delay Time		$t_{d(off)}$	—	55	110	
Fall Time		t_f	—	150	300	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 50 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	52	73	nC
		Q_1	—	13	—	
		Q_2	—	34	—	
		Q_3	—	27	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 50 Adc, V_{GS} = 0)	V_{SD}	—	1.52	2.5	Vdc
	(I_S = 50 Adc, V_{GS} = 0, T_J = °C)		—	1.1	—	
Reverse Recovery Time	(I_S = 50 Adc, V_{GS} = 0 , dI_S/dt = 100 A/μs)	t_{rr}	—	200	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the tab to center of die)		L_d	—	3.5	—	nH
Internal Source Inductance (Measured from the source lead 0.1″ from package to source bond pad)		L_s	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

CASE 418B–02
ISSUE B

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