MN86062

CODEC LSI for Facsimile Images

■ Overview

The MN86062 is a high-speed LSI codec for compressing and decompressing images using the MH, MR, and MMR standard compression methods specified in the ITU-T T.4 and T.6 recommendation. Registers and other settings provide flexible support for a variety of processing.

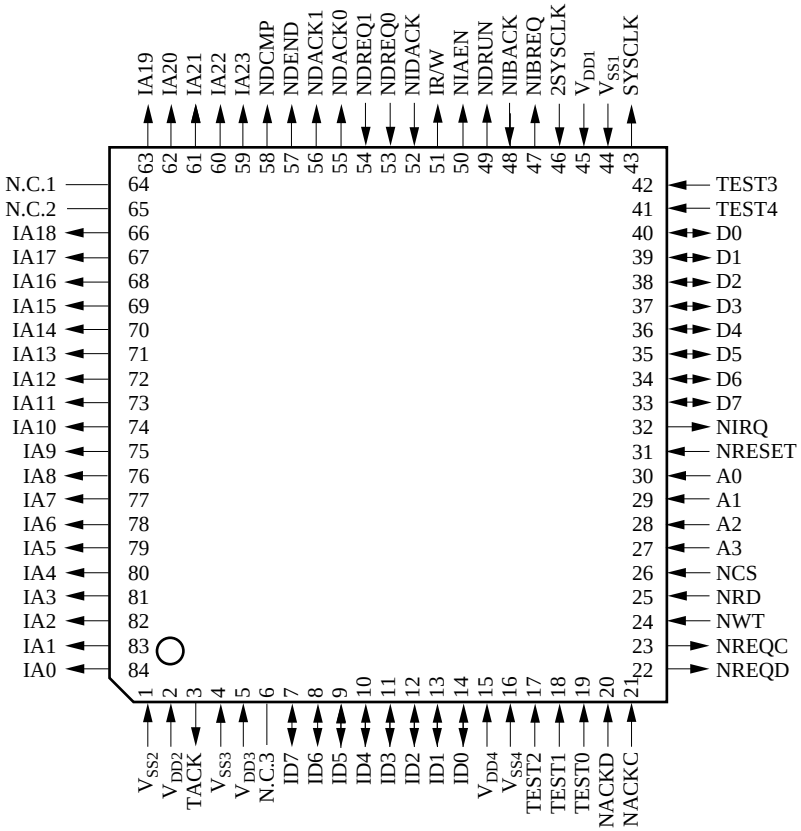
■ Features

- Compression methods
  MH, MR, and MMR
- Operating mode:
  Page mode
- Bus configuration:
  Choice of dual- or single-bus operation
- Decoding error processing:
  Choice of replacing with the previous line or a white line
- Image bus configuration:
  8 bits, maximum 16 megabytes address space of image bus, 2-channel master DMA
- System bus configuration:
  X80 interface compatible, 8 bits, 2-channel slave DMA
- Pixels per line:
  maximum 64K, in byte increments
- Concurrent DMA transfers over image bus and command processing
- Support for pointer management for image buffer
- Wide selection of independent parameters for coding, decoding, transfers between buses, and DMA transfersr
- Support for time-shared processing by line for both coding and decoding

■ Applications

- Facsimile equipment

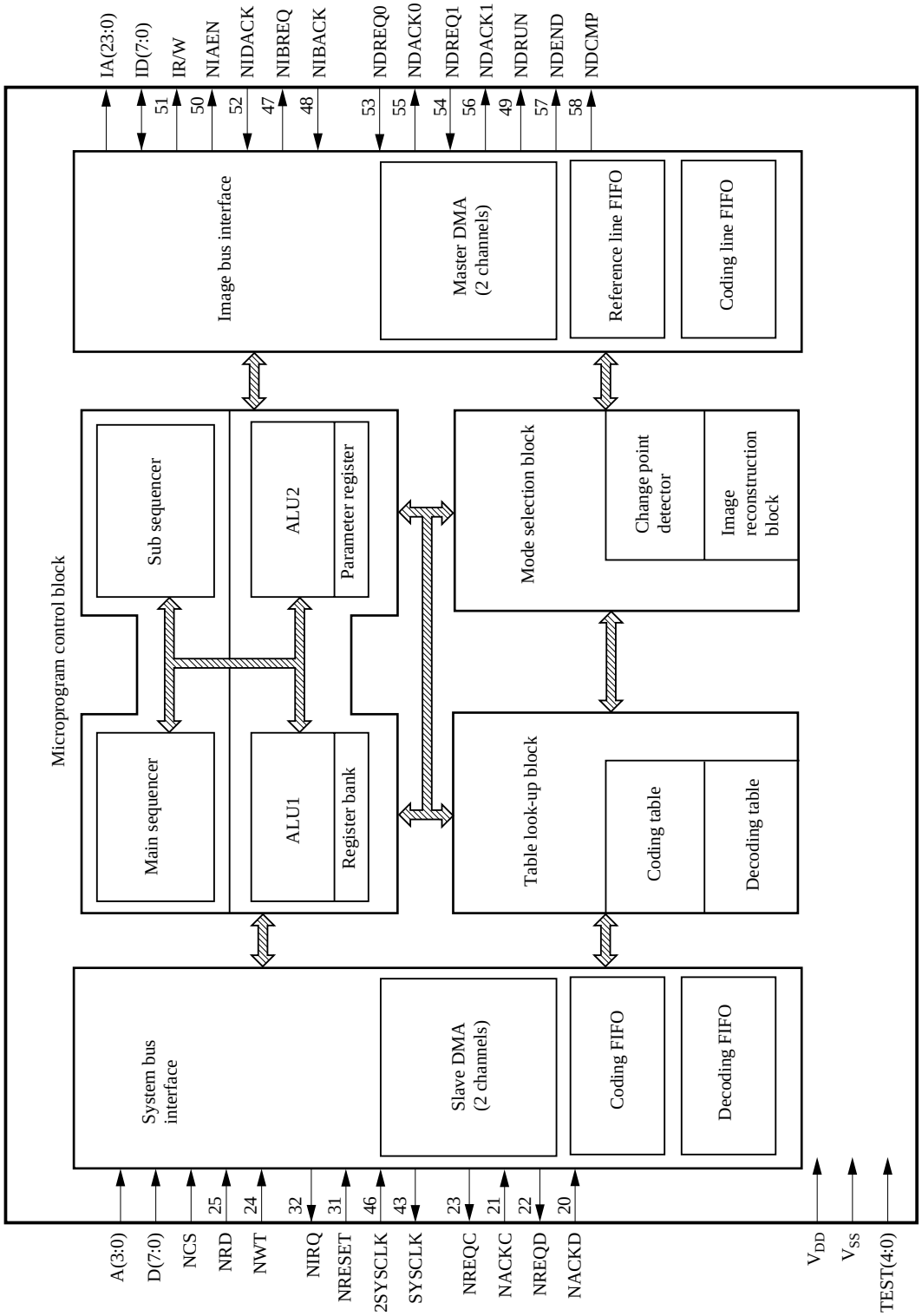
■ Pin Assignment



(TOP VIEW)

QFP084-P-1818

■ Block Diagram



■ Pin Descriptions

● System Bus Interface

Pin No.	Symbol	I/O	Function Description
27	A3	I	Address bus for accessing internal registers
28	A2		
29	A1		
30	A0		
33	D7	I/O	Data bus for bidirectional transfers over system bus
34	D6	Tristate	
35	D5		
36	D4		
37	D3		
38	D2		
39	D1		
40	D0		
24	NWT	I	Connect to WR pin on X80-compatible microprocessor
25	NRD	I	Connect to RD pin on X80-compatible microprocessor
26	NCS	I	Chip select pin
23	NREQC	O Tristate	This output pin indicates a DMA transfer request from the 86062 to memory.
22	NREQD	O Tristate	This output pin indicates a DMA transfer request from the memory to 86062.
21	NACKC	I	This input pin accepts the response to the NREQC signal.
20	NACKD	I	This input pin accepts the response to the NREQD signal.
32	NIRQ	O Open drain	This output pin indicates an interrupt request.
31	NRESET	I	External input resets the 86062.
46	2SYSCLK	I	This input pin accepts a clock signal with twice the system clock frequency.
43	SYSCLK	O	This output pin provides a clock signal with half the frequency of 2SYSCLK.
15	V_{DD4}	I	Connect these power supply pins to a 5 volt power supply.
5	V_{DD3}		
2	V_{DD2}		
45	V_{DD1}		
16	V_{SS4}	I	Connect these power supply pins to ground.
4	V_{SS3}		
1	V_{SS2}		
44	V_{SS1}		
41	TEST4	I	Do not use these test pins.
42	TEST3		
17	TEST2		
18	TEST1		
19	TEST0		
3	TACK	O	Do not use these test pins.

■ Pin Descriptions (continued)

● Image Bus Interface (continued)

Pin No.	Symbol	I/O	Function Description
59	IA23	O	Image address bus. The address is valid when the NIAEN pin is at "L"
60	IA22	Tristate	level.
61	IA21		
62	IA20		
63	IA19		
66	IA18		
67	IA17		
68	IA16		
69	IA15		
70	IA14		
71	IA13		
72	IA12		
73	IA11		
74	IA10		
75	IA9		
76	IA8		
77	IA7		
78	IA6		
79	IA5		
80	IA4		
81	IA3		
82	IA2		
83	IA1		
84	IA0		
7	ID7	I/O	Image data bus for bidirectional transfers of image data
8	ID6	Tristate	
9	ID5		
10	ID4		
11	ID3		
12	ID2		
13	ID1		
14	ID0		
47	IBREQ	O	This output pin indicates a request for control of the image bus.
48	IBACK	I	This input pin accepts the response to the NIBREQ signal.
50	IAEN	O	This output pin indicates whether the values of image address bus are
		Tristate	valid.
51	IR/W	O	This output pin indicates the data transfer direction for the image bus.
		Tristate	

■ Pin Descriptions (continued)

- Image Bus Interface (continued)

Pin No.	Symbol	I/O	Function Description
52	IDACK	I	This input pin indicates the end of a data read or write operation.
49	DRUN	O Tristate	This output pin indicates whether a DMA transfer is in progress.
57	DEND	O	This output pin indicates the end of a DMA cycle.
58	DCMP	O	This output pin indicates successful completion of a DMA block transfer.
53	DREQ0	I	This input pin indicates a DMA transfer request from the I/O block to memory.
54	DREQ1	I	This input pin indicates a DMA transfer request from the memory to I/O block.
55	DACK0	O	This output pin gives the response to the NDREQ0 signal.
56	DACK1	O	This output pin gives the response to the NDREQ1 signal.

- Test Pin Setting

Symbol	Pin No.	Fixed Level
TEST0	19	GND
TEST1	18	GND
TEST2	17	GND
TEST3	42	GND
TEST4	41	GND

■ Package Dimensions (Unit: mm)

QFP084-P-1818