MN8280

Video Signal Processing LSI for Wide-Screen TVs

■ Overview

This LSI offers these and other functions for wide-screen TV receivers: 3-dimensional Y/C separation, color decoding, and horizontal compression.

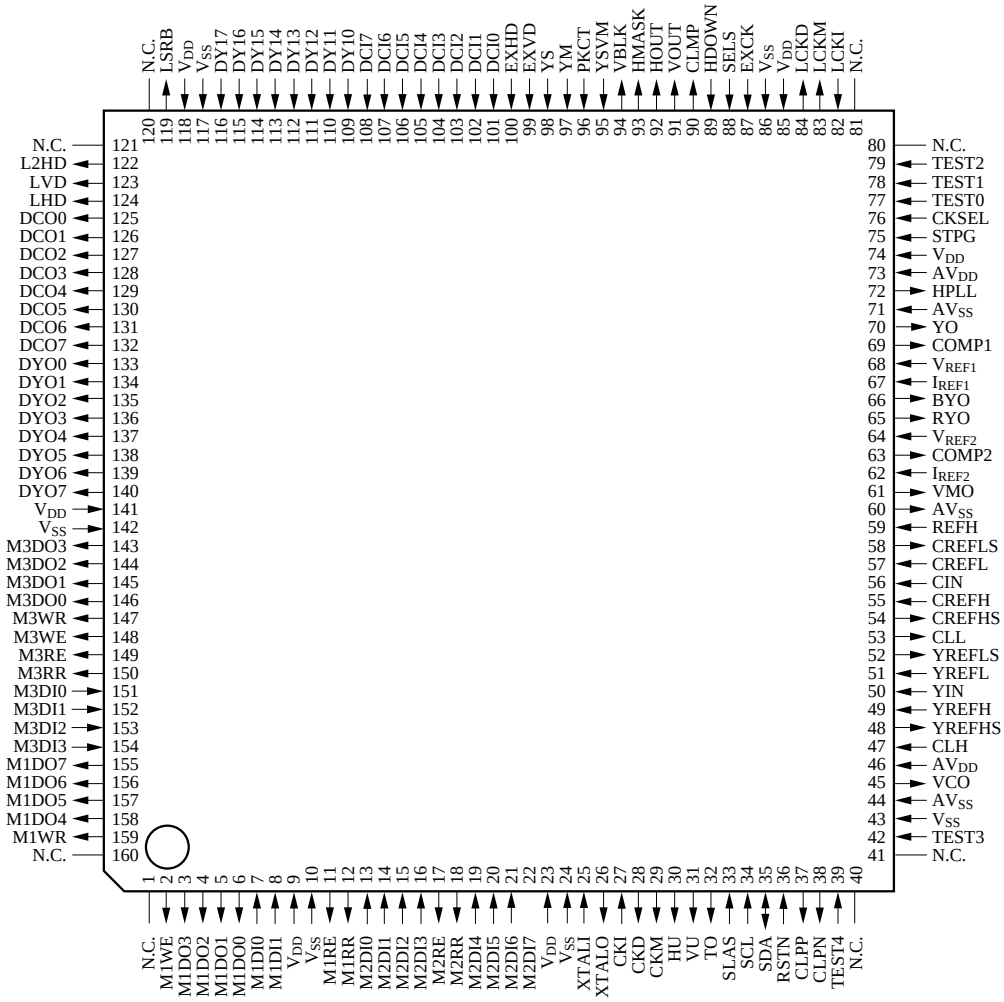
■ Features

- 3-dimensional Y/C separation
- Color demodulation
- Automatic change of aspect ratio
- EDTV identifier signal detector
- HH playback
- Synchronization signal separation
- Horizontal and vertical contour correction
- Subtitle processing
- VT/VH demodulation
- Luminance optimization contour correction
- Operating voltage 5V

■ Applications

- Wide-screen TV receivers

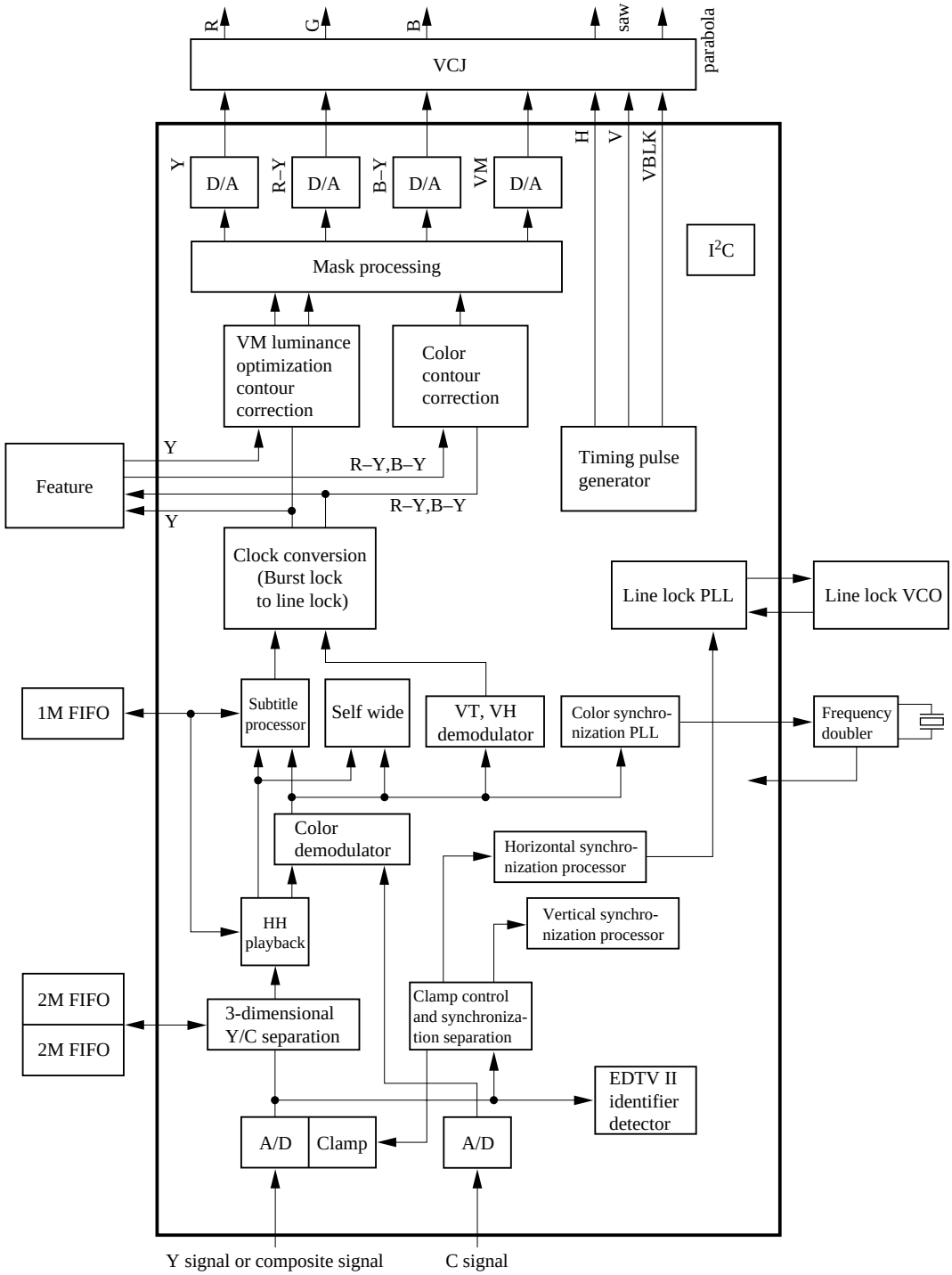
■ Pin Assignment



(TOP VIEW)

QFP160-P-2828B

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
1	N.C.	—	No connection
2	M1WE	O	Write enable output pin for memory chip 1
3	M1DO3	O	Data output pin for memory chip 1
4	M1DO2	O	Data output pin for memory chip 1
5	M1DO1	O	Data output pin for memory chip 1
6	M1DO0	O	Data output pin for memory chip 1
7	M1DI0	I	Data input pin for memory chip 1
8	M1DI1	I	Data input pin for memory chip 1
9	V_{DD}	I	Power supply
10	V_{SS}	I	GND
11	M1RE	O	Read enable output pin for memory chip 1
12	M1RR	O	Read reset output pin for memory chip 1
13	M2DI0	I	Data input pin for memory chip 2
14	M2DI1	I	Data input pin for memory chip 2
15	M2DI2	I	Data input pin for memory chip 2
16	M2DI3	I	Data input pin for memory chip 2
17	M2RE	O	Read enable output pin for memory chip 2
18	M2RR	O	Read reset output pin for memory chip 2
19	M2DI4	I	Data input pin for memory chip 2
20	M2DI5	I	Data input pin for memory chip 2
21	M2DI6	I	Data input pin for memory chip 2
22	M2DI7	I	Data input pin for memory chip 2
23	V_{DD}	I	Power supply
24	V_{SS}	I	GND
25	XTALI	I	Burst lock clock input pin (28 MHz)
26	XTALO	O	Burst lock clock output pin (28 MHz)
27	CKI	I	Memory interface clock input pin (28 MHz)
28	CKD	O	Burst lock clock output pin (28 MHz)
29	CKM	O	Burst lock clock output pin (14 MHz)
30	HU	O	Horizontal pulse output pin (burst lock)
31	VU	O	Vertical pulse output pin (burst lock)
32	TO	O	Test output pin
33	SLAS	I	Slave address selection pin
34	SCL	I	I^2C clock input pin
35	SDA	I/O	I^2C data I/O pin
36	RSTN	I	Reset signal input pin (Normally "H" level)
37	CLPP	O	External clamp control pin (P-channel)
38	CLPN	O	External clamp control pin (N-channel)
39	TEST4	I	Test pin (Normally "L" level)
40	N.C.	—	No connection

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
41	N.C.	—	No connection
42	TEST3	I	Test pin (Normally "L" level)
43	V_{SS}	I	GND
44	AV_{SS}	I	GND
45	VCO	AO	R-2R D/A converter output (burst lock PLL)
46	AV_{DD}	I	Power supply
47	CLH	A	Clamp current source selection pin
48	YREFHS	A	Luminance A/D converter reference voltage output pin (upper limit)
49	YREFH	A	Luminance A/D converter reference voltage input pin (upper limit)
50	YIN	AI	Luminance signal input pin
51	YREFL	A	Luminance A/D converter reference voltage input pin (lower limit)
52	YREFLS	A	Luminance A/D converter reference voltage output pin (lower limit)
53	CLL	A	Clamp current source selection pin
54	CREFHS	A	Chrominance A/D converter reference voltage output pin (upper limit)
55	CREFH	A	Chrominance A/D converter reference voltage input pin (upper limit)
56	CIN	AI	Chrominance signal input pin
57	CREFL	A	Chrominance A/D converter reference voltage input pin (lower limit)
58	CREFLS	A	Chrominance A/D converter reference voltage output pin (lower limit)
59	REFH	I	R-2R power supply
60	AV_{SS}	I	GND
61	VMO	O	VM signal output pin (DAC2)
62	I_{REF2}	A	DAC2 reference current setting pin
63	COMP2	A	DAC2 phase compensation pin
64	V_{REF2}	A	DAC2 reference voltage setting pin
65	RYO	AO	Color difference (R-Y) signal output pin (DAC1)
66	BYO	AO	Color difference (B-Y) signal output pin (DAC1)
67	I_{REF1}	A	DAC1 reference current setting pin
68	V_{REF1}	A	DAC1 reference voltage setting pin
69	COMP1	A	DAC1 phase compensation pin
70	YO	AO	Brightness signal output pin (DAC1)
71	AV_{SS}	I	GND
72	HPLL	AO	R-2R D/A converter output (line lock PLL)
73	AV_{DD}	I	Power supply
74	V_{DD}	I	Power supply
75	STPG	I	Test pin (Normally "L" level)
76	CKSEL	I	Test pin (Normally "L" level)
77	TEST0	I	Test pin (Normally "L" level)
78	TEST1	I	Test pin (Normally "L" level)
79	TEST2	I	Test pin (Normally "L" level)
80	N.C.	—	No connection

Note: The I/O column uses the following abbreviations: A for analog setting pin, AI for analog input, and AO for analog output.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
81	N.C.	—	No connection
82	LCKI	I	Line lock clock input pin (28 MHz)
83	LCKM	O	Line lock clock output pin (14 MHz)
84	LCKD	O	Line lock clock output pin (28 MHz)
85	V_{DD}	I	Power supply
86	V_{SS}	I	GND
87	EXCK	I	Image quality correction block external clock input pin (28 MHz)
88	SELS	I	Image quality correction block clock selection pin
89	HDOWN	I	Hold down input pin
90	CLMP	O	Clamp pulse output pin
91	VOUT	O	Vertical pulse output pin
92	HOUT	O	Horizontal pulse output pin
93	HMASK	O	Horizontal mask signal output pin
94	VBLK	O	Vertical blanking signal output pin
95	YSVM	I	VM signal control input pin
96	PKCT	I	Image quality correction control signal input pin
97	YM	I	Video signal gain control input pin
98	YS	I	Video signal select signal input pin
99	EXVD	I	External vertical pulse input pin
100	EXHD	I	External horizontal pulse input pin
101	DCI0	I	Color difference signal input pin 0 (LSB)
102	DCI1	I	Color difference signal input pin 1
103	DCI2	I	Color difference signal input pin 2
104	DCI3	I	Color difference signal input pin 3
105	DCI4	I	Color difference signal input pin 4
106	DCI5	I	Color difference signal input pin 5
107	DCI6	I	Color difference signal input pin 6
108	DCI7	I	Color difference signal input pin 7 (MSB)
109	DYI0	I	Luminance signal input pin 0 (LSB)
110	DYI1	I	Luminance signal input pin 1
111	DYI2	I	Luminance signal input pin 2
112	DYI3	I	Luminance signal input pin 3
113	DYI4	I	Luminance signal input pin 4
114	DYI5	I	Luminance signal input pin 5
115	DYI6	I	Luminance signal input pin 6
116	DYI7	I	Luminance signal input pin 7 (MSB)
117	V_{SS}	I	GND
118	V_{DD}	I	Power supply
119	LSRB	O	Color difference signal discrimination signal output pin
120	N.C.	—	No connection

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
121	N.C.	—	No connection
122	L2HD	O	Double-speed horizontal pulse output pin (line lock)
123	LVD	O	Vertical pulse output pin (line lock)
124	LHD	O	Horizontal pulse output pin (line lock)
125	DCO0	O	Color difference signal output pin 0 (LSB)
126	DCO1	O	Color difference signal output pin 1
127	DCO2	O	Color difference signal output pin 2
128	DCO3	O	Color difference signal output pin 3
129	DCO4	O	Color difference signal output pin 4
130	DCO5	O	Color difference signal output pin 5
131	DCO6	O	Color difference signal output pin 6
132	DCO7	O	Color difference signal output pin 7 (MSB)
133	DYO0	O	Luminance signal output pin 0 (LSB)
134	DYO1	O	Luminance signal output pin 1
135	DYO2	O	Luminance signal output pin 2
136	DYO3	O	Luminance signal output pin 3
137	DYO4	O	Luminance signal output pin 4
138	DYO5	O	Luminance signal output pin 5
139	DYO6	O	Luminance signal output pin 6
140	DYO7	O	Luminance signal output pin 7 (MSB)
141	V_{DD}	I	Power supply
142	V_{SS}	I	GND
143	M3DO3	O	Data output pin for memory chip 3
144	M3DO2	O	Data output pin for memory chip 3
145	M3DO1	O	Data output pin for memory chip 3
146	M3DO0	O	Data output pin for memory chip 3
147	M3WR	O	Write reset output pin for memory chip 3
148	M3WE	O	Write enable output pin for memory chip 3
149	M3RE	O	Read enable output pin for memory chip 3
150	M3RR	O	Read reset output pin for memory chip 3
151	M3DI0	I	Data input pin for memory chip 3
152	M3DI1	I	Data input pin for memory chip 3
153	M3DI2	I	Data input pin for memory chip 3
154	M3DI3	I	Data input pin for memory chip 3
155	MIDO7	O	Data output pin for memory chip 1
156	MIDO6	O	Data output pin for memory chip 1
157	MIDO5	O	Data output pin for memory chip 1
158	MIDO4	O	Data output pin for memory chip 1
159	M1WR	O	Write reset output pin for memory chip 1
160	N.C.	—	No connection

■ Package Dimensions (Unit: mm)

QFP160-P-2828B