MN6761S

External Synchronization Control LSI for Color Video Cameras

■ Overview

The MN6761S is an external synchronization control LSI for color video cameras.

When used in combination with a synchronizing signal generator (MN67601NS or MN67602PS), it provides external synchronization control for NTSC and PAL video systems.

■ Features

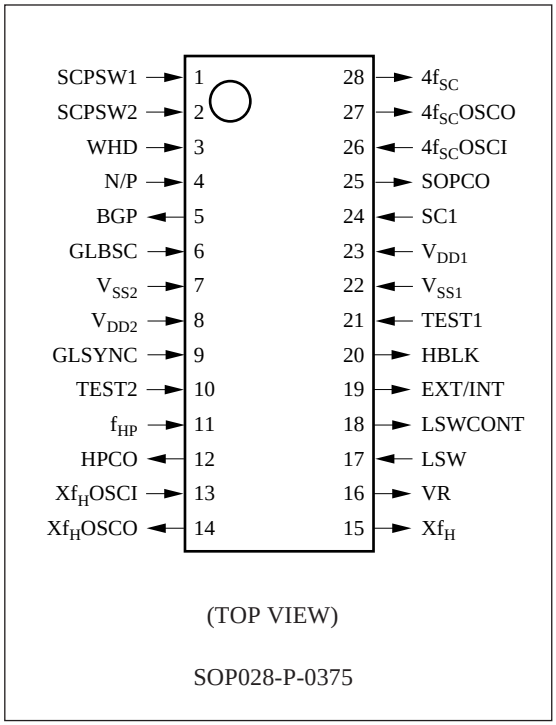
- Synchronization of both the video camera and the VCR
- External synchronization inputs:

  Composite synchronizing signal and burst subcarrier
- External synchronization techniques
  - Horizontal synchronization: phase-locked loop
  - Vertical synchronization: reset technique
  - Subcarrier synchronization: phase-locked loop
- Support for both NTSC and PAL systems
- Built-in feature for automatically switching between external and internal synchronization
- Built-in horizontal phase adjustment circuit

■ Applications

- Color video cameras

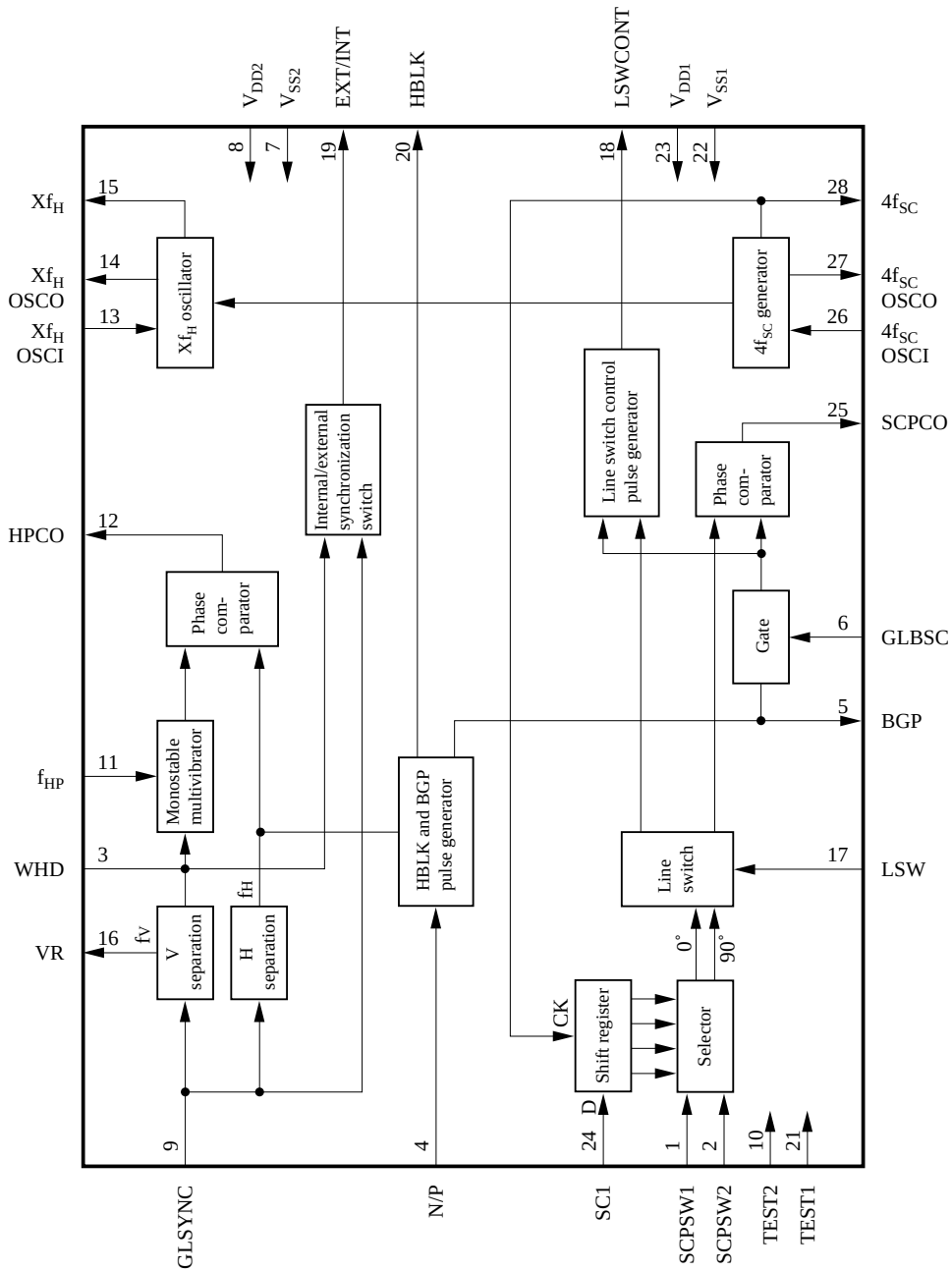
■ Pin Assignment



(TOP VIEW)

SOP028-P-0375

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Pin Name	Function Description
23	V_{DD1}	Power supply	"H" level (5V) power supply for subcarrier circuits
22	V_{SS1}	Power supply	"L" level (GND) power supply for subcarrier circuits
8	V_{DD2}	Power supply	"H" level (5V) power supply for synchronizing signal circuits
7	V_{SS2}	Power supply	"L" level (GND) power supply for synchronizing signal circuits
9	GLSYNC	External synchronizing signal input	Input pin for composite synchronizing signal derived from video signal (reference for horizontal and vertical signals)
6	CLBSC	External burst subcarrier input	Input pin for burst subcarrier signal derived from video signal (reference for subcarrier signals)
3	WHD	Horizontal synchronization input	Input pin for WHD signal from synchronizing signal generator
11	f_{HP}	Monostable multivibrator input	Pin for connecting CR circuit for adjusting delay for analog monostable multivibrator (thus adjusting horizontal phase)
24	SC1	Subcarrier input	Input pin for SC1 signal from synchronizing signal generator
1 2	SCPSW1 SCPSW2	Subcarrier phase switch inputs	Pin selecting which of the four phase signals generated from the SC1 signal goes to the phase comparator
17	LSW	Line switch input	For a PAL system, supply the LSW signal from the synchronizing signal generator. For an NTSC system, keep this pin at "H" level.
4	N/P	NTSC/PAL selection input	"H" level selects NTSC operation; "L" level, PAL operation.
12	HPCO	Horizontal phase comparator output	This pin is at "L" level when the WHD signal, after passing through the monostable multivibrator, leads the rising edge of the HSYNC signal derived by separating off the horizontal component of the GLSYNC signal and is at "H" level when the signal lags. At all other times, it is in the high-impedance state.
13	Xf_HOSCI	Oscillator input for the synchronization circuits	Clock oscillator pins for the synchronization circuits. Connect these pins to an inductor, capacitor, and variable capacitor. (The pins have built-in feedback resistors.)
14	Xf_HOSCO	Oscillator output for the synchronization circuits	The circuit oscillates during external synchronization mode. The oscillation stops for internal synchronization mode. The oscillator frequency, Xf_H is 14.31818 MHz ($910f_H$) for NTSC and 4.406 MHz ($282f_H$) for PAL.
15	Xf_H	Clock output for synchronizing signal circuits	Clock output pin for synchronizing signal circuits. This pin provides the clock (Xf_H) for the external synchronization mode and stays at "L" level for the internal synchronization mode. Connect to the $EX910f_HI$ pin of the synchronizing signal generator for NTSC operation and to the $EX282f_HI$ pin for PAL operation.

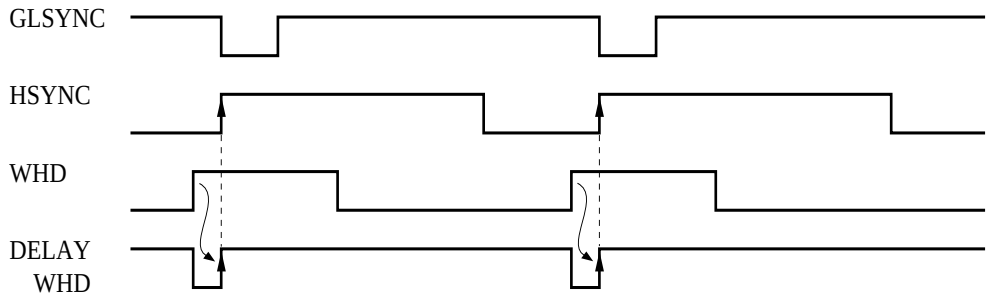
■ Pin Descriptions (continued)

Pin No.	Symbol	Pin Name	Function Description
16	VR	Vertical reset output	This pin generates a vertical reset pulse for the V-SERATION interval detected in the GLSYNC signal. Connect it to the VR pin of the synchronizing signal generator.
25	SCPCO	Subcarrier phase comparator output	This pin is at "L" level when the SC1 signal leads the GLBSC signal and is at "H" level when the signal lags. At all other times, it is in the high-impedance state.
26	$4f_{SC}$OSCI	Oscillator input for subcarrier circuits	Clock oscillator pins for the subcarrier circuits. Connect these pins to a crystal oscillator, capacitor, and variable capacitor. (The pins have built-in feedback resistors.) The circuit oscillates during external synchronization mode. The oscillation stops for internal synchronization mode. The oscillator frequency, $4f_{SC}$, is 14.31818 MHz for NTSC and 14.734 MHz for PAL.
27	$4f_{SC}$OSCO	Oscillator output for subcarrier circuits	
28	$4f_{SC}$	Subcarrier clock output	Clock output from subcarrier circuits. In external synchronization mode, this pin provides the ($4f_{SC}$) clock signal; in internal synchronization mode, it remains at "L" level. Connect this pin to the EX$4f_{SC}$I pin on the synchronizing signal generator.
18	LSWCONT	Line switch polarity control output	During PAL operation, this pin emits an error detection pulse if the LSW polarity is wrong, and the chip reverses the LSW polarity. During internal synchronization mode, this pin remains at "L" level. Connect this pin to the LSWCONT pin on the synchronizing signal generator.
19	EXT/INT	Automatic internal/ external switching output	If the chip detects GLSYNC input, it switches to external synchronization mode and drives this pin at "H" level. Otherwise, it switches to internal synchronization mode and drives this pin at "L" level. Connect this pin to the EXT/INT pin on the synchronizing signal generator.
5	BGP	Burst gate pulse output	These pulses have a width of 2.5 µs (NTSC) or 2.3 µs (PAL) and trail the rising edge of the HSYNC signal by 5.3 µs (NTSC) or 5.6 µs. They are generated for only 10 H to 256 H (NTSC) or 304 H (PAL) after the VR pulse.
20	HBLK	Horizontal blanking output	These pulses have a width of 8.9 µs (NTSC) or 8.8 µs (PAL) and follow the rising edge of the HSYNC signal.
21 10	TEST1 TEST2	Test inputs	Leave these test inputs open. (The pins include built-in pull-up resistors.)

■ Timing Chart

1. Horizontal synchronization block

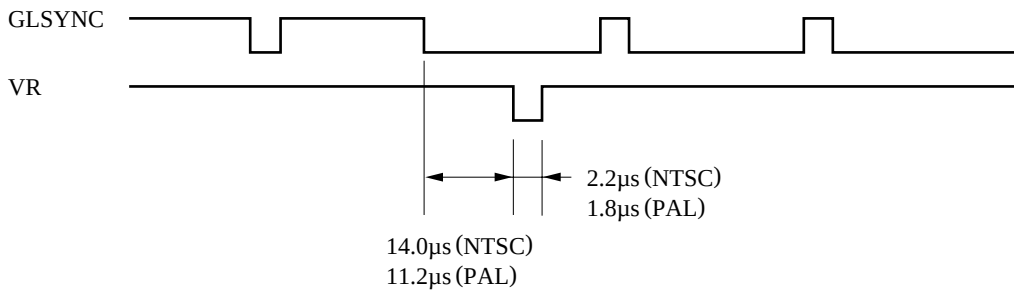
This block compares the phases of the HSYNC signal derived by separating off the horizontal component of the GLSYNC input and the WHD signal from the synchronizing signal generator after it has passed through the monostable multivibrator. It is thus possible to adjust the horizontal phase by adjusting the CR integral circuit's time constant.



Timing chart for horizontal pulse phase comparison

2. Vertical synchronization block

This block detects the V-SERATION interval in the GLSYNC input and generates a vertical reset (VR) pulse with 0.5 H of the start of that interval. It then issues no pulses for 256 H (NTSC) or 304 H (PAL) after this VR pulse.



Vertical reset pulse timing chart

3. Subcarrier synchronization block

This block converts the SC1 output from the synchronizing signal generator into four signals with the same frequency as the burst subcarrier, but different phases. In this phase-locked loop circuit, the phase of GLBSC is compared with the phase selected by 2 bits (SCPSW1 and SCPSW2).

During PAL operation, if the LSW polarity is wrong, this block sends an error detection pulse (LSWCONT) to the synchronizing signal generator and reverses the LSW polarity. It also adjusts the relationship between fields 1 through 4.

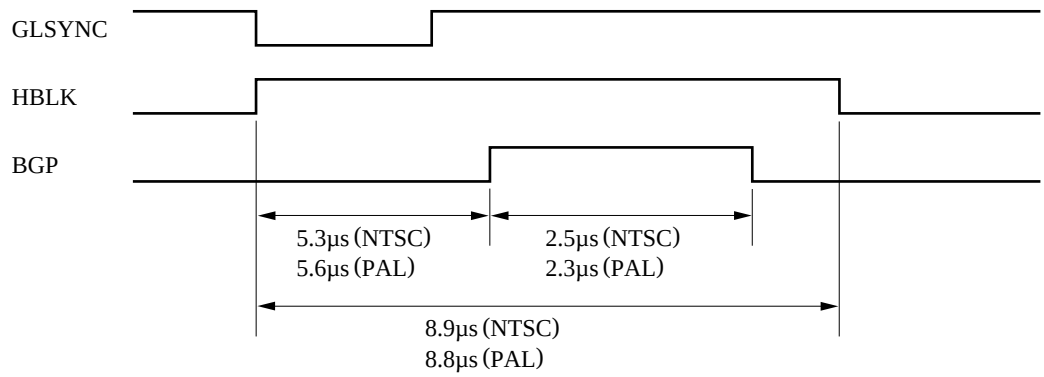
4. Oscillator blocks

The Xf_H and $4f_{SC}$ oscillator blocks operate only during external synchronization mode. Connecting a variable capacitor creates voltage-controlled oscillators that generate the synchronization signal circuit clock (Xf_H) and subcarrier circuit clock ($4f_{SC}$) for output to the synchronization signal generator.

5. Automatic internal/external switching block

If it detects a minimum of ten edges from the GLSYNC input, this block switches the chip to the external synchronization mode and drives the EXT/INT pin at "H" level. If there are no edges in the GLSYNC input for 10 H, this block switches the chip to the internal synchronization mode and drives this pin at "L" level.

HBLK and BGP plus generator



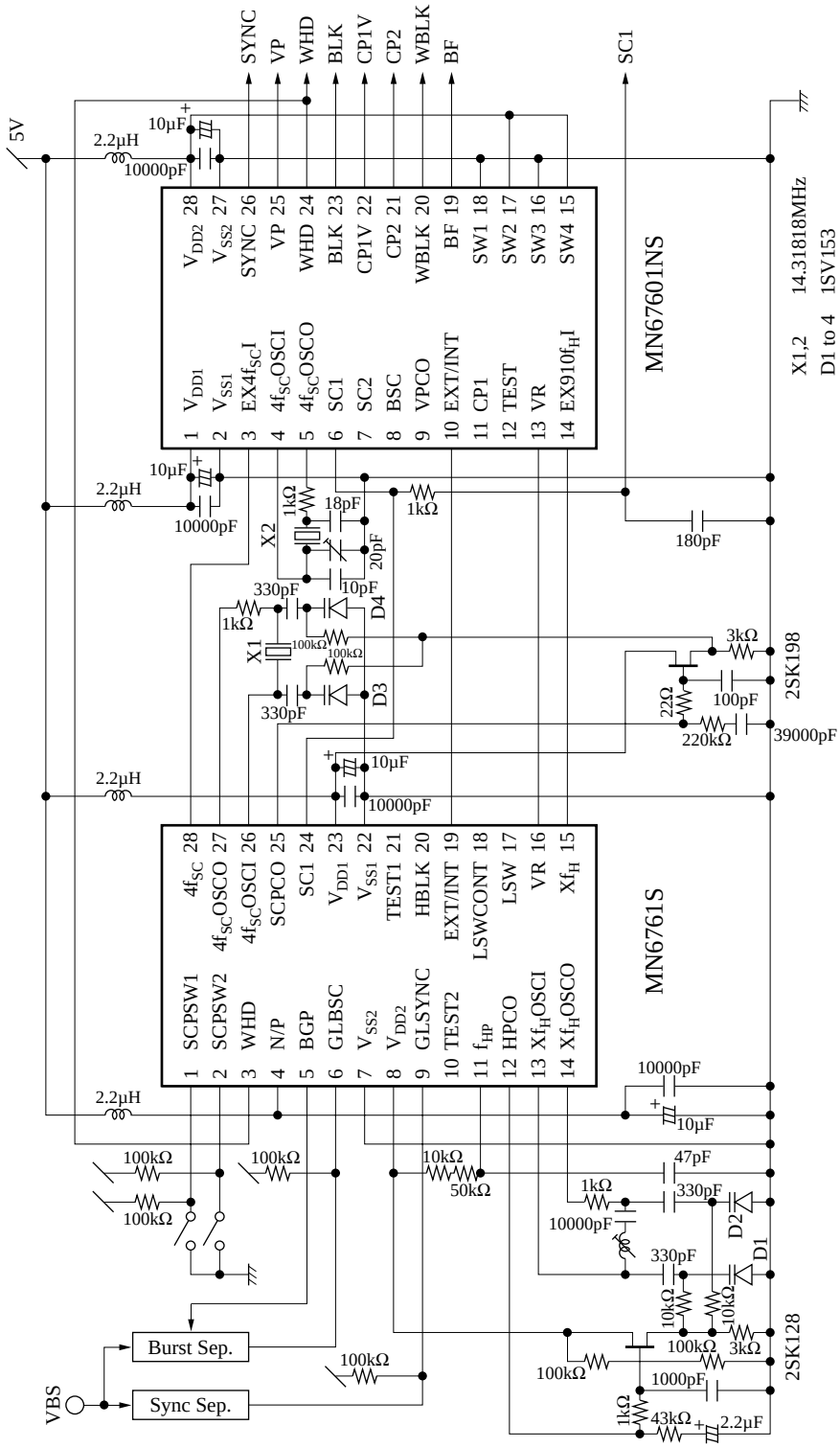
HBLK and BGP pulse timing chart

There is an HBLK pulse for each H.

BGP pulses are generated for only 10 H to 256 H (NTSC) or 304 H (PAL) after the VR pulse.

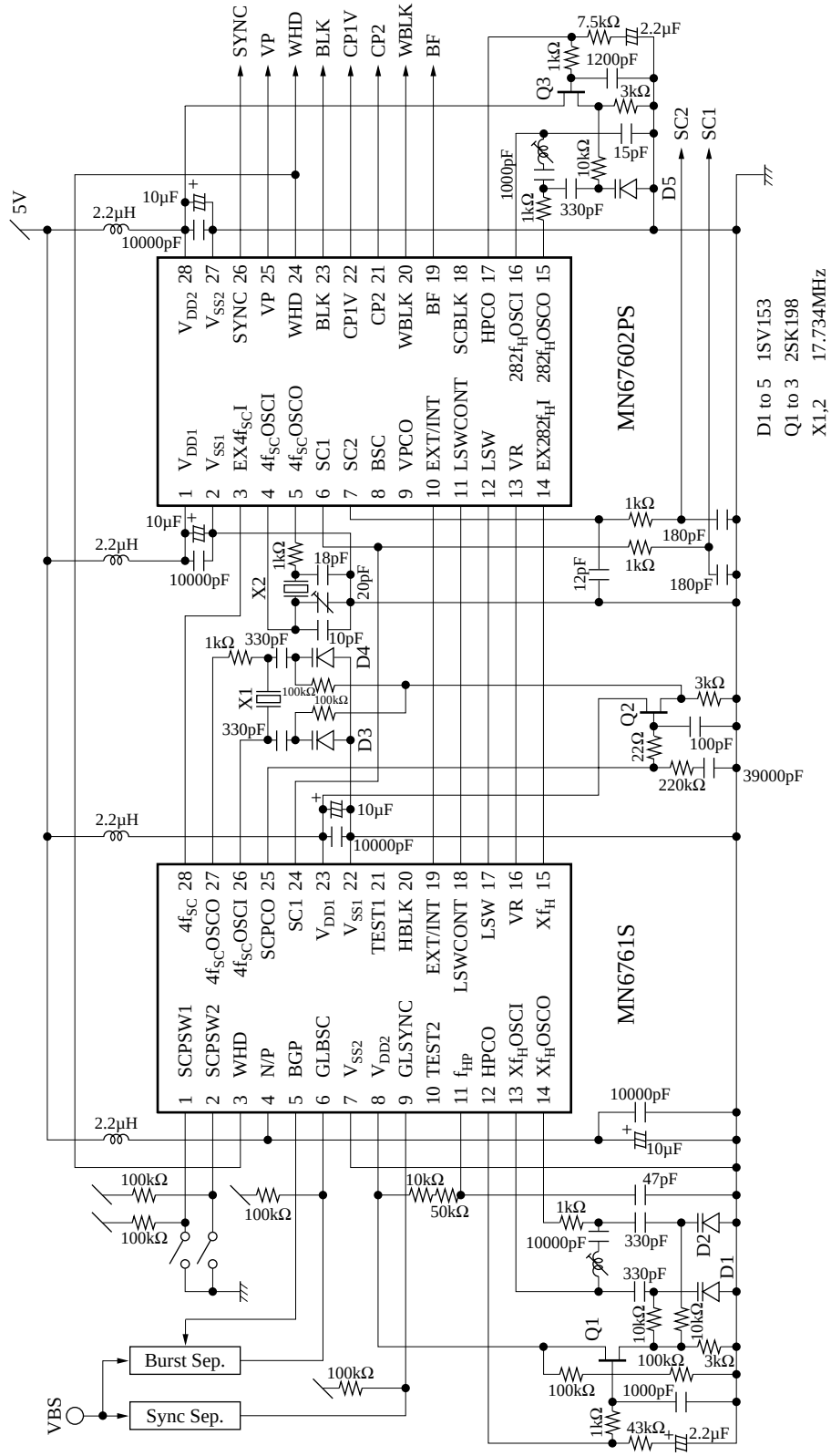
■ Application Circuit Example

1. External synchronization for NTSC system



■ Application Circuit Example

2. External synchronization for PAL system



■ Package Dimensions (Unit: mm)

SOP028-P-0375