MN65771F

Low Power 10-Bit 5 V CMOS A/D Converter for Image Processing

■ Overview

The MN65771F is a high-speed 10-bit CMOS analog-to-digital converter for image processing applications.

It uses a half flash structure based on chopper comparators to achieve both high speed and low power consumption.

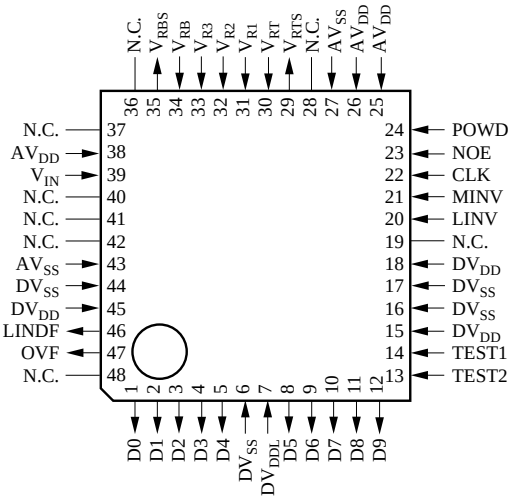
■ Features

- Maximum conversion rate: 18 MSPS (min.)
- Linearity error: ±1.3 LSB (typ.)
- Differential linearity error: ±1.0 LSB (typ.)
- Power supply voltage: 5.0 V or 3.3 V
- Power consumption: 115 mW (typ.) (f_{CLK}=20 MHz)

■ Applications

- Digital television receivers
- Digital video equipment
- Digital image processing equipment

■ Pin Assignment

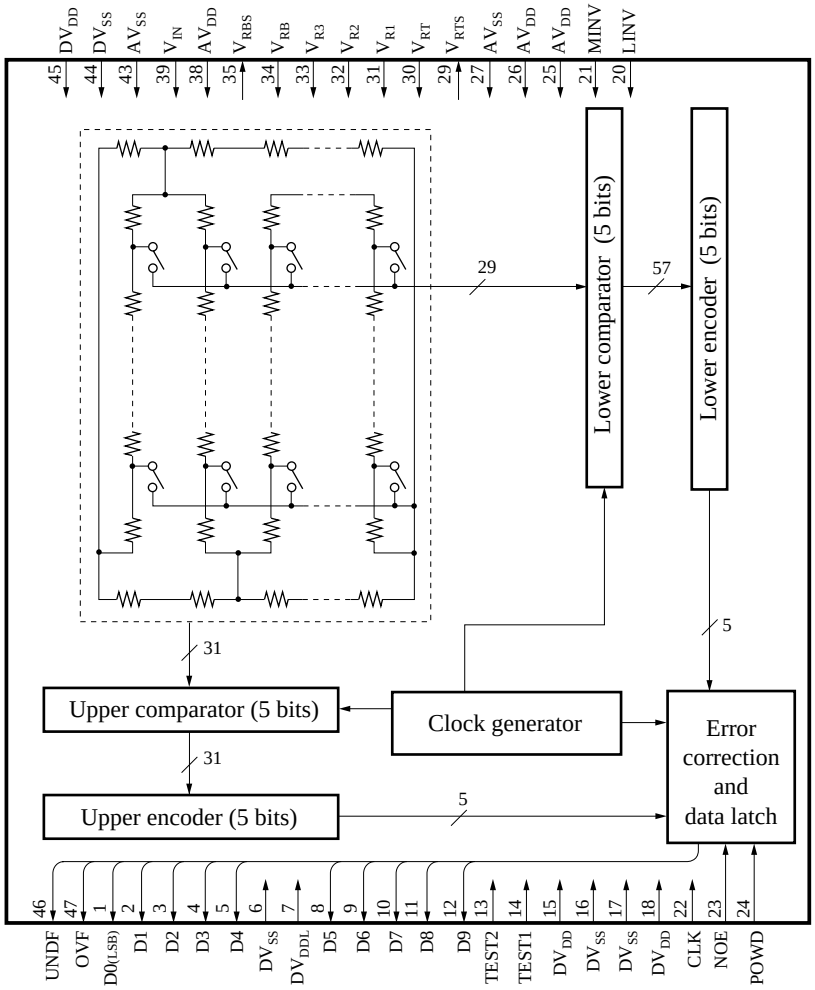


(TOP VIEW)

QFH048-P-0707

■ Block Diagram

Pin NO.
(19, 28, 36, 37,
40, 41, 42, 48 are N.C.pin.)



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	D0	Digital code output (LSB)
2	D1	Digital code output
3	D2	Digital code output
4	D3	Digital code output
5	D4	Digital code output
6	DV_{SS}	Ground for digital circuits
7	DV_{DDL}	Power supply for digital circuits
8	D5	Digital code output
9	D6	Digital code output
10	D7	Digital code output
11	D8	Digital code output
12	D9	Digital code output
13	TEST2	Test mode selection
14	TEST1	Test mode selection
15	DV_{DD}	Power supply for digital circuits
16	DV_{SS}	Ground for digital circuits
17	DV_{SS}	Ground for digital circuits
18	DV_{DD}	Power supply for digital circuits
19	N.C.	No connection
20	LINV	Output inversion
21	MINV	Output inversion
22	CLK	Sampling clock
23	NOE	Digital output enable
24	POWD	Power down mode selection
25	AV_{DD}	Power supply for analog circuits
26	AV_{DD}	Power supply for analog circuits
27	AV_{SS}	Ground for analog circuits
28	N.C.	No connection
29	V_{RTS}	Reference voltage power supply (TOP)
30	V_{RT}	Reference voltage input (TOP)
31	V_{R1}	Intermediate reference voltage
32	V_{R2}	Intermediate reference voltage
33	V_{R3}	Intermediate reference voltage
34	V_{RB}	Reference voltage input (BOTTOM)
35	V_{RBS}	Reference voltage power supply (BOTTOM)
36	N.C.	No connection
37	N.C.	No connection
38	AV_{DD}	Power supply for analog circuits
39	V_{IN}	Analog signal input
40	N.C.	No connection

■ Pin Descriptions (continued)

Pin No.	Symbol	Function Description
41	N.C.	No connection
42	N.C.	No connection
43	AV_{SS}	Ground for analog circuits
44	DV_{SS}	Ground for digital circuits
45	DV_{DD}	Power supply for digital circuits
46	UNDF	Underflow output
47	OVF	Overflow output
48	N.C.	No connection

■ Absolute Maximum Ratings Ta=25˚C

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +7.0	V
Input voltage	V_I	– 0.3 to V_{DD} +0.3	V
Output voltage	V_O	– 0.3 to V_{DD} +0.3	V
Operating ambient temperature	T_{opr}	–20 to +70	˚C
Storage temperature	T_{stg}	–55 to +125	˚C

■ Recommended Operating Conditions $V_{DD}=AV_{DD}=DV_{DD}=5.0V$, $DV_{DDL}=3.3V$, $V_{SS}=AV_{SS}=DV_{SS}=0V$, Ta=25˚C

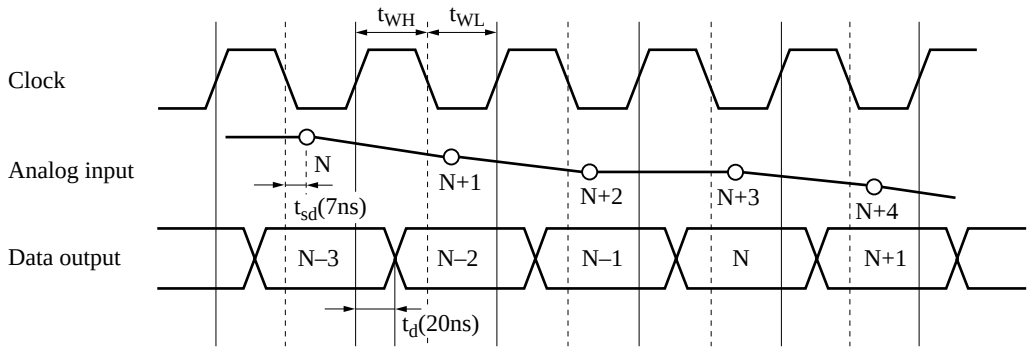
Parameter		Symbol	min	typ	max	Unit
Power supply voltage		V_{DD}	4.50	5.00	5.50	V
Power supply voltage for digital output circuits		DV_{DDL}	3.00	3.30	5.50	V
Digital input voltage	"H" level	V_{IH}	2.4		V_{DD}	V
	"L" level	V_{IL}	V_{SS}		0.8	V
Reference voltage	"H" level	V_{RT}		4.0		V
	"L" level	V_{RB}		2.0		V
Clock	"H" level pulse width	t_{WH}	25			ns
	"L" level pulse width	t_{WL}	25			ns
Analog input voltage		V_{AIN}	V_{SS}		V_{DD}	V

■ Electrical Characteristics $V_{DD}=AV_{DD}=DV_{DD}=3.0V$, $AV_{SS}=DV_{SS}=0V$, Ta=25˚C

Parameter		Symbol	Conditions	min	typ	max	Unit
Power consumption		P_C	F_C=20MSPS (not including reference current)		115	200	mW
Resolution		RES			10		bit
Linearity error		E_L	f_{CLK}=18MSPS		±1.3	±2.5	LSB
Differential linearity error		E_D	V_{RT}=4.0V V_{BB}=2.0V		±1.0	±1.5	LSB
Maximum conversion rate		$F_{C(max.)}$		18			MSPS
Clock frequency		f_{CLK}		1		18	MHz
Analog input dynamic range		D_R		2		$V_{RT} - V_{RB}$	V
Output current	"H" level	I_{OH}	$V_{OH}=V_{DD}-0.8V$			–1.5	mA
	"L" level	I_{OL}	V_{OL}=0.4V	1.5			mA
Output delay time		t_d	C_L=20pF	10	20	30	ns
Analog input capacitance		C_I			15		pF
Sampling delay		t_{sd}			7		ns

■ Timing Chart

The chip samples the analog input at the falling edge of the clock signal and provides the corresponding digital output 2.5 clock cycles later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

QFH048-P-0707