MN65752H

Low Power 8-Bit, 2-Channel CMOS A/D Converter for Image Processing

■ Overview

The MN65752H is an 8-bit, 2-channel CMOS analog-to-digital converter for image processing applications.

It uses a half flash structure based on chopper comparators and achieves both high speed and low power consumption with multiplexing.

It provides separate power supply pins for the circuits driving the low-voltage digital output pins.

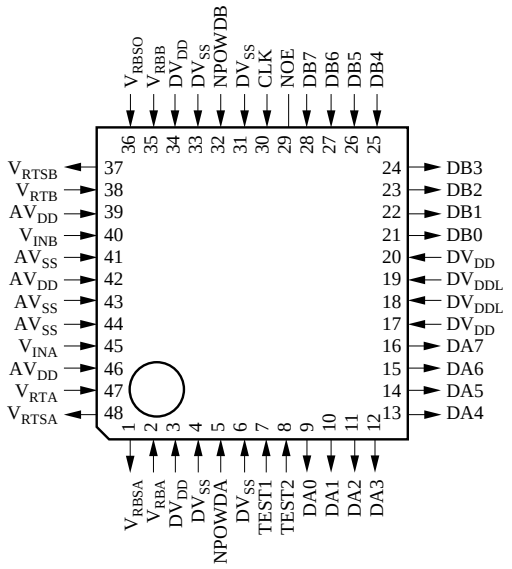
■ Features

- Maximum conversion rate: 20 MSPS (min.)
- Linearity error: ±0.9 LSB (typ.)
- Differential linearity error: ±0.5 LSB (typ.)
- Power supply voltage: 3.6 V or 2.6 V
- Power consumption: 50 mW (typ.) (f_{CLK}=16 MHz)

■ Applications

- Digital television receivers
- Digital video equipment
- Digital image processing equipment

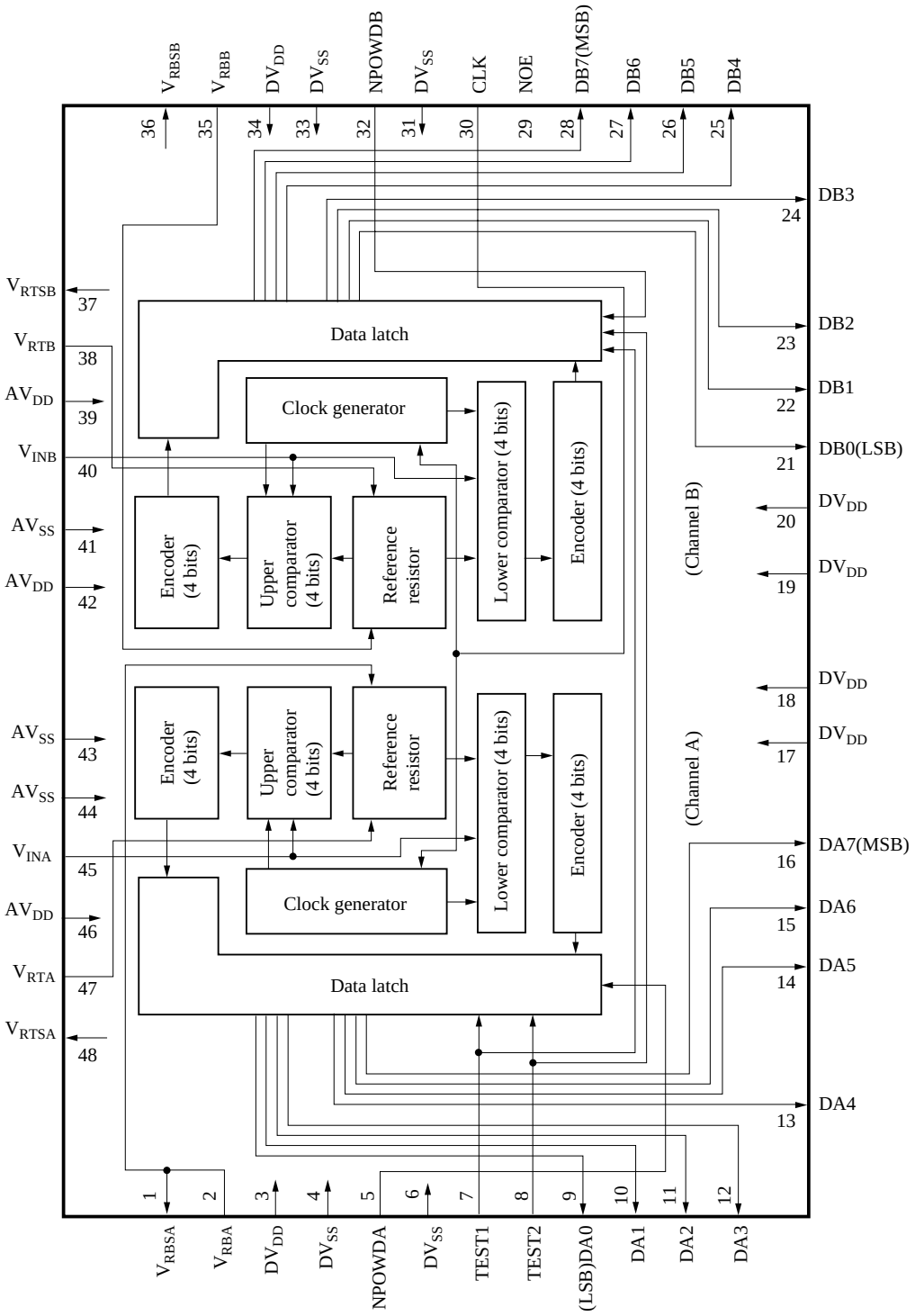
■ Pin Assignment



(TOP VIEW)

QFH048-P-0707

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	V_{RBSA}	Reference voltage power supply (BOTTOM)
2	V_{RBA}	Reference voltage input (BOTTOM)
3	DV_{DD}	Power supply for digital circuits
4	DV_{SS}	Ground for digital circuits
5	NPOWDA	Power down mode selection
6	DV_{SS}	Ground for digital circuits
7	TEST1	Test mode selection
8	TEST2	Test mode selection
9	DA0	Digital code output (LSB)
10	DA1	Digital code output
11	DA2	Digital code output
12	DA3	Digital code output
13	DA4	Digital code output
14	DA5	Digital code output
15	DA6	Digital code output
16	DA7	Digital code output (MSB)
17	DV_{DD}	Power supply for digital circuits
18	DV_{DDL}	Power supply for low-voltage digital outputs
19	DV_{DDL}	Power supply for low-voltage digital outputs
20	DV_{DD}	Power supply for digital circuits
21	DB0	Digital code output (LSB)
22	DB1	Digital code output
23	DB2	Digital code output
24	DB3	Digital code output
25	DB4	Digital code output
26	DB5	Digital code output
27	DB6	Digital code output
28	DB7	Digital code output (MSB)
29	NOE	Digital output enable
30	CLK	Sampling clock
31	DV_{SS}	Ground for digital circuits
32	NPOWDB	Power down mode selection
33	DV_{SS}	Ground for digital circuits
34	DV_{DD}	Power supply for digital circuits
35	V_{RBB}	Reference voltage input (BOTTOM)
36	V_{RBSB}	Reference voltage power supply (BOTTOM)
37	V_{RTSB}	Reference voltage power supply (TOP)
38	V_{RTB}	Reference voltage input (TOP)
39	AV_{DD}	Power supply for analog circuits
40	V_{INB}	Ground for analog circuits

■ Pin Descriptions (continued)

Pin No.	Symbol	Function Description
41	AV_{SS}	Ground for analog circuits
42	AV_{DD}	Power supply for analog circuits
43	AV_{SS}	Ground for analog circuits
44	AV_{SS}	Ground for analog circuits
45	V_{INA}	Analog signal input
46	AV_{DD}	Power supply for analog circuits
47	V_{RTA}	Reference voltage input (TOP)
48	V_{RTSA}	Reference voltage power supply (TOP)

■ Absolute Maximum Ratings Ta=25˚C

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +7.0	V
Power supply voltage for digital output circuits	DV_{DDL}	– 0.3 to V_{DD}+0.3	V
Input voltage	V_I	– 0.3 to V_{DD}+0.3	V
Output voltage	V_O	– 0.3 to V_{DD}+0.3	V
Operating ambient temperature	T_{opr}	–20 to +70	˚C
Storage temperature	T_{stg}	–55 to +125	˚C

■ Recommended Operating Conditions $V_{DD}=AV_{DD}=DV_{DD}=3.6V$, $DV_{DDL}=2..6V$, $V_{SS}=AV_{SS}=DV_{SS}=0V$, Ta=25˚C

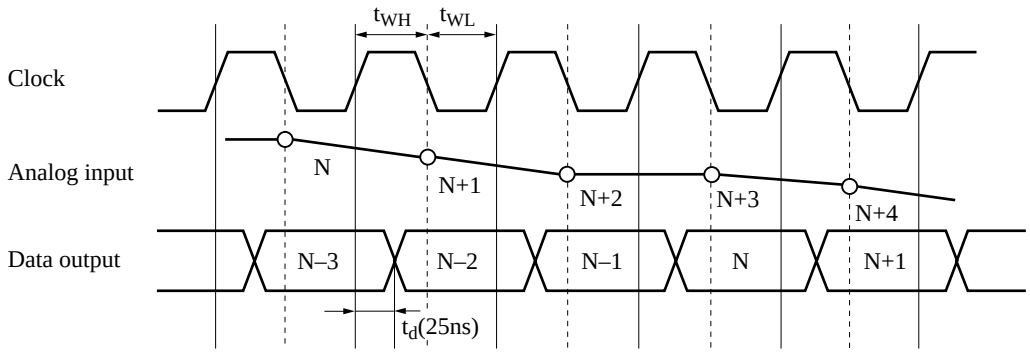
Parameter		Symbol	min	typ	max	Unit
Power supply voltage		V_{DD}	3.30	3.60	5.25	V
Power supply voltage for digital output circuits		DV_{DDL}	2.50	2.60	5.25	V
Digital input voltage	"H" level	V_{IH}	$V_{DD}\times 0.55$		V_{DD}	V
	"L" level	V_{IL}	V_{SS}		$V_{DD}\times 0.2$	V
Reference voltage	"H" level	V_{RT}		2.80	V_{DD}	V
	"L" level	V_{RB}	V_{SS}	1.30		V
Clock	"H" level pulse width	t_{WH}	20			ns
	"L" level pulse width	t_{WL}	20			ns
Analog input voltage		V_{AIN}	V_{SS}		V_{DD}	V

■ Electrical Characteristics $V_{DD}=AV_{DD}=DV_{DD}=3.6V$, $DV_{DDL}=2.6V$, $AV_{SS}=DV_{SS}=0V$, Ta=25˚C

Parameter		Symbol	Conditions	min	typ	max	Unit
Power consumption		P_C	f_{CLK}= 16 MSPS (not including reference current)		50	90	mW
Resolution		RES			8		bit
Linearity error		E_L	f_{CLK}=20MSPS		±0.9	±1.8	LSB
Differential linearity error		E_D	V_{RT}=2.8V, V_{RB}=1.3V		±0.5	±1.0	LSB
Maximum conversion rate		$F_{C(max.)}$		20			MSPS
Clock frequency		f_{CLK}		1		20	MHz
Analog input dynamic range		D_R		1.5		$V_{RT}-V_{RB}$	V
Output current	"H" level	I_{OH}	$V_{OH}=DV_{DDL}-0.8V$			–1.5	mA
	"L" level	I_{OL}	V_{OL}=0.4V	1.5			mA
Output delay time		t_d	C_L=20pF	10	25	40	ns
Analog input capacitance		C_I			15		pF

■ Timing Chart

The chip samples the analog input at the falling edge of the clock signal and provides the corresponding digital output 2.5 clock cycles later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

QFH048-P-0707