MN655431SH

Low Power 8-Bit CMOS A/D Converter for Image Processing

■ Overview

The MN655431SH is an 8-bit CMOS analog-to-digital converter with a maximum conversion rate of 15 MSPS.

It uses a half flash structure based on chopper comparators and achieves both high speed and low power consumption with multiplex processing.

It provides separate power supply pins for the circuits driving the low-voltage digital output pins.

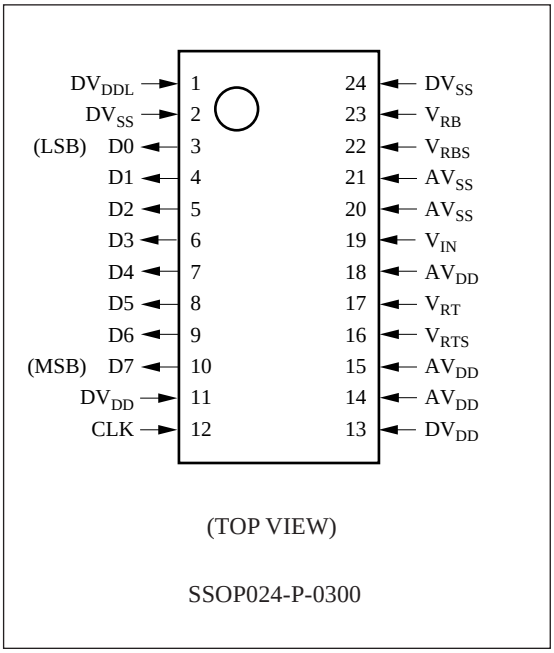
■ Features

- Maximum conversion rate: 15 MSPS (min.)
- Linearity error: ±0.5 LSB (typ.)
- Differential linearity error: ±0.4 LSB (typ.)
- Power supply voltage: 4.40 to 5.25 V
- Power consumption: 90 mW (typ.)

■ Applications

- Digital television receivers
- Digital video equipment
- Digital image processing equipment

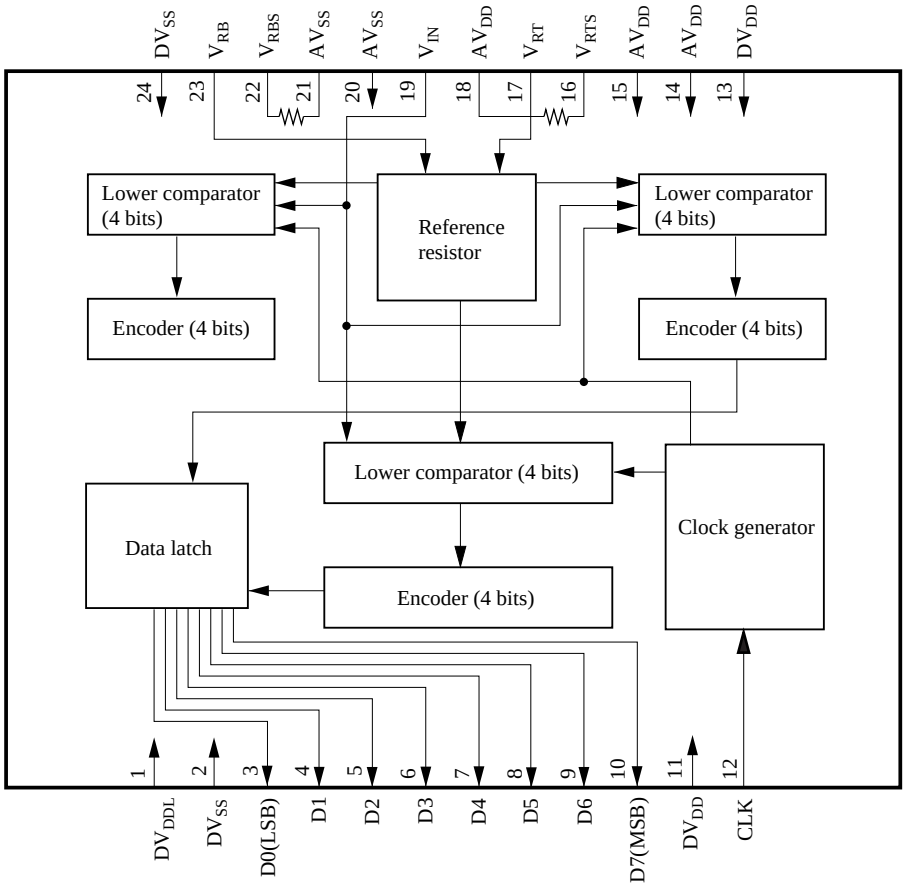
■ Pin Assignment



(TOP VIEW)

SSOP024-P-0300

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	DV_{DDL}	Power supply for digital output circuits
2	DV_{SS}	Ground for digital circuits
3	D0	Digital output (LSB)
4	D1	Digital output
5	D2	Digital output
6	D3	Digital output
7	D4	Digital output
8	D5	Digital output
9	D6	Digital output
10	D7	Digital output (MSB)
11	DV_{DD}	Power supply for digital circuits
12	CLK	Sampling clock
13	DV_{DD}	Power supply for digital circuits
14	AV_{DD}	Power supply for analog circuits
15	AV_{DD}	Power supply for analog circuits
16	V_{RTS}	Power supply for reference voltage (TOP)
17	V_{RT}	Reference voltage (TOP)
18	AV_{DD}	Power supply for analog circuits
19	V_{IN}	Analog input
20	AV_{SS}	Ground for analog circuits
21	AV_{SS}	Ground for analog circuits
22	V_{RBS}	Power supply for reference voltage (BOTTOM)
23	V_{RB}	Reference voltage (BOTTOM)
24	DV_{SS}	Ground for digital circuits

■ Absolute Maximum Ratings Ta=25˚C

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +7.0	V
Power supply voltage for digital outputs	DV_{DDL}	– 0.3 to $+V_{DD}$ +0.3	V
Input voltage	V_I	AV_{SS} – 0.3 to V_{DD} +0.3	V
Output voltage	V_O	DV_{SS} – 0.3 to V_{DD} +0.3	V
Operating ambient temperature	T_{opr}	–20 to +70	˚C
Storage temperature	T_{stg}	–55 to +125	˚C

■ Recommended Operating Conditions

V_{DD}=AV_{DD}=DV_{DD}=5.0V, DV_{DDL}=3.5V, V_{SS}=AV_{SS}=DV_{SS}=0V, Ta=25˚C

Parameter		Symbol	min	typ	max	Unit
Power supply voltage		V_{DD}	4.50	5.00	5.25	V
Power supply voltage for digital outputs		DV_{DDL}	3.4		3.6	V
Digital input voltage	"H" level	V_{IH}	2.4		V_{DD}	V
	"L" level	V_{IL}	V_{SS}		0.8	V
Reference voltage	"H" level	V_{RT}	3.3		V_{DD}	V
	"L" level	V_{RB}	V_{SS}		1.5	V
Clock	"H" level pulse width	t_{WH}	30			ns
	"L" level pulse width	t_{WL}	30			ns
Analog input voltage		V_{AIN}	V_{SS}		V_{DD}	V

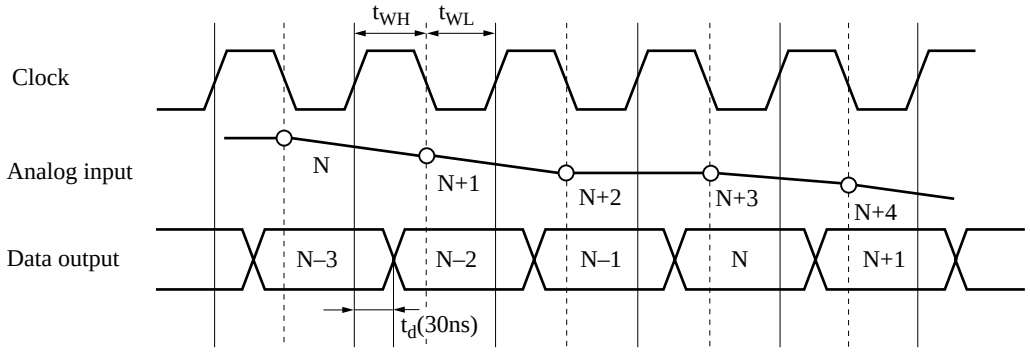
■ Electrical Characteristics

V_{DD}=AV_{DD}=DV_{DD}=5.0V, DV_{DDL}=3.5V, AV_{SS}=DV_{SS}=0V, Ta=25˚C

Parameter		Symbol	Conditions	min	typ	max	Unit
Power supply voltage		I_{DD}	f_{CLK} = 15 MHz (includes reference power supply)		18	26	mA
Resolution		RES			8		bit
Linearity error		E_L	f_{CLK}=15MHz		±0.5	±1.3	LSB
Differential linearity error		E_D	V_{RT}=3.5V V_{RB}=1.5V		±0.4	±0.7	LSB
Maximum conversion rate		$F_{c(max.)}$		15			MSPS
Clock frequency		f_{CLK}		1		15	MHz
Analog input dynamic range		D_R		2		V_{RT}–V_{RB}	V
Output current	"H" level	I_{OH}	V_{OH}=DV_{DDL} – 0.8V			–2	mA
	"L" level	I_{OL}	V_{OL}= 0.4V	2			mA
Output delay time		t_d			30	45	ns
Analog input capacitance		C_I			18		pF

■ Timing Chart

The chip samples the analog input at the falling edge of the clock signal and provides the corresponding digital output 2.5 clock cycles later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

SSOP024-P-0300