MN6479A

D/A Converter for Digital Audio Equipment

■ Overview

The MN6479A is a CMOS digital-to-analog converter by noise shaping technology and is designed for PCM digital audio equipment. It features a built-in 8 times oversampling and 16-bit input digital filter.

It includes a digital de-emphasis circuit and analog post filter to reduce the parts count and power consumption of the overall D/A conversion system.

And also, it includes two noise-shaping 1-bit D/A converters, one each for the left and right channels.

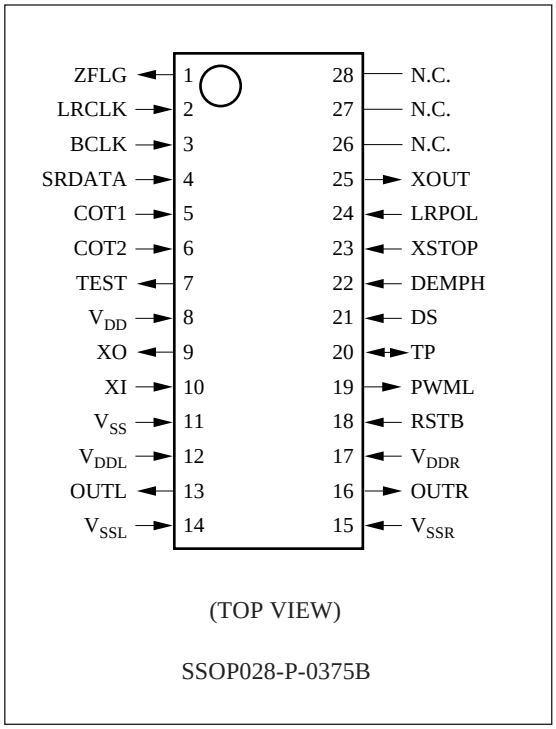
■ Features

- Built-in 8 times oversampling digital filter
- Built-in 2nd order analog post filter with a cutoff frequency of 100 kHz
- Built-in digital de-emphasis circuit with a deviation between +0.47 dB and – 0.07 dB
- Choice of normal or double-speed playback
- Mode for suspending oscillator operation
- No zero cross distortion
- Output pin for detecting zero input
- $384f_s$ operation
- Single 5 volt power supply

■ Applications

- CD players and other digital audio equipment

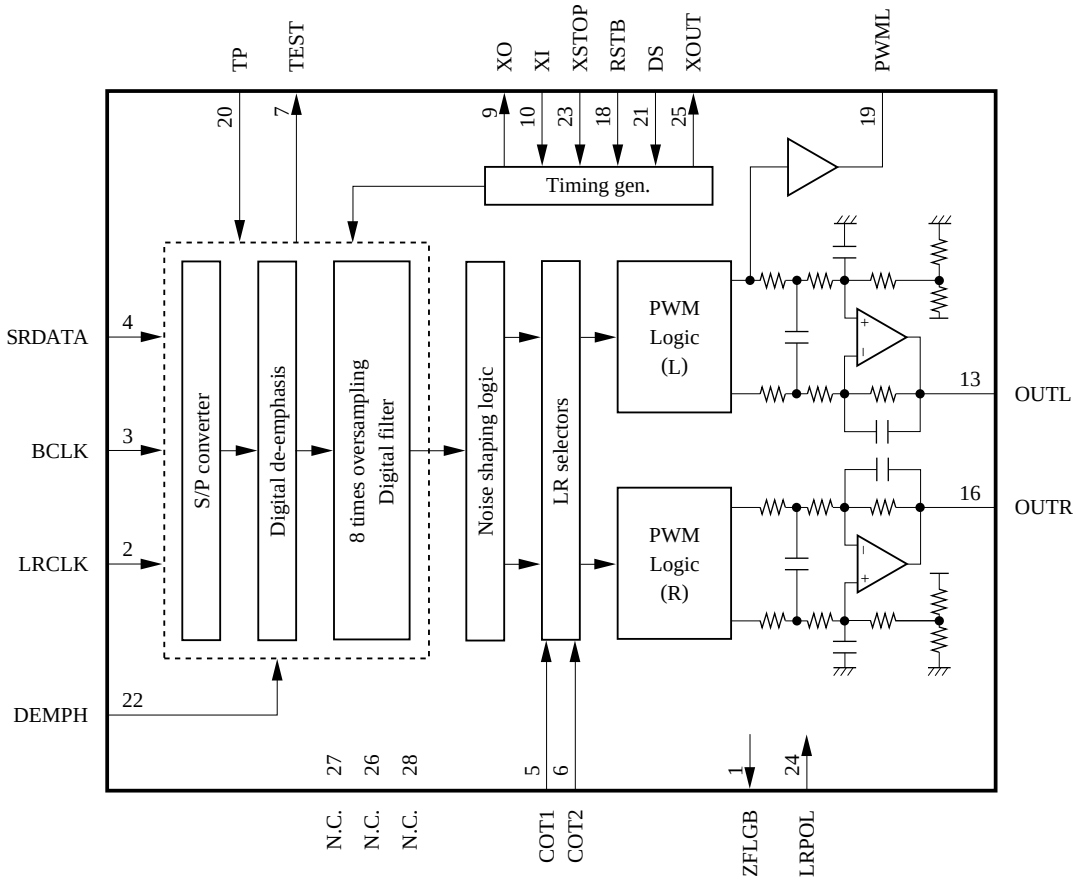
■ Pin Assignment



(TOP VIEW)

SSOP028-P-0375B

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	ZFLG	Zero input detection output pin
2	LRCLK	LRCLK input pin
3	BCLK	Bit clock input pin for serial data
4	SRDATA	Serial data input pin
4	COT 1	L: Stereo output; L: Left channel output only; H: Right channel output only; H: Output with channels reversed
5	COT2	L: Stereo output; H: Left channel output only; L: Right channel output only; H: Output with channels reversed
7	TEST	LSI test mode selection pin. Keep this pin at "L" level.
8	V_{DD}	Power supply pin for digital circuits (+5V)
9	XO	Crystal oscillator pin
10	XI	Crystal oscillator pin (external clock input pin)
11	V_{SS}	Ground pin for digital circuits (0V)
12	V_{DDL}	Power supply pin for left channel analog circuits (+5V)
13	OUTL	Left channel analog signal output pin
14	V_{SSL}	Ground pin for left channel analog circuits (0V)
15	V_{SSR}	Ground pin for right channel analog circuits (0V)
16	OUTR	Right channel analog signal output pin
17	V_{DDR}	Power supply pin for left channel analog circuits (+5V)
18	RSTB	Reset input pin (Active low)
19	PWML	LSI test output pin. Leave this pin open.
20	TP	LSI test I/O pin. Keep this pin at "L" level.
21	DS	Double-speed selection pin
22	DEMPH	De-emphasis ON/OFF pin. ON at "H" level.
23	XSTOP	Clock oscillation stop set pin. "H" level; stop mode
24	LRPOL	LRCLK polarity selection pin
25	XOUT	$384f_s$ output pin. Maximum load capacity: 30 pF.
26	N.C.	Connect to "H" or "L" level or leave open.
27	N.C.	Connect to "H" or "L" level or leave open.
28	N.C.	Connect to "H" or "L" level or leave open.

■ Conversion Characteristics

V_{DD} =5.00V, V_{SS} =0V, V_{DDL}, V_{DDR}=5.00V, V_{SSL}, V_{SSR} =0V, f=16.9344MHz, Ta=0˚C to 70˚C

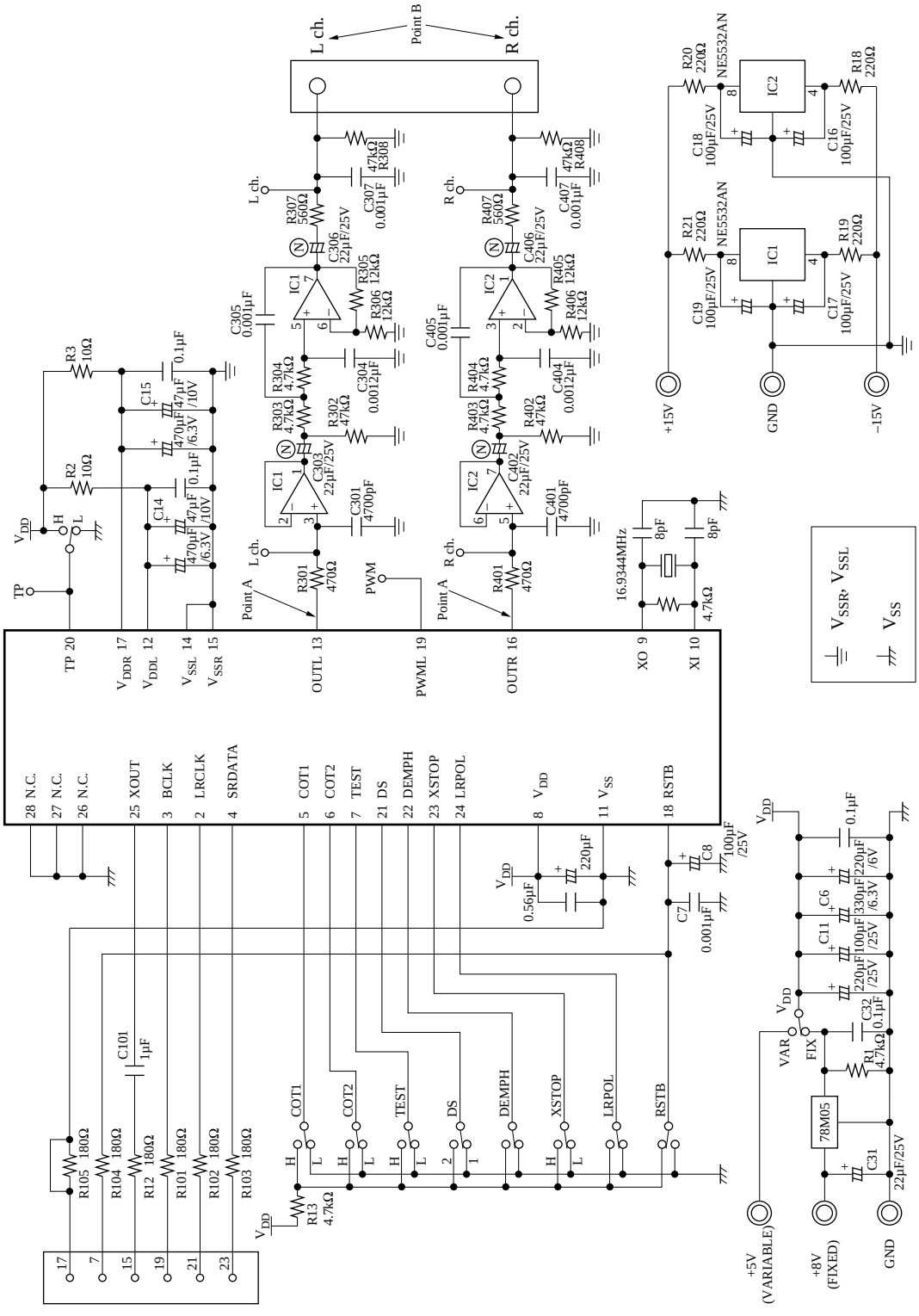
Parameter	Symbol	Test Conditions	min	typ	max	Unit
Signal-to-noise ratio	S/N	EIAJ	96	102		dB
Dynamic range	D.R.	EIAJ	90	97		dB
Total harmonic distortion ratio	THD + N	EIAJ		0.003	0.007	%
Crosstalk		EIAJ	90	98		dB
Output level 1 *1		1kHz F.S.		1.2		V_{rms}
Output level 2 *2		1kHz F.S.	2.0	2.3	2.6	V_{rms}

Notes

*1: This level is measured at point A (LSI output pin) in the application circuit example next page.

*2: This level is measured at point B in the same circuit.

■ Application Circuit Example



■ Package Dimensions (Unit: mm)

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