MN6463

A/D Converter for Digital Audio Equipment

■ Overview

The MN6463 is a 2-channel, 16-bit analog-to-digital converter for pulse code modulation (PCM) digital audio equipment. It has a built-in digital filter and employs noise shaping technology. Addition of this digital filter permits simplification of the pre-analog-filter of the A/D converter, thus opening the door to compact designs for MD, DAT, and other digital audiovisual equipment.

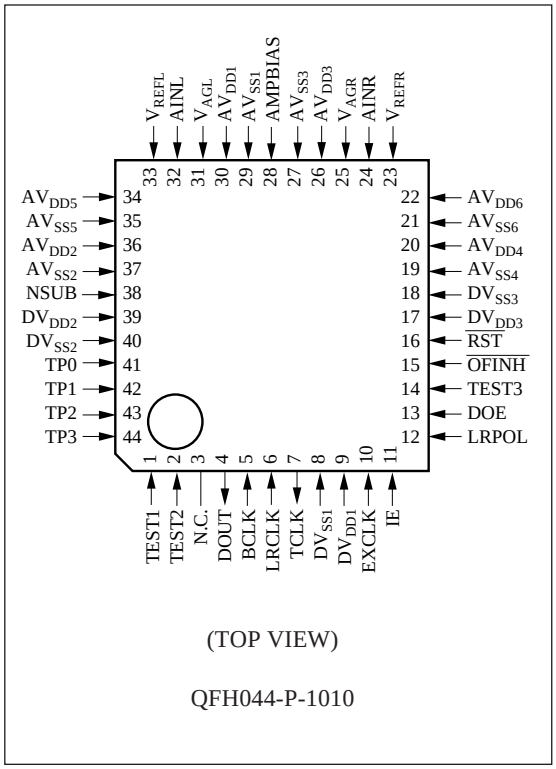
■ Features

- Operates on a single 5-V power supply (Also requires V_{REFL}=V_{REFR}=1.0V and V_{AGL}=V_{AGR}=2.5V)
- CMOS LSI mixed analog and digital circuits
- A/D converter of noise shaping technology with 64-fold oversampling
- Switchable between signal processing LSI format and I²S format and two's complement output
- System clock of 256 f_s
- Sample and hold circuit is unnecessary
- Built-in offset correction circuit
- Built-in overflow limiter
- Tristate output pins

■ Applications

- MD, DAT, electronic musical instruments, and other digital audio equipment

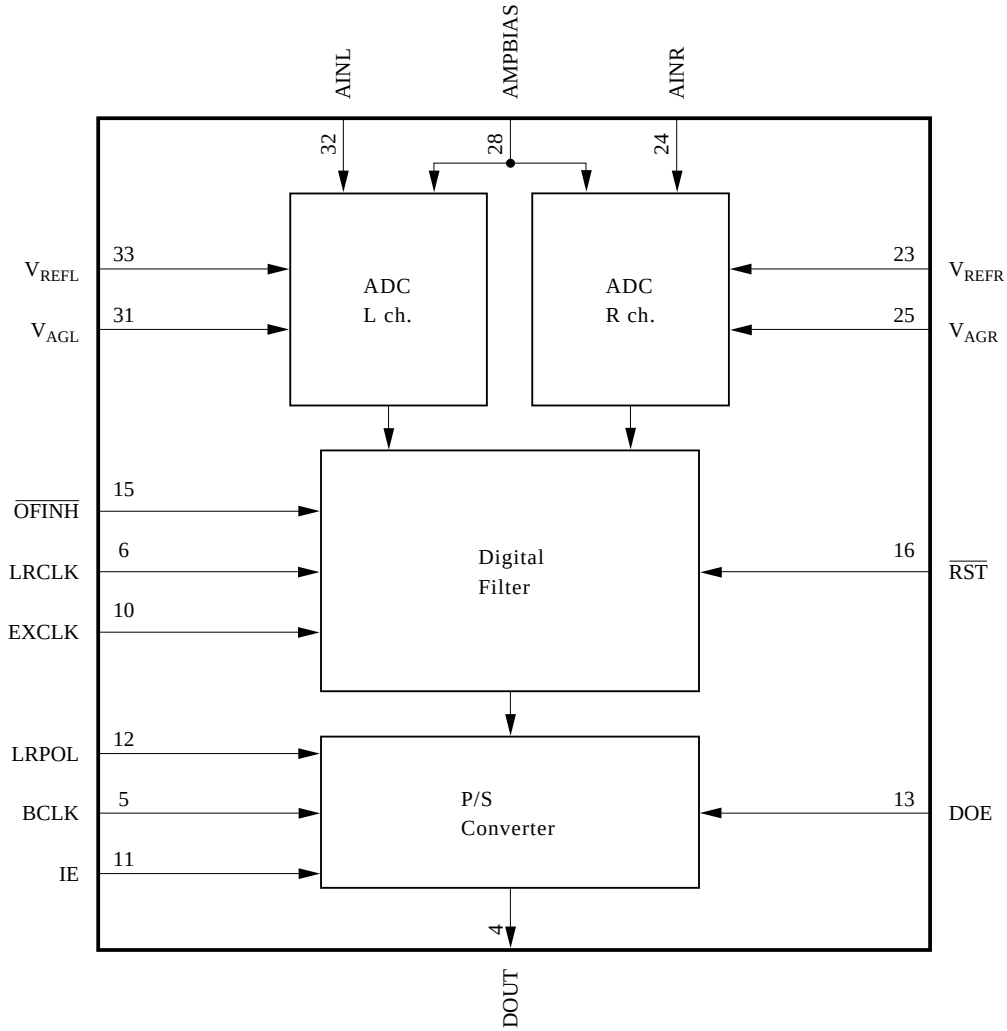
■ Pin Assignment



(TOP VIEW)

QFH044-P-1010

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description	
1	TEST1	I	Test pin.	Keep these at "L" level.
2	TEST2	I	Test pin.	Keep these at "L" level.
3	N.C.		No connection	
4	DOUT	O	Serial data output pin.	The data format is two's complement, MSB first, with bits packed to the left. After the 16 bits outputs, the output level is "L."
5	BCLK	I	Bit clock input pin.	Input a clock signal with a frequency between 32 f_s and 64 f_s.
6	LRCLK	I	LRCLK pin.	Input a f_s clock signal. When the LRPOL pin is at "L" level, the DOUT pin outputs the left channel data when this pin is at "L" level. When the LRPOL pin is at "H" level, the DOUT pin outputs the left channel data when this pin is at "H" level.
7	TCLK	O	Test clock pin.	Leave this pin open or keep it at "L" level.
8	DV_{SS1}		Ground pin for digital circuits.	Connect this to 0V.
9	DV_{DD1}		Power supply pin for digital circuits.	Connect this to a +5V supply.
10	EXCLK	I	256 f_s pin.	Input a 256 f_s clock signal.
11	IE	I	Output format selection pin.	"H" level; I^2S format "L" level; signal processing LSI format.
12	LRPOL	I	LRCLK polarity selection pin.	
13	DOE	I	Output control pin.	"L" level input places DOUT pin in high-impedance state.
14	TEST3	I	Test pin.	Keep this at "H" level.
15	$\overline{OFINH}$	I	Offset elimination circuit disable pin.	"L" level input disables the offset elimination circuit.
16	$\overline{RST}$	I	Reset pin.	"L" level input resets internal data. Always supply a "L" level pulse with a width greater than the LRCLK period when the power is first supplied or when waking the chip from a power-down mode.
17	DV_{DD3}	I	Power supply pin for digital circuits.	Connect this to a +5V supply.
18	DV_{SS3}	I	Ground pin for digital circuits.	Connect this to 0V.
19	AV_{SS4}	I	Ground pin for right channel analog circuit.	Connect this to 0V.
20	AV_{DD4}	I	Power supply pin for right channel analog circuits.	Connect this to a +5V supply.
21	AV_{SS6}	I	Ground pin for right channel analog switch driver.	Connect this to 0V.
22	AV_{DD6}	I	Power supply pin for right channel analog switch driver.	Connect this to a +5V supply.
23	V_{REFR}	I	Right channel reference level pin.	Connect this to a +1.0V supply.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
24	AINR	I	Right channel analog signal pin.
25	V_{AGR}	I	Right channel reference voltage pin. Connect this to a +2.5V supply.
26	AV_{DD3}	I	Power supply pin for right channel analog circuits. Connect this to a +5V supply.
27	AV_{SS3}	I	Ground pin for right channel analog circuits. Connect this to 0V.
28	AMPBIAS	I	Operational amplifier bias pin. Connect this to a +2.5V supply.
29	AV_{SS1}	I	Ground pin for left channel analog switch driver. Connect this to 0V.
30	AV_{DD1}	I	Power supply pin for left channel analog switch driver. Connect this to a +5V supply.
31	V_{AGL}	I	Left channel reference voltage pin. Connect this to a +2.5V supply.
32	AINL	I	Left channel analog signal pin.
33	V_{REFL}	I	Left channel reference level pin. Connect this to a +1.0V supply.
34	AV_{DD5}	I	Power supply pin for left channel analog circuits. Connect this to a +5V supply.
35	AV_{SS5}	I	Ground pin for left channel analog circuit. Connect this to 0V.
36	AV_{DD2}	I	Power supply pin for left channel analog circuits. Connect this to a +5V supply.
37	AV_{SS2}	I	Ground pin for left channel analog circuit. Connect this to 0V.
38	NSUB	I	Silicon substrate potential fixing pin. Connect this to the +5V analog power supply.
39	DV_{DD2}	I	Power supply pin for digital circuits. Connect this to a +5V supply.
40	DV_{SS2}	I	Ground pin for digital circuits. Connect this to 0V.
41	TPO	I	Test pin. Leave open or keep at "L" level.
42	TP1	I	Test pin. Leave open or keep at "L" level.
43	TP2	I	Test pin. Leave open or keep at "L" level.
44	TP3	I	Test pin. Leave open or keep at "L" level.

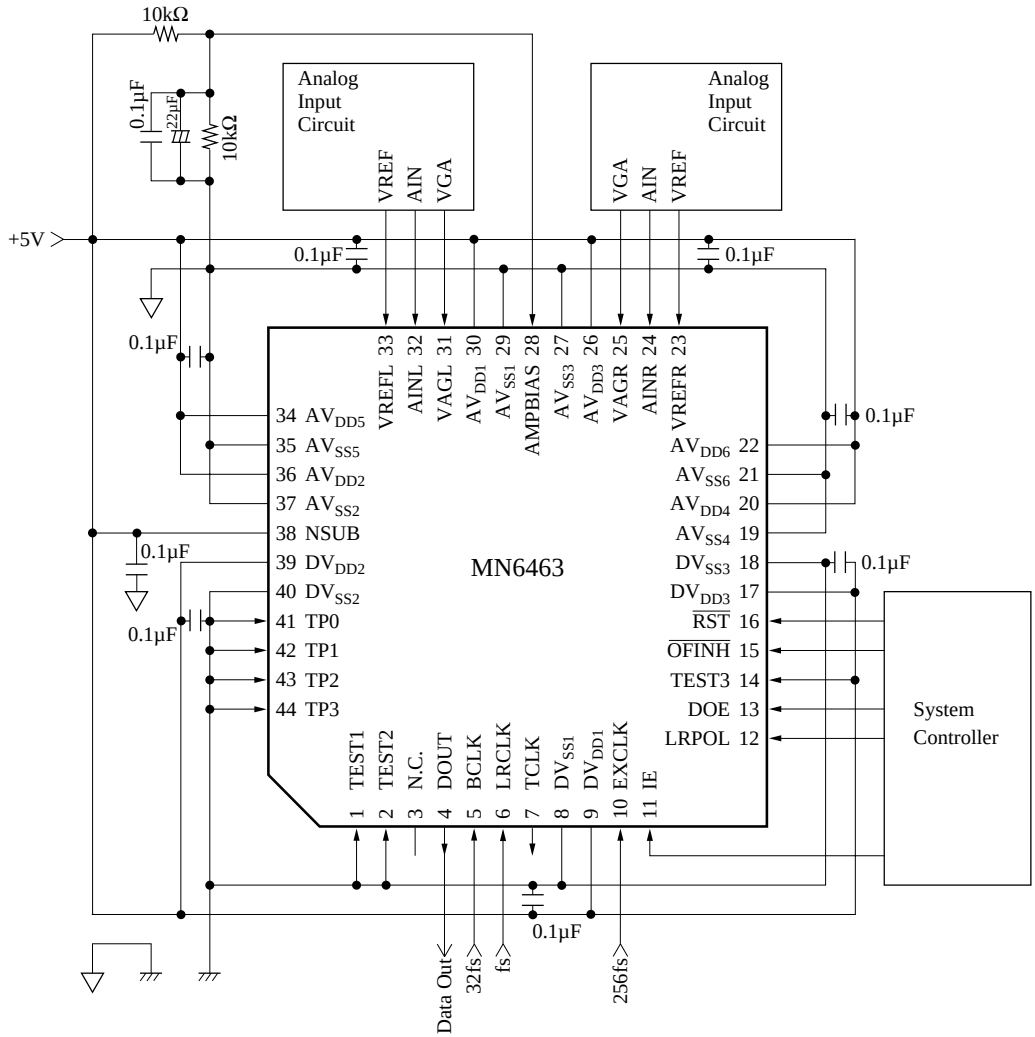
■ Conversion Characteristics

AV_{DD}=DV_{DD}=NSUB=5.0V, AMPBIAS=V_{AGL}=V_{AGR}=2.5V,

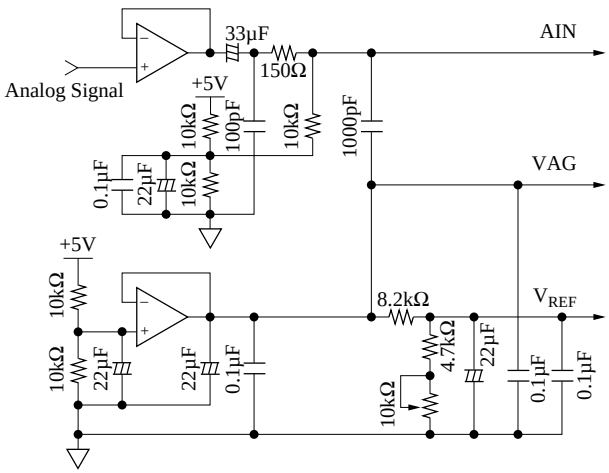
V_{REFL}=V_{REFR}=1.0V, AV_{SS}=DV_{SS}=0V, Ta=25˚C, f_{EXCLK}=12.288MHz

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Signal-to-noise ratio	S/N	EIAJ (1kHz)	88	94		dB
Dynamic range	D.R.	EIAJ (1kHz)	88	94		dB
Total harmonic distortion	THD+N	EIAJ (1kHz)		0.005	0.01	%
Channel separation	α	(1kHz)		100		dB

■ Application Circuit Example



Analog Input Circuit



■ Package Dimensions (Unit: mm)

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