MN5571

Gray Scale Font Engine

■ Overview

The MN5571 is a high-speed rasterizer that generates bit-mapped gray scale font data (bit-mapped font data with gray scale data for each bit) from outline font data (data describing the character outline).

The MN5571 uses two external SRAM devices: one is for a storage area holding the outline data; the other, for a work area holding intermediate results.

The MN5571 achieves its high processing speed with parallel processing of intermediate data generation, gray scale bit map generation, and transfer of the completed bit map data to external devices.

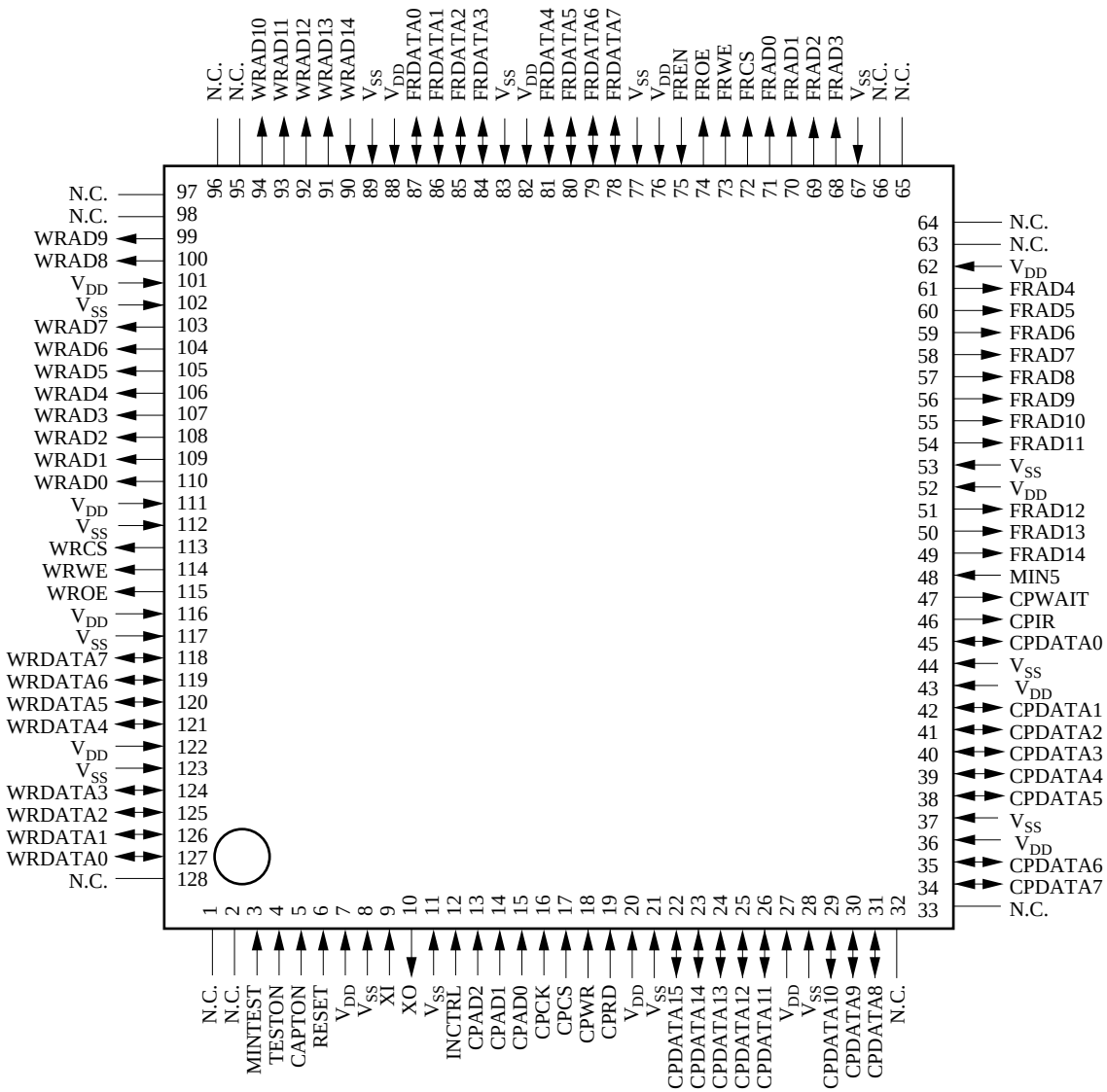
■ Features

- Gray scale support: Choice of 2, 4, 8, or 16 levels
- Character sizes: Max. 1024 × 1024 dots
  The character height and width need not be the same.
- Throughput: Approximately 1000 characters per second (matrix of 16 × 16 dots for typical Japanese text)
- Affine transformations: Slanting, rotation, mirror image, parallelogram
- Energy-saving modes: SLEEP and STOP modes
- Operating power supply voltage: 3.3 V ± 0.3 V (5 volt input also supported)

■ Applications

- Television displays:
  - Internet terminals
  - Set-top boxes
  - Game computers
  - Karaoke equipment
- CRT displays:
  - Personal computers
  - Word processors
- Liquid crystal displays:
  - Portable information terminals
  - Mobile communications terminals
  - Car navigation systems

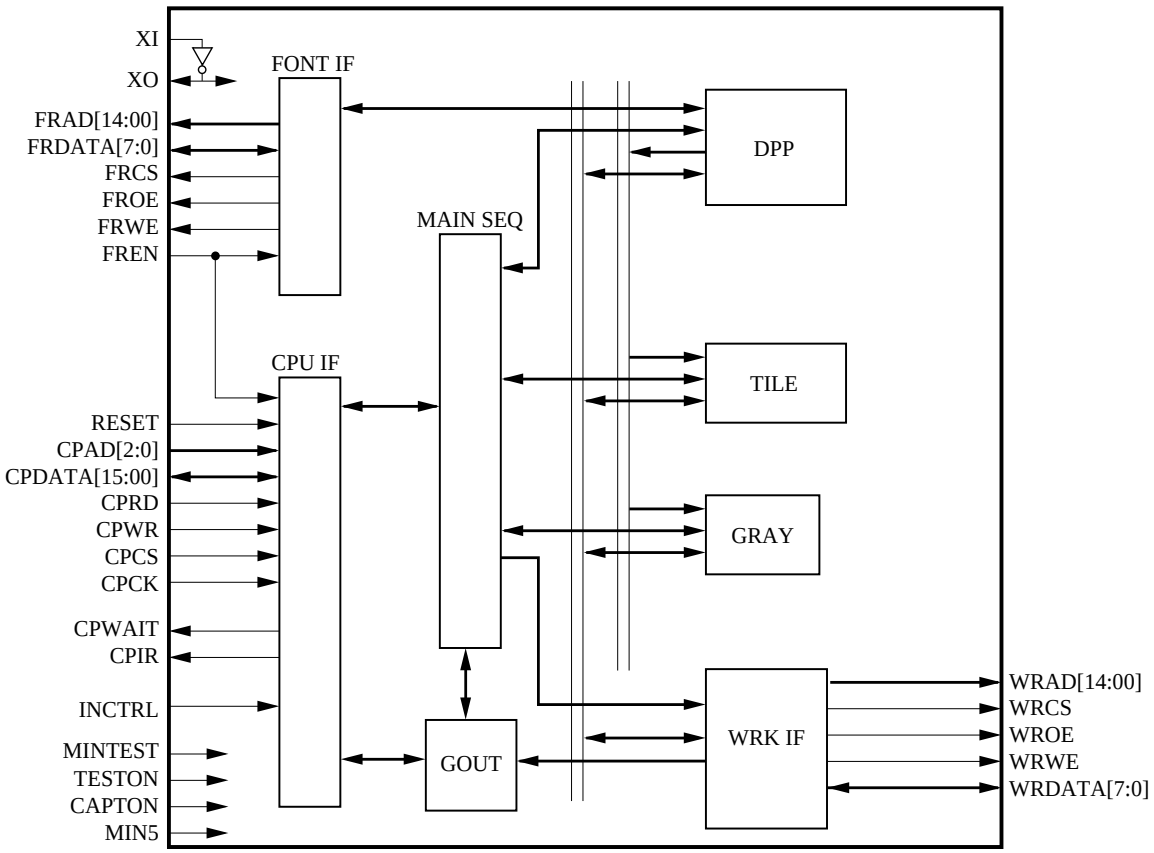
■ Pin Assignment



(TOP VIEW)
LQFP128-P-1818B

Note: Never leave V_{DD} and V_{SS} pins open.

■ Block Diagram



Block Descriptions

MAIN SEQ:	LSI's main sequencer. This block controls parallel operation of the other blocks.
CPU interface:	This interface block to the host CPU.
Font interface:	This interface block to the font memory.
WRK interface:	This interface block to the work memory.
GOUT:	This block transfers gray scale data from the WRK interface to the CPU interface.
DPP:	This block generates the data for generating tile-data.
TILE:	This block generates the tile-data.
GRAY:	This block generates the gray scale data from the tile-data.

■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
9	XI	I	Oscillator-cell input (system clock)
10	XO	O	Oscillator-cell output (system clock)
6	RESET	I	System reset signal (negative logic)
13 to 15	CPAD[2:0]	I	Address signals from host
22 to 26 ,29 to 31 , 34 ,35 , 38 to 42 ,45	CPDATA[15:00]	I/O	Data I/O signals to and from host
47	CPWAIT	O	Wait signal to host
46	CPIR	O	Interrupt request signal to host
19	CPRD	I	Read signal from host (negative logic)
18	CPWR	I	Write signal from host (negative logic)
17	CPCS	I	Chip select signal from host (negative logic)
16	CPCK	I	Clock signal from host
12	INCTRL	I	Signal switching to STOP mode
49 to 51 ,54 to 61 , 68 to 71	FRAD[14:00]	O	Address output signals to font RAM
78 to 81 ,84 to 87	FRDATA[7:0]	I/O	Data I/O signals to and from font RAM
72	FRCS	O	Read enable signal to font RAM (negative logic)
74	FROE	O	Chip select signal to font RAM (negative logic)
73	FRWE	O	Write enable signal to font RAM (negative logic)
75	FREN	I	Signal indicating presence of font RAM (negative logic)
90 to 94 ,99 ,100 , 103 to 110	WRAD[14:00]	O	Address output signals to work RAM
118 to 121 , 124 to 127	WRDATA[7:0]	I/O	Data I/O signals to and from work RAM
113	WRCS	O	Chip select signal to work RAM (negative logic)
115	WROE	O	Read enable signal to work RAM (negative logic)
114	WRWE	O	Write enable signal to work RAM (negative logic)
3	MINTEST	I	Test signal input (Normally keep this at "L" level.)
4	TESTON	I	Test signal input (Normally keep this at "L" level.)
5	CAPTON	I	Test signal input (Normally keep this at "L" level.)
48	MIN5	I	5 volt reference (If 5 volt input is not used, this pin has same voltage of V_{DD} .)
7 ,20 ,27 ,36 ,43 , 52 ,62 ,76 ,82 ,88 , 101 ,111 ,116 ,122	V_{DD}	I	Power supply pins (3.3 V ± 0.3 V)
8 ,11 ,21 ,28 , 37 ,44 ,53 ,67 , 77 ,83 ,89 ,102 , 112 ,117 ,123	V_{SS}	I	Ground pins (0 V)

■ Function Description

This section describes MN5571 functions concretely.

● Registers

The CPU controls the MN5571 operation by the following registers.

1. Address map

CPAD[2:0]:

(2)	(1)	(0)	Symbol	Contents	R/W
0	0	0	STAT	Status register	R
0	0	1	MASK	Interrupt register	R/W
0	1	0	COMM	Command register	R/W
0	1	1	DATA	Data register	R/W
1	0	0	INCNT	Font memory free register	R
1	0	1		Not used	
1	1	0		Not used	
1	1	1	SYCNT	System control register	W

2. Register bits

The following describes the meaning of the bits in the above registers.

• STAT register

This register indicates the MN5571's operating status. It is read-only. After reading, it sets all the set bits to "0" and resets the CPIR output pin.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	EM	—	—	GO	—	—	ER	GE	—	FE	IN

IN: The completion of work area initialization sets this bit to "1".
Read/write access to the work area is prohibited during initialization.

FE: The presence of the font memory RAM sets this bit to "1".

GE: The generation of output data sets this bit to "1".

ER: An invalid command error occurrence sets this bit to "1".

GO: Reading gray scale data when the gray scale data buffer is empty sets this bit to "1".

EM: When the font memory is empty, this bit is set to "1".

– : Unused

Bit 10 (EM) is set to "1" after a hardware or software reset, the program should always read the STAT register to clear it.

• MASK register

This register controls interrupt signals from the MN5571. It is a read/write register.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	EM	0	0	GO	0	0	ER	GE	0	0	IN

IN: Setting this bit to "1" produces an interrupt when the work memory has been initialized.

GE: Setting this bit to "1" produces an interrupt when output data has been generated.

ER: Setting this bit to "1" produces an interrupt when the chip encounters an invalid command.

GO: Setting this bit to "1" produces an interrupt when there is an attempt to read gray scale data from an empty gray scale data buffer.

EM: Setting this bit to "1" produces an interrupt when the font memory is empty.

0 : Unused

Reading the status register automatically clears the interrupt. The software's interrupt handler must always read the status register to clear the interrupt source. Always set unused bits to "0."

• COMM register

This register specifies the MN5571's operating mode. It is a read/write register.

This register accepts the following commands.

Hex	Command	Contents
0x0001	TCLR	Clear work memory area
0x0007	SRST	Software reset
0x8000	FTIN	Start font generation

The status is shown as NOP (0x0000) right after hardware or software reset while CPU reading the register, and is shown as 0x8001 (EXEC) in generating fonts while CPU reading the register.

• DATA register

The MN5571 uses this register for data I/O. It is a read/write register.

Register function depends on the contents of the COMM register.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Read/write data															

COMM / R/W	EXEC(0x8001)	Other value
Reads	Gray scale data read	Undefined
Writes	Font data write	Undefined

• INCNT register

This register indicates the amount of free font-memory. It is read only.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FREE													

The field FREE indicates the number of words (16 bits) available for storing font data.

• System control register (SYCNT)

This register controls the MN5571's power-saving mode. It is write only.

This register accepts the following commands.

Reading this register leads to unpredictable operation (not guaranteed).

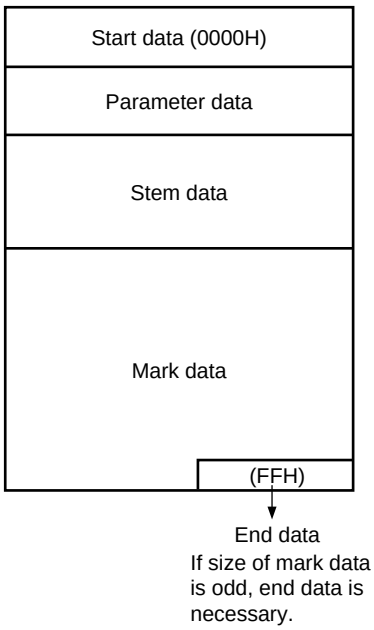
Hex	Command	Contents
0xAAAA	CKSP	Switches into SLEEP mode (stopping internal clock)
0x0000 (0xAAAA)	CKST	Switches out of SLEEP mode (restarting internal clock)

Always wait ten clock cycles when switching into or out of SLEEP mode.

• Data Formats for Input Font Data and Output Gray Scale Data

1. Data Format for Input Font Data

The MN5571 expects input font data in the following format.



2. Data Formats for Output Gray Scale Data

The MN5571 delivers gray scale data in the following formats.

Gray Scale Data Format for 4, 8, or 16 Levels

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	mode		–	width						–	height					
1	pixel[0]				pixel[1]				pixel[2]				pixel[3]			
2	pixel[4]				pixel[5]				pixel[6]				pixel[7]			
3	pixel[8]				pixel[9]				pixel[10]				_	_	_	_
4	pixel[11]				pixel[12]				pixel[13]				pixel[14]			

Line 0

Line 1

Gray Scale Data Format for 2 Levels

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	mode		–	width						–	height					
1	pixel[0] to pixel[15]															
2	pixel[16] to pixel[21]						_	_	_	_	_	_	_	_	_	_
3	pixel[22] to pixel[37]															
4	pixel[38] to pixel[43]						_	_	_	_	_	_	_	_	_	_

Line 0

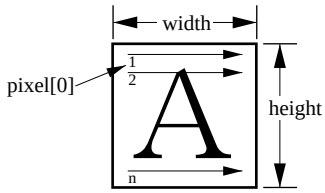
Line 1

Description of Gray Scale Data Format

mode: gray scale

3: 2 levels
2: 4 levels
1: 8 levels
0: 16 levels

width, height, pixel[n]: character size and data position



- Power-saving standby modes

Two power-saving standby modes are supported: SLEEP and STOP. The SLEEP mode conserves power by turning off the internal clock signal CLK. The STOP mode produces a complete stop by shutting down the oscillator circuit. It also cuts off the input pins to the host to prevent leakage current due to input penetration current.

■ Operating Procedure

● Overview

The procedure for operating the MN5571 is divided into four main steps.

- Initialization

  This step, which is performed only once after a hardware or software reset, consists of clearing the MN5571's internal registers and the memory and giving the MN5571 the command to start rasterizing.

- Writing font data

  The font data for the characters to be rasterized are transferred to the MN5571.

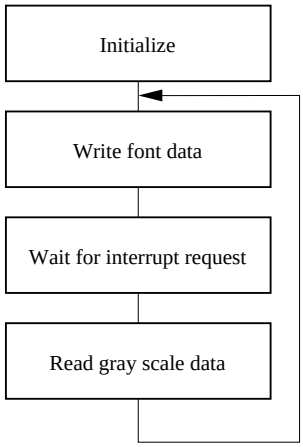
- Waiting for interrupt request

  This step waits for the MN5571 to indicate that it is ready for output.

- Reading gray scale data

  This step outputs the gray scale data that the MN5571 has generated.

Operational flow

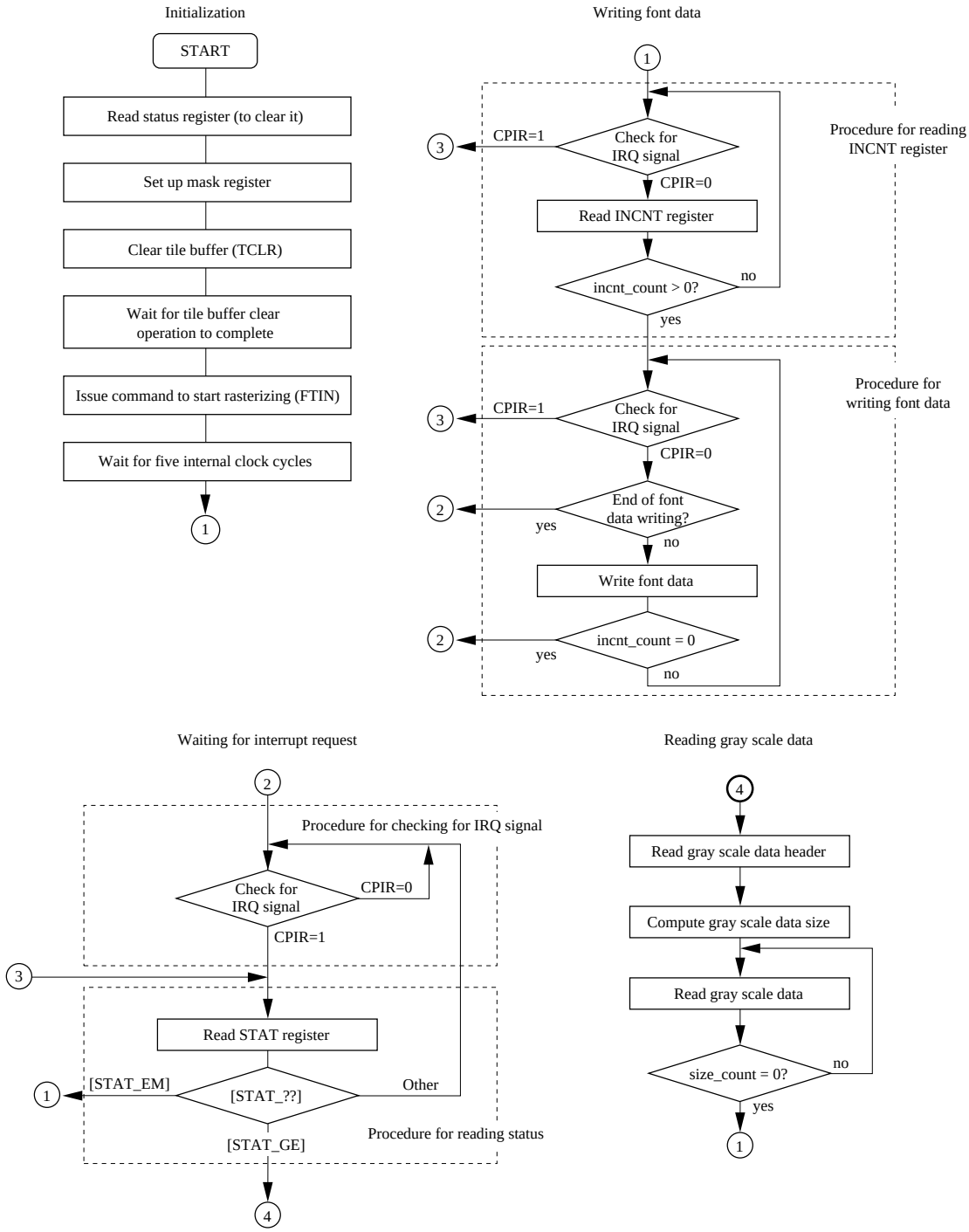


● Examples of Operation

This section gives two examples in different procedures.

1. With Font Memory RAM

This example shows the general procedure for using the rasterizer together with an external RAM for font data. Driving the FREN pin at "L" level configures the MN5571 for this mode of operation. The following flowchart assumes software control of the MN5571.



Description for flowchart

The following is a detailed description of the flowchart.

(1) Initialization

This step is performed only once after a hardware or software reset.

If there is a font memory RAM attached, the FREN pin must be at "L" level before the hardware reset.

- Read status register

  A font memory RAM attached is confirmed.

  STAT_FE = "1"

  The status register is read and that the FE bit is "1" is checked.

  After a hardware or software reset, always the STAT register is read to initialize it.

- Set up mask register

  The mask register is set up to enable the desired interrupts.

  MASK ← 16'b0000_0100_1000_1001;
  (STAT_EM, STAT_GO, STAT_GE, STAT_IN)

- Clear tile buffer

  The TCLR instruction code is written to the COMM register to initiate clearing of the tile buffer.

  COMM ← TCLR

- Wait for tile buffer clear operation to complete

  The IN bit in the STAT register indicates the completion of a tile buffer clear operation.

  STAT_IN = "1"

  This example sets the IN bit in the MASK register and waits for the corresponding interrupt request.

  When accepting the interrupt request, always the status register is read to clear the interrupt request.

  Do not access the command register while the chip is clearing the tile buffer.

- Issue command to start rasterizing

  The FTIN instruction code is written to the COMM register to start rasterizing.

  COMM ← FTIN

- Wait for five internal clock cycles

  To ensure circuit stability, do not access the MN5571 command register within 5 internal clock cycles after writing the FTIN instruction code.

(2) Writing font data

The following is the procedure for writing font data to the MN5571.

(a) Procedure for reading INCNT register

- Check for IRQ signal

  IRQ signal is checked. If the CPIR bit is "1," the status register is read.

- Read INCNT register

  The number of words available for storing font data is read from the INCNT register.

  << incnt_count >> ← INCNT

  This number indicates how much space is available for font data in the font memory.

- INCNT contents check

  If the INCNT register is "0," the register contents are read again.

(b) Procedure for writing font data

• Check for IRQ signal

Interrupt requests are checked. If the CPIR bit is "1," the status register is read.

• Check word count for font data to be written

When the count reaches zero, the state is switched to waiting for a change in the IRQ signal.

• Write font data

One word of font data is written to the DATA register.

DATA ← << font data >>

<< incnt_count >> ← << incnt_count >> – 1

• INCNT check

When the count reaches zero, the state is switched to waiting for a change in the IRQ signal.

(3) Waiting for IRQ signal change

• Checking for IRQ signal

Wait for a change in the IRQ signal generated in the status register.

• Read STAT register

STAT register is read.

• Branch by status register bit

If the STAT_EM bit is "1," the state goes to read the contents of the INCNT register. If the STAT_GM bit is "1," it goes to read the gray scale data.

Otherwise, it returns to waiting for a change in the IRQ signal.

(4) Reading gray scale data

This step reads the gray scale data from the MN5571.

• Read gray scale data header

The ghead, the gray scale data header is read from the DATA register.

<< ghead >> ← DATA

• Compute gray scale data size

Compute the size of the gray scale data set using the following procedure.

```
mode = ghead[15:14];
width = ghead[12:7];
height = ghead[5:0];
if(mode=3{
     size = (width/4+((width%4)!=0))*height;
}else{
     size = (width/16+((width%16)!=0))*height;
}
```

• Read gray scale data

Numbers of data expressed by contents of "size" are read from DATA register.

<< gray_scale_data >> ← DATA

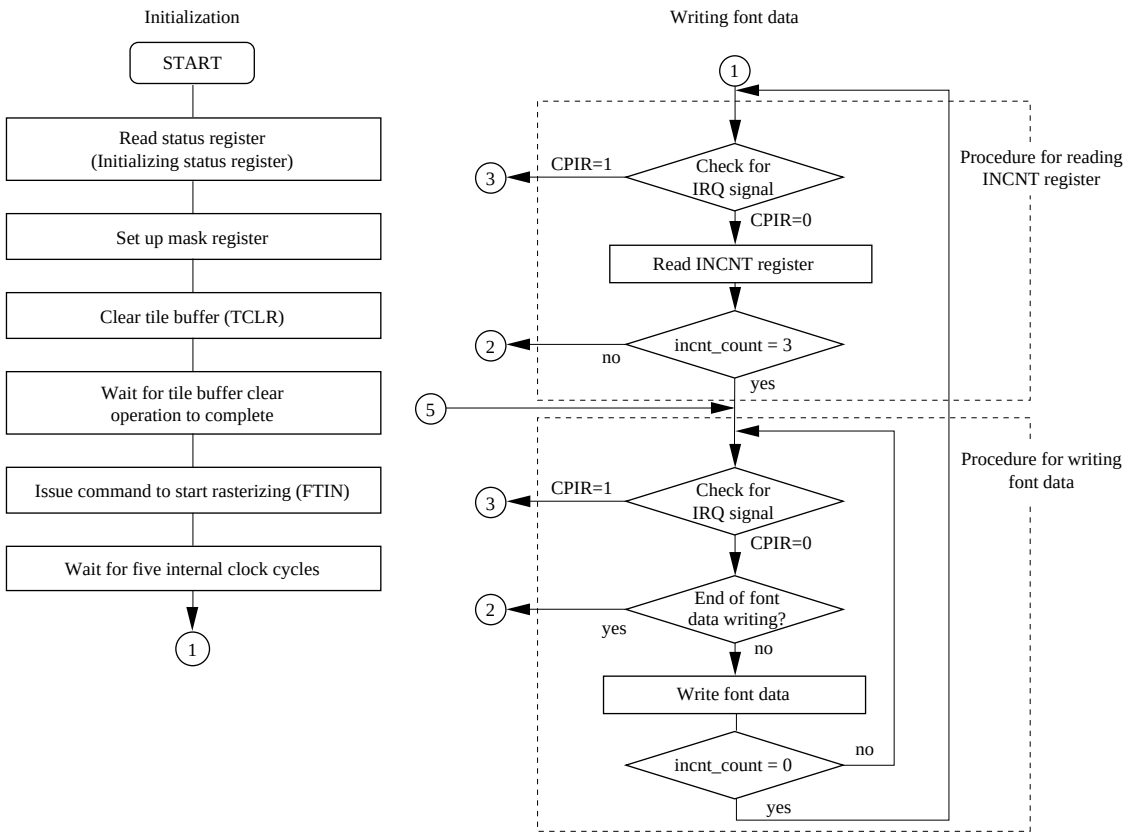
<< size_count >> ← << size_count >> – 1

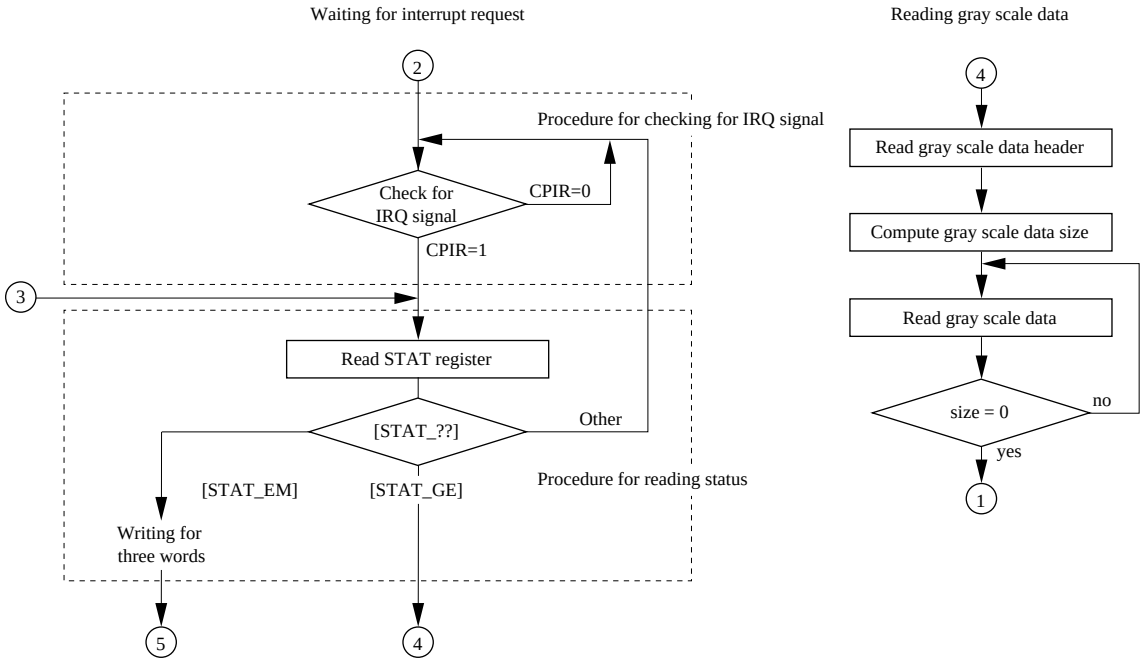
• Check size

When all the gray scale data has been read, the contents of the INCNT register are read.

2. Chip without Font Memory RAM

This example shows the general procedure for using the rasterizer without an external RAM for font data. Driving the FREN pin at "H" level configures the MN5571 for this mode of operation. The following flow-chart assumes software control of the MN5571.





Description for flowchart

The following is a detailed description of the flowchart.

(1) Initialization

This step is performed only once after a hardware or software reset.

If there is no font memory RAM attached, the FREN pin must be at "H" level before the hardware reset.

• Read status register

No font memory RAM attached is confirmed.

STAT_FE = "0"

The status register is read and the state that the FE bit is "0" is checked.

After a hardware or software reset, the STAT register is always read to initialize it.

• Set up mask register

The mask register is set up to enable the desired interrupts.

MASK ← 16'b0000_0100_1000_1001;
(STAT_EM, STAT_GO, STAT_GE, STAT_IN)

• Clear tile buffer

The TCLR instruction code is written to the COMM register to initiate clearing of the tile buffer.

COMM ← TCLR

• Wait for tile buffer clear operation to complete

The IN bit in the STAT register indicates the completion of a tile buffer clear operation.

STAT_IN = "1"

This example sets the IN bit in the MASK register and waits for the corresponding interrupt request.

When accepting the interrupt request, the status register is always read to clear the interrupt request.

Do not access the command register while the chip is clearing the tile buffer.

• Issue command to start rasterizing

The FTIN instruction code is written to the COMM register to start rasterizing.

COMM ← FTIN

• Wait for five internal clock cycles

To ensure circuit stability, do not access the MN5571 command register within 5 internal clock cycles after writing the FTIN instruction code.

(2) Writing font data

The following is the procedure for writing font data to the MN5571.

(a) Procedure for reading INCNT register

• Check for IRQ signal

Interrupt request is checked. If the CPIR bit is "1," the status register is read.

• Read INCNT register

The number of words available for storing font data is read from the INCNT register.

<< incnt_count >> ← INCNT

This number indicates how much space is available for font data (max. 3).

• INCNT check

If the INCNT register contains a number other than three, the state goes to wait for a change in the IRQ signal.

(b) Procedure for writing font data

• Check for IRQ signal

Interrupt requests are checked. If the CPIR bit is "1," the status register is read.

• Check word count for font data to be written

When the count reaches zero, the state is switched to waiting for a change in the IRQ signal.

• Write font data

One word of font data to the DATA register is written.

DATA ← << font data >>

<< incnt_count >> ← << incnt_count >> – 1

• INCNT check

When the count reaches zero, the state returns to reading the contents of the INCNT register.

(3) Waiting for interrupt request

• Checking for IRQ signal

The state waits for a change in the IRQ signal generated by a change in the status register.

• Read STAT register

STAT register is read.

• Branch by status register bit

If the STAT_EM bit is "1," there is room to write three words of font data, so the state is switched to writing font data. If the STAT_GE bit is "1," the state goes to read the gray scale data.

Otherwise, it returns to waiting for a change in the IRQ signal.

(4) Reading gray scale data

This step reads the gray scale data from the MN5571.

• Read gray scale data header

The ghead, the gray scale data header is read from the DATA register.

<< ghead >> ← DATA

• Compute gray scale data size

Compute the size of the gray scale data set using the following procedure.

```
mode = ghead[15:14];
width = ghead[12:7];
height = ghead[5:0];
if(mode<3{
     size = (width/4+((width%4)!=0))*height;
}else{
     size = (width/16+((width%16)!=0))*height;
}
```

• Read gray scale data

Numbers of data expressed by contents of "size" are read from DATA register.

<<gray_scale_data>> ← DATA

<<size_count>> ← <<size_count>> –1

• Check size

When all the gray scale data has been read, the contents of the INCNT register are read.

● Additional Notes

- The most efficient timing for writing font data is once every 400 ns* (8 internal clock cycles).
- The most efficient timing for reading gray scale data is once every 750 ns* (15 internal clock cycles).

Note: * At a system clock frequency of 20 MHz (an internal clock cycle time of 50 ns).

■ External Interface Specifications

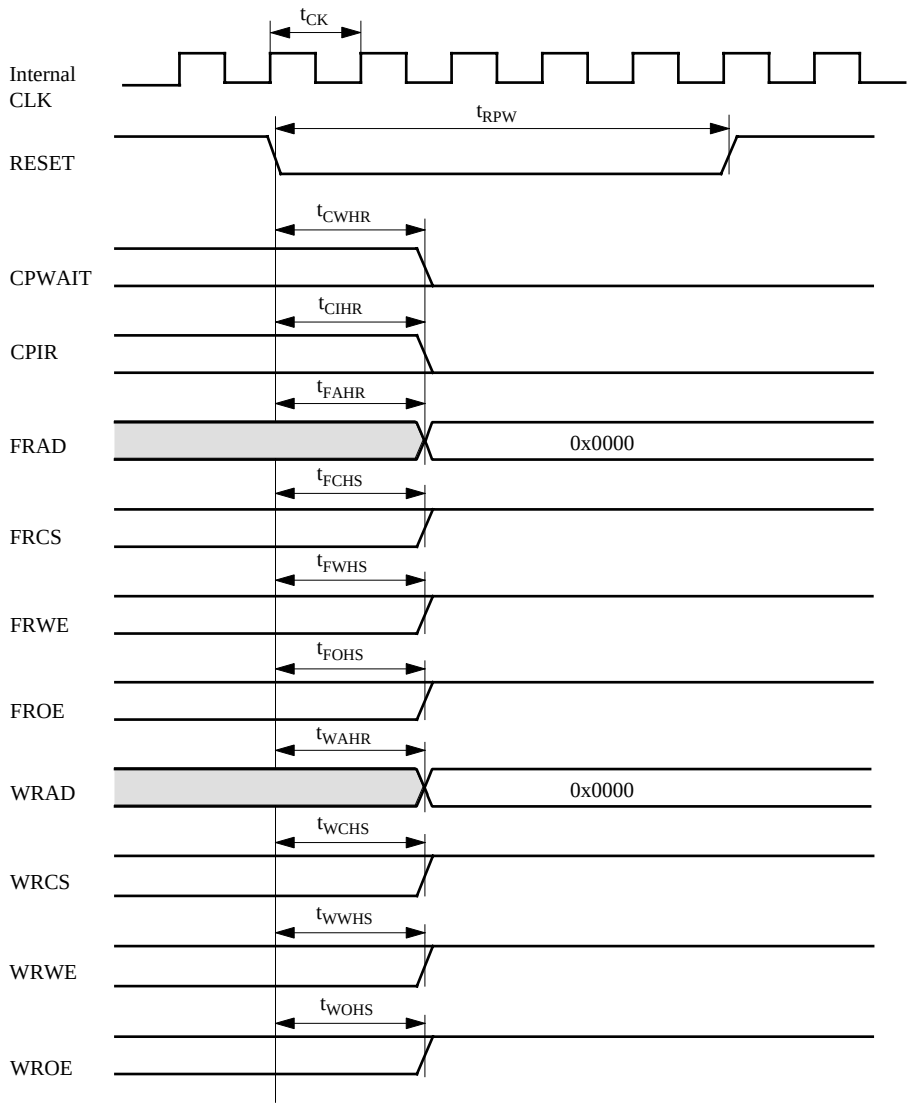
The following are the I/O timing specifications for the chip's external interfaces.

1. Hardware reset

(a) Timing chart

The RESET signal is not synchronized with the internal clock.

• Hardware RESET Timing



(b) AC characteristics

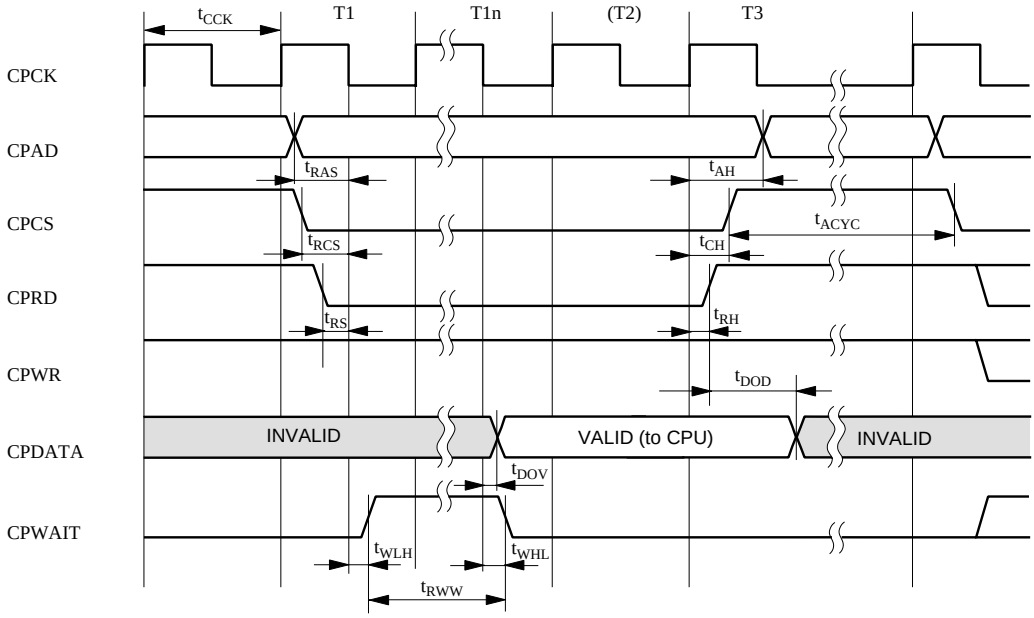
Parameter	Symbol	min	max	Unit
Internal clock cycle	t_{CK}	40	—	ns
RESET pulse width	t_{RPW}	$t_{CK} \times 1$	—	ns
CPWAIT reset validation time	t_{CWHR}	—	40	ns
CPIR reset validation time	t_{CIHR}	—	40	ns
FRAD reset validation time	t_{FAHR}	—	40	ns
FRCS set validation time	t_{FCHS}	—	40	ns
FRWE set validation time	t_{FWHS}	—	40	ns
FROE set validation time	t_{FOHS}	—	40	ns
WRAD reset validation time	t_{WAHR}	—	40	ns
WRCS set validation time	t_{WCHS}	—	40	ns
WRWE set validation time	t_{WWHS}	—	40	ns
WROE set validation time	t_{WOHS}	—	40	ns

Note: The load capacity for the host interface is 30 pF; for the SRAM interface, 20 pF.

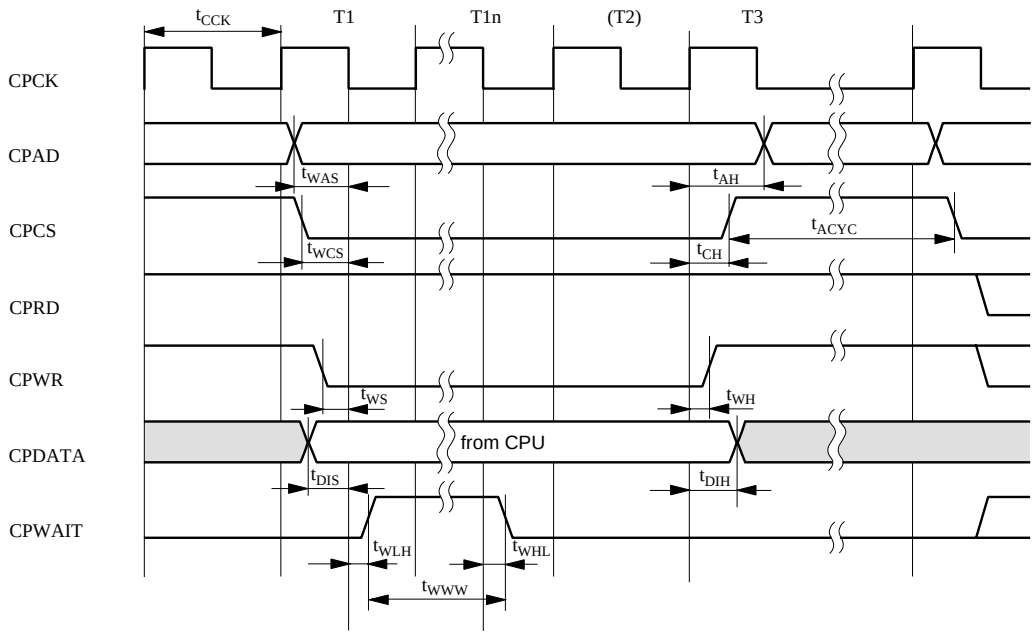
2. Host interface

(a) Timing charts

• CPU Read Timing



• CPU Write Timing



(b) AC characteristics

• Read cycle

Parameter	Symbol	min	max	Unit
CPU clock cycle	t_{CCK}	40	—	ns
Internal clock cycle	t_{CK}	40	—	ns
CPAD setup time relative to falling edge of CPCK	t_{RAS}	10	—	ns
CPCS setup time relative to falling edge of CPCK	t_{RCS}	10	—	ns
CPRD setup time relative to falling edge of CPCK	t_{RS}	10	—	ns
CPWAIT rise time relative to falling edge of CPCK	t_{WLH}	—	22	ns
CPAD hold time relative to rising edge of CPCK	t_{AH}	0	—	ns
CPCS hold time relative to rising edge of CPCK	t_{CH}	0	—	ns
CPRD hold time relative to rising edge of CPCK	t_{RH}	0	—	ns
CPDATA validation time relative to falling edge of CPCK	t_{DOV}	—	0	ns
CPDATA delay time relative to rising edge of CPRD	t_{DOD}	0	—	ns
CPWAIT fall time relative to falling edge of CPCK	t_{WHL}	—	22	ns
CPCS fall time relative to rising edge of CPCS	t_{ACYC}	$t_{CK} \times 2$	—	ns
Width of read cycle CPWAIT "H" pulse	t_{RWW}	$t_{CCK} \times 3$	—	ns

Note: The load capacity for the host interface is 30 pF.

• Write cycle

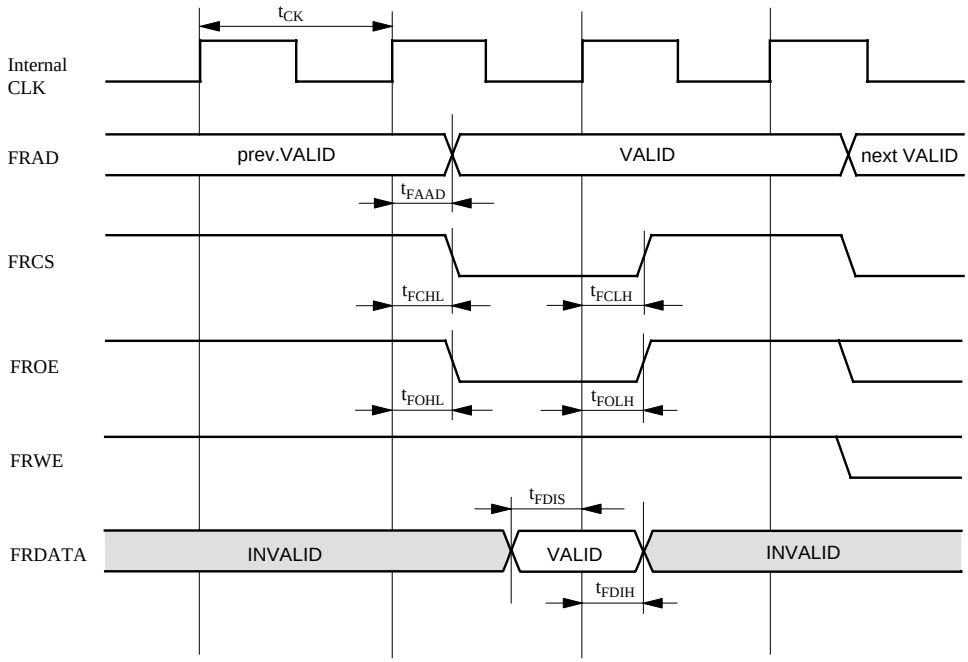
Parameter	Symbol	min	max	Unit
CPU clock cycle	t_{CCK}	40	—	ns
Internal clock cycle	t_{CK}	40	—	ns
CPAD setup time relative to falling edge of CPCK	t_{WAS}	10	—	ns
CPCS setup time relative to falling edge of CPCK	t_{WCS}	10	—	ns
CPWR setup time relative to falling edge of CPCK	t_{WS}	10	—	ns
CPDATA setup time relative to falling edge of CPCK	t_{DIS}	10		
CPWAIT rise time relative to rising edge of CPCK	t_{WLH}	—	22	ns
CPAD hold time relative to rising edge of CPCK	t_{AH}	0	—	ns
CPCS hold time relative to rising edge of CPCK	t_{CH}	0	—	ns
CPWR hold time relative to rising edge of CPCK	t_{WH}	0	—	ns
CPDATA hold time relative to rising edge of CPCK	t_{DIH}	—	0	ns
CPWAIT fall time relative to falling edge of CPCK	t_{WHL}	—	22	ns
CPCS fall time relative to rising edge of CPCS	t_{ACYC}	$t_{CK} \times 2$	—	ns
Width of write cycle CPWAIT "H" pulse	t_{WWW}	$t_{CCK} \times 2$	—	ns

Note: The load capacity for the host interface is 30 pF.

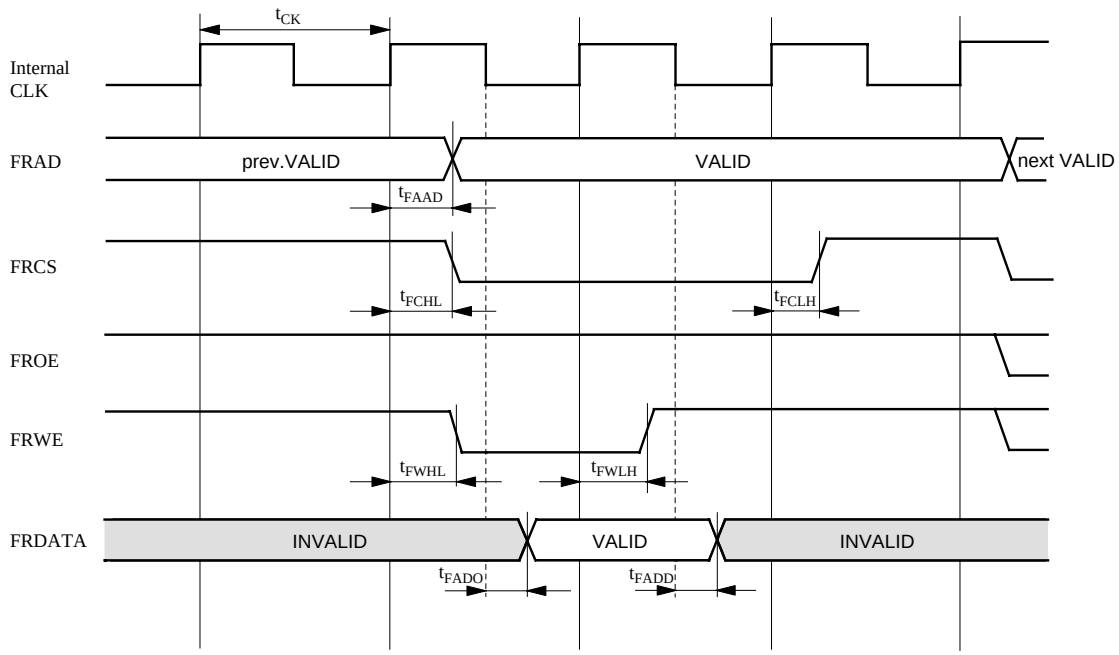
3. Font memory interface

(a) Timing charts

• FONT MEMORY Read Timing



• FONT MEMORY Write Timing



(b) AC characteristics

• Read cycle

Parameter	Symbol	min	max	Unit
Internal clock cycle	t_{CK}	40	—	ns
FRAD delay time relative to rising edge of CLK	t_{FADD}	—	20	ns
FRCS fall time relative to rising edge of CLK	t_{FCHL}	—	13	ns
FROE fall time relative to rising edge of CLK	t_{FOHL}	—	13	ns
FRCS rise time relative to rising edge of CLK	t_{FCLH}	—	6 + α	ns
FROE rise time relative to rising edge of CLK	t_{FOLH}	—	13	ns
FRDATA setup time relative to rising edge of CLK	t_{FDIS}	6	—	ns
FRDATA hold time relative to rising edge of CLK	t_{FDIH}	12	—	ns

• Write cycle

Parameter	Symbol	min	max	Unit
Internal clock cycle	t_{CK}	40	—	ns
FRAD delay time relative to rising edge of CLK	t_{FADD}	—	20	ns
FRCS fall time relative to rising edge of CLK	t_{FCHL}	—	13	ns
FRWE fall time relative to rising edge of CLK	t_{FWHL}	—	13	ns
FRCS rise time relative to rising edge of CLK	t_{FCLH}	—	6 + α	ns
FRWE rise time relative to rising edge of CLK	t_{FWLH}	—	14	ns
FRDATA validation time relative to falling edge of CLK	t_{FADO}	—	12	ns
FRDATA delay time relative to falling edge of CLK	t_{FADD}	—	8	ns

Notes

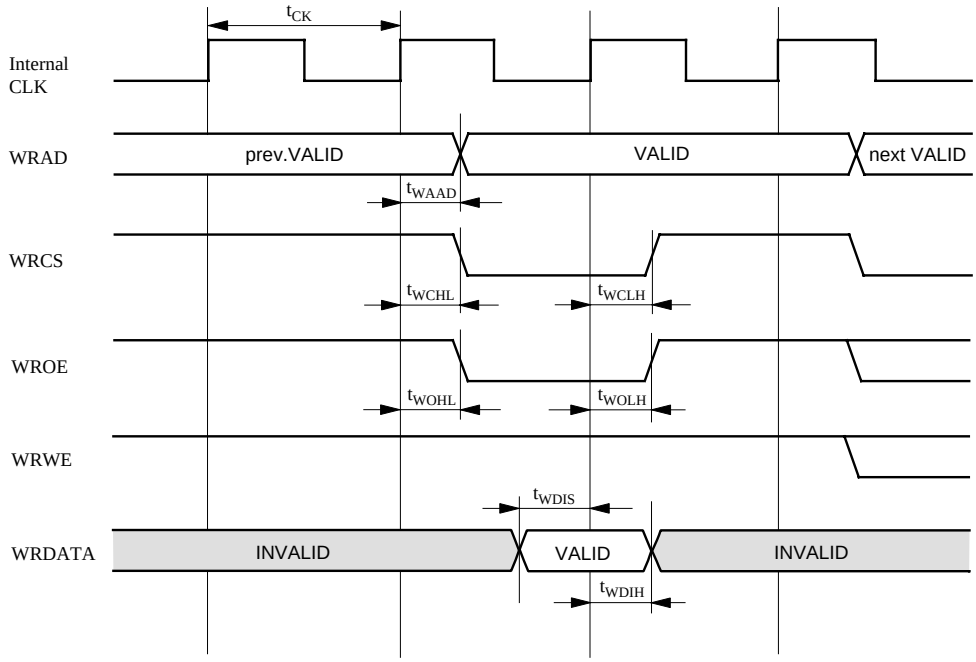
1: The load capacity for the SRAM interface is 20 pF.

2: Because the FRCS pin uses N-channel open drain output, the pull-up time, α, depends on the value of the external pull-up resistor.

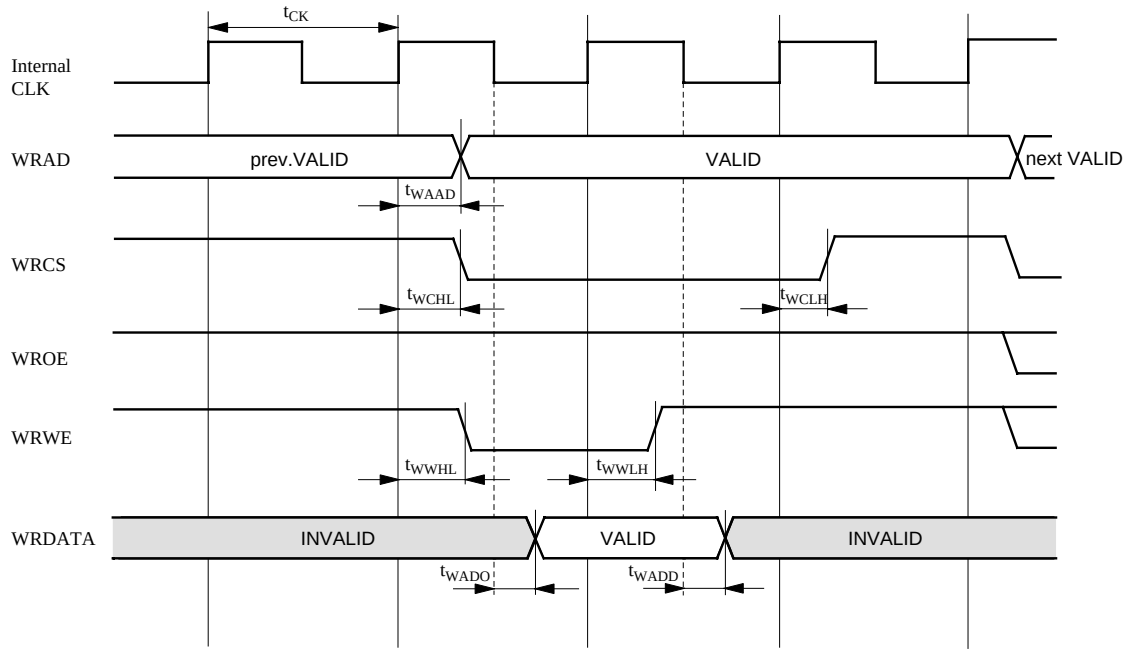
4. Work memory interface

(a) Timing charts

• WORK MEMORY Read Timing



• WORK MEMORY Write Timing



(b) AC characteristics

• Read cycle

Parameter	Symbol	min	max	Unit
Internal clock cycle	t_{CK}	40	—	ns
WRAD delay time relative to rising edge of CLK	t_{WADD}	—	20	ns
WRCS fall time relative to rising edge of CLK	t_{WCHL}	—	13	ns
WROE fall time relative to rising edge of CLK	t_{WOHL}	—	13	ns
WRCS rise time relative to rising edge of CLK	t_{WCLH}	—	6 + α	ns
WROE rise time relative to rising edge of CLK	t_{WOLH}	—	13	ns
WRDATA setup time relative to rising edge of CLK	t_{WDIS}	6	—	ns
WRDATA hold time relative to rising edge of CLK	t_{WDIH}	12	—	ns

• Write cycle

Parameter	Symbol	min	max	Unit
Internal clock cycle	t_{CK}	40	—	ns
WRAD delay time relative to rising edge of CLK	t_{WADD}	—	20	ns
WRCS fall time relative to rising edge of CLK	t_{WCHL}	—	13	ns
WRWE fall time relative to rising edge of CLK	t_{WWHL}	—	13	ns
WRCS rise time relative to rising edge of CLK	t_{WCLH}	—	6 + α	ns
WRWE rise time relative to rising edge of CLK	t_{WWLH}	—	14	ns
WRDATA validation time relative to falling edge of CLK	t_{WADO}	—	12	ns
WRDATA delay time relative to falling edge of CLK	t_{WADD}	—	8	ns

Notes

1: The load capacity for the SRAM interface is 20 pF.

2: Because the FRCS pin uses N-channel open drain output, the pull-up time, α, depends on the value of the external pull-up resistor.

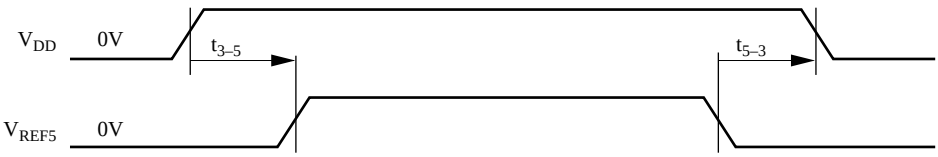
■ Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	– 0.3 to +4.6	V
5 volt reference voltage *1	V_{REF5}	– 0.3 to +5.7	V
Input pin voltage (except TYPE-* pins)	V_I	– 0.3 to V_{DD}+0.3	V
Input pin voltage (except pins labeled TYPE-A)	V_{I5}	– 0.3 to 6.0*2	V
Output pin voltage (except TYPE-* pins)	V_O	– 0.3 to V_{DD}+0.3	V
Output pin voltage (except pins labeled TYPE-A)	V_{O5}	– 0.3 to 6.0*2	V
Output pin voltage (except pins labeled TYPE-B)	V_{O5}	– 0.3 to V_{REF5}+0.3*2	V
Output current (pins labeled TYPE-HL2)	I_O	±6	mA
Output current (pins labeled TYPE-HL4)	I_O	±12	mA
Output current (pins labeled TYPE-L4)	I_{OL}	+12	mA
Power Dissipation	P_D	1340	mW
Operating ambient temperature	T_{opr}	–40 to 70	˚C
Storage temperature	T_{stg}	–55 to 150	˚C

Notes

*1: The rising and falling edges in the power supply sequence must satisfy the requirements outlined in the following timing chart.



Both t_{3-5} and t_{5-3} must be greater than or equal to zero.
Both V_{DD} and V_{REF5} must have smooth transitions.

*2: If $V_{DD} \leq 1.4$ V, the range is – 0.3 to 4.6 V.

*3: TYPE-A pins: CPAD0 to 2, CPCK, CPCS, CPRD, CPWR, FRCS, FREN, WRCS, RESET, INCTRL

TYPE-B pins: CPDATA0 to 15, FRDATA0 to 7, WRDATA0 to 7

TYPE-HL2 pins: FRAD0 to 14, WRAD0 to 14

TYPE-HL4 pins: CPIR, FROE, FRWE, WROE, WRWE, CPDATA0 to 15, CPWAIT, FRDATA0 to 7, WRDATA0 to 7

TYPE-L4 pins: FRCS, WRCS

TYPE-* pins mean TYPE-A, TYPE-B, TYPE-HL2, TYPE-HL4, and TYPE-L4 pins.

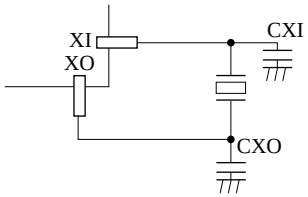
*4: The above ratings represent the maximum values that may be applied without damaging the chip, not the limits for guaranteed operation.

*5: Directly connect all V_{DD} pins to external power supplies and all V_{SS} pins to the ground.

■ Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply voltage	V_{DD}		3.0	3.3	3.6	V
5 volt reference voltage	V_{REF5}		4.75	5.0	5.25	V
Rise time for input	t_r		0		100	ns
Fall time for input	t_f		0		100	
Oscillation frequency	f_{OSC1}	25MHz Xtal		25		MHz
Recommended value for external capacitance	C_{XI7}	V_{DD}=3.3V Built-in feedback resistor		47		pF
	C_{XO7}			47		
Ambient temperature	Ta		0		70	˚C



Note: Because oscillation characteristics depend on such factors as oscillator model and external capacitance, always consult the oscillator manufacturer when selecting components.

■ Input/Output Capacitance

Parameter	Symbol	Conditions	min	typ	max	Unit
Input pins	C_{IN}	V_{DD}=V_I=0V f=1MHz, Ta=25˚C		7	15	pF
Output pins	C_{OUT}			7	15	pF
I/O pins	$C_{I/O}$			7	15	pF

■ Electrical Characteristics

V_{DD}=3.0 to 3.6V, V_{REF5}=4.75 to 5.25V, V_{SS}=0.00V, f_{TEST}=25MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent supply current	I_{DDS}	V_I (pull-up) = open V_I (pull-down) = open V_I (XI) =V_{DD}*1 Other input pins and I/O pins in the high-impedance state are all simultaneously connected to either the V_{SS} or V_{DD} level.			50	µA
5 volt reference power supply V_{REF5} (MIN5 pin) input leakage current	I_{LRF5}				±20	µA
Operating supply current	I_{DDO}	V_I=V_{DD} or V_{SS} f=25MHz V_{DD}=3.3V Outputs open		50	100	mA
Operating supply current in the SLEEP mode	I_{SLP}	V_I=V_{DD} or V_{SS} f=25MHz V_{DD}=3.3V Outputs open		3	6	mA
Operating supply current in the STOP mode	I_{STP}	V_I=V_{DD} or V_{SS} f=25MHz V_{DD}=3.3V Outputs open			50	µA
Oscillator circuit: XO						
Built-in feedback resistor	R_{fb7}	V_I=V_{DD} or V_{SS} V_{DD}=3.3V	313	940	2820	kΩ
CMOS level inputs: CAPTON, TESTON						
"H" level input voltage	V_{IH2}		V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}		0		V_{DD} × 0.3	V
Input leakage current	I_{LI}	V_I=V_{DD} or V_{SS}			±5	µA
CMOS level inputs with pull-down resistor: MINTEST						
"H" level input voltage	V_{IH2}		V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}		0		V_{DD} × 0.3	V
Pull-down resistance	R_{PD1}	V_I=V_{DD}	10	30	90	kΩ
Input leakage current	I_{LIPD}	V_I=V_{SS}			±10	µA

Note *1: The V_{DD} applied to the oscillator pin XI must use a power supply different from that for the I_{DDS} being measured.

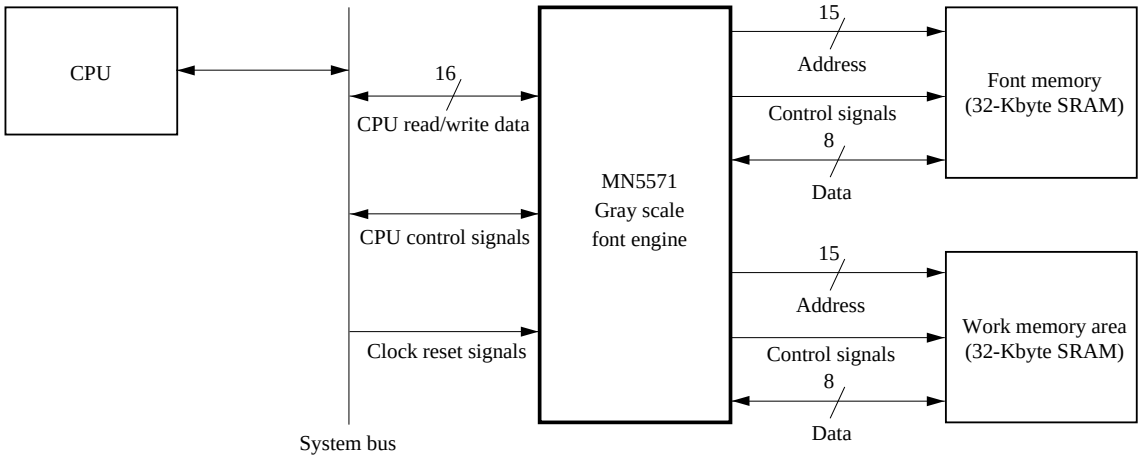
■ Electrical Characteristics (continued)

V_{DD}=3.0 to 3.6V, V_{REF5}=4.75 to 5.25V, V_{SS}=0.00V, f_{TEST}=25MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
TTL level inputs: CPAD0 to CPAD2, CPCK, CPCS, CPRD, CPWR, FREN, RESET, INCTRL						
"H" level input voltage	V_{I5H1}		2.0		V_{REF5}	V
"L" level input voltage	V_{I5L1}		0		0.8	V
Input leakage current	I_{LI5}	V_I=V_{REF5} or V_{SS}			±10	µA
Push-pull outputs: FRAD0 to FRAD14, WRAD0 to WRAD14						
"H" level output voltage	V_{OH}	I_O=– 2.0mA V_I=V_{DD} or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	I_O=2.0mA V_I=V_{DD} or V_{SS}			0.4	V
Push-pull outputs: CPIR, FROE, FRWE, WROE, WRWE, CPWAIT						
"H" level output voltage	V_{OH}	I_O=– 4.0mA V_I=V_{DD} or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	I_O=4.0mA V_I=V_{DD} or V_{SS}			0.4	V
N-channel open drain outputs: FRCS, WRCS						
"L" level output voltage	V_{OL}	I_O=4.0mA V_I=V_{DD} or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_O=High-impedance state V_I=V_{DD} or V_{SS} V_O=V_{DD} or V_{SS}			±5	µA
TTL level I/O: CPDATA0 to CPDATA15, FRDATA0 to FRDATA7, WRDATA0 to WRDATA7						
"H" level input voltage	V_{I5H1}		2.0		V_{REF5}	V
"L" level input voltage	V_{I5L1}		0		0.8	V
"H" level output voltage	V_{OH}	I_O=– 4.0mA V_I=V_{DD} or V_{SS}	2.4			V
"L" level output voltage	V_{OL}	I_O=4.0mA V_I=V_{DD} or V_{SS}			0.4	V
Output leakage current	I_{LO5}	V_O=High-impedance state V_I=V_{REF5} or V_{SS} V_O=V_{REF5} or V_{SS}			±10	µA

■ Application Example

The MN5571 uses two external SRAM devices to achieve high throughput. The one used as a work memory area is always required. The MN5571 can operate without the one used as font memory, but throughput suffers.



■ Package Dimensions (Unit: mm)

LQFP128-P-1818B