MN5520A

Low Power CPU-Controller for PC/AT Computers

■ Overview

The MN5520A is a CPU controller. It is designed for use in combination with the MN5521 I/O peripheral controller and the MN871107 floppy disk drive controller in notebook, subnotebooks, pen-based computers, and other types of PC/AT computers requiring low power consumption.

Note: PC/AT is a registered trademark of International Business Machines Corporation.
i486 is a trademark of Intel Corporation.

■ Features

- CPU support
  - 5 and 3.3-volt versions of SL Enhanced i486SX/DX/DX2/DX4 microprocessors
  - Support for ×1 clock Intel CPUs
  - Operating speeds of 25 or 33 MHz
- Built-in power management functions
  - System management interrupt (SMI) and I/O trapping
  - Suspend/resume function
- Cache support: write through or L1 write back
- DRAM support

  Detection and setup: Automatic detection and setup with software

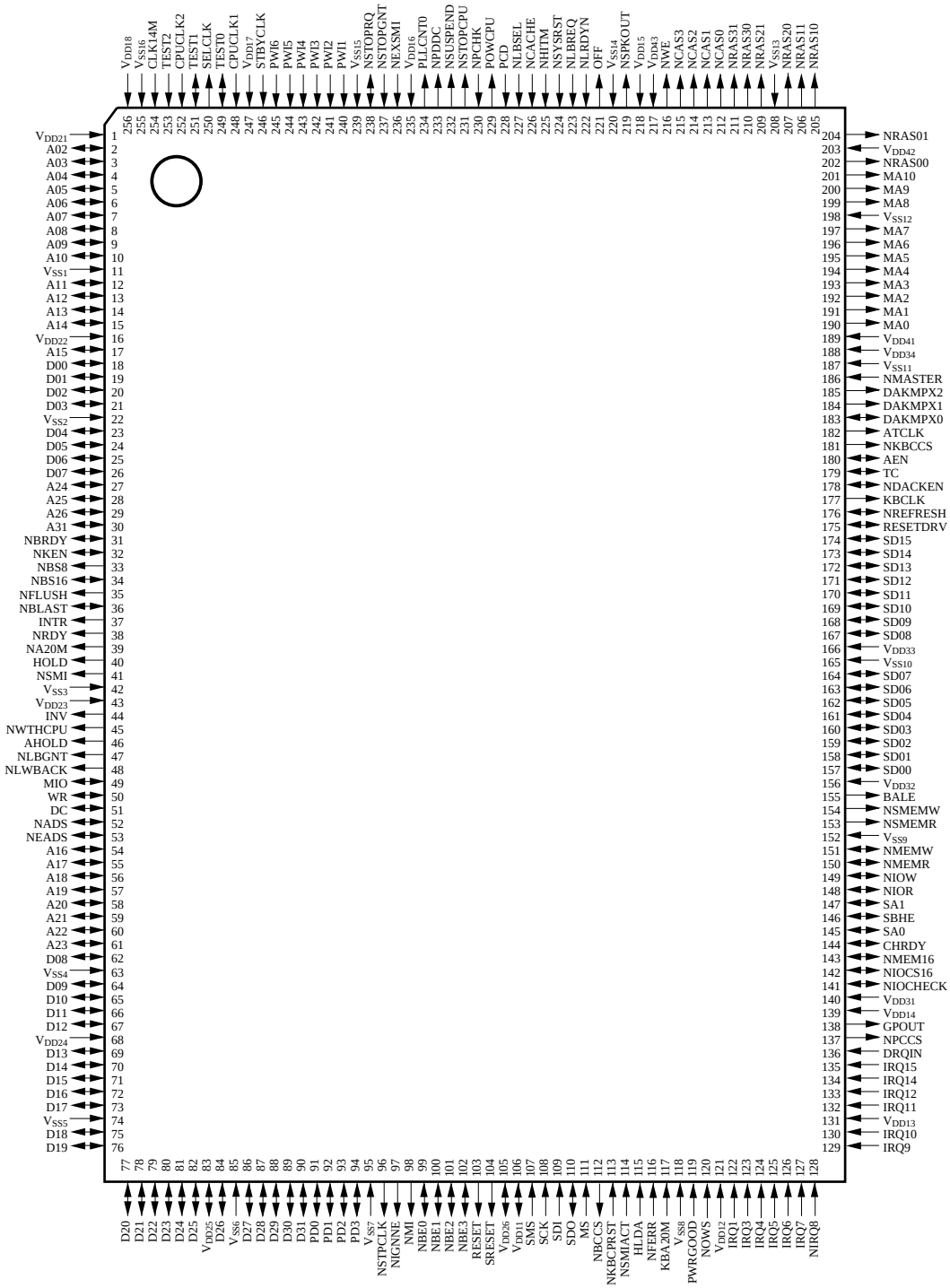
  DRAM
  - Access modes: Interleaved, or no-page interleaved
  - Types: 256 K, 512 K, 1 M, 2 M, 4 M (×1, ×4, ×8, ×16 bits)
  - Refresh type: 512, 1 K, 2 K
  - Suspend refresh modes: Slow refresh or self refresh
  - Access speed: 100 ns or faster DRAM
  - Size: max. 128 megabytes in 4 banks (min. 1 megabyte in 1 bank)
- Built-in PIC: Two 8259-compatible
- Built-in PIT: 8254-compatible
- Built-in DMA controller:

  Two 8237-compatible controllers + LS612
- Support for local bus and ISA bus
- Built-in fast A20 gate control function
- Flash ROM support:
  128-Kbyte to 2-Mbyte (8-bit bus)

■ Applications

- Portable information equipment, data communications equipment, word processors, copiers, handy terminals, sequencers, numerically controlled machinery, game computers, karaoke equipment, car navigation systems, etc.

■ Pin Assignment

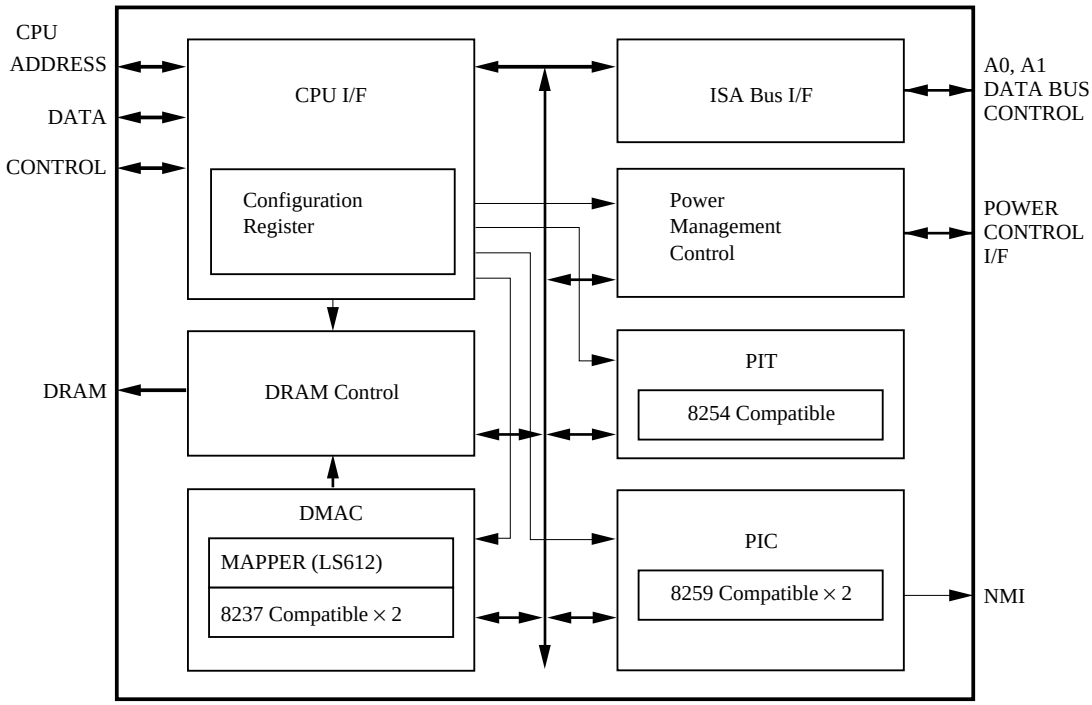


(TOP VIEW)

QFP256-P-2840

Note: Do not leave any of the V_{SS} or V_{DD} pins open.

■ Block Diagram



■ Pin Descriptions

The P column gives the corresponding power supply group number;
the T column, the I/O direction: I/O = bidirectional, I = input, O = output, Tri = tristate,
IS = Schmidt input, OD = open drain.

Pin No.	Symbol	Pin Type		Function Description
		P	T	
CPU bus interface				
2 to 10 12 to 15 ,17 54 to 61 27 to 29 ,30	A02 to 10 A11 to 14 ,A15 A16 to 23 A24 to 26 ,A31	2	I/O	CPU address input (output when DMA)
31	NBRDY			Ready signal output for burst transfers to CPU (input when local bus device is participating in a burst transfer)
32	NKEN		Tri	Cache enable signal to CPU
34	NBS16		I/O	16-bit bus sizing request signal output to CPU (input when local bus master)
35	NFLUSH		O	CPU's internal cache flush signal
36	NBLAST		I/O	End signal input for CPU's burst transfers (output when DMA or ISA bus master)
37	INTR		O	Interrupt request signal to CPU
38	NRDY			Ready signal to CPU
39	NA20M			CPU's A20M terminal control signal
40	HOLD			Hold request signal to CPU
41	NSMI			System management interrupt request signal to CPU
44	INV			Invalidating signal every line for CPU's internal cache (used by CPU supporting write back cache)
45	NWTHCPU			CPU's write back/write through selection signal (CPU's WB/ WT# signal) (used by CPU supporting write back cache)
46	AHOLD			CPU's address line floating control signal
47	NLBGNT			Bus grant signal for local bus master
48	NLWBACK			Signal indicating the write back cycle outbreak to local bus devices
49	MIO		I/O	CPU status signal input "H" level: Memory; "L" level: I/O (output when DMA or ISA bus master)
50	WR			CPU status signal input "H" level: Write; "L" level: Read (output when DMA or ISA bus master)
51	DC			CPU status signal input "H" level: Data; "L" level: Code (output when DMA or ISA bus master)
52	NADS			CPU address strobe signal (output when DMA or ISA bus master)
53	NEADS			Address effective status signal to CPU during cache invalidation cycle (output when device is DMA or ISA bus master)

■ Pin Descriptions (continued)

The P column gives the corresponding power supply group number;
the T column, the I/O direction: I/O = bidirectional, I = input, O = output, Tri = tristate,
IS = Schmidt input, OD = open drain.

Pin No.	Symbol	Pin Type		Function Description
		P	T	
CPU bus interface (continued)				
18 to 21 23 to 26 62 ,64 to 67 69 to 73 75 to 82 84 ,86 to 90	D00 to 03 D04 to 07 D08 ,D09 to 12 D13 to 17 D18 to 25 D26 ,D27 to 31	2	I/O	CPU and memory data
91 to 94	PD0 to 3			Memory parity data
96	NSTPCLK		O	Internal clock stop request signal to CPU
97	NIGNNE			Signal to CPU to ignore floating point errors and continue execution
98	NMI			Non-maskable interrupt to CPU
99 to 102	NBE0 to 3		I/O	Byte enable signal from CPU (output when DMA or ISA bus master)
103	RESET		O	Master reset signal to CPU (asserted by PWRGOOD and NSYSRST)
104	SRESET			Software reset signal to CPU (asserted by register to reset CPU only)
114	NSMIACT	1	I	Signal indicating that the CPU has detected the system management interrupt (SMI) signal and switched to SMI mode
115	HLDA			CPU's hold acknowledge request signal
116	NFERR			Signal from CPU indicating floating point error
222	NLRDYN			Signal from local device indicating end of cycle
223	NLBREQ			Signal from local device requesting local bus control
225	NHITM			Signal indicating hit the line marked as write pending in the CPU's internal cache
226	NCACHE			Signal indicating that current CPU cycle is cacheable (used by CPU supporting write back cache)
227	NLBSEL			Select signal from local device (Local devices should generate this signal by address decoding only.)
228	PCD			Page descriptor table cache disable status signal from CPU in paging mode
230	NPCHK			Parity check status signal from CPU

■ Pin Descriptions (continued)

The P column gives the corresponding power supply group number;
the T column, the I/O direction: I/O = bidirectional, I = input, O = output, Tri = tristate,
IS = Schmidt input, OD = open drain.

Pin No.	Symbol	Pin Type		Function Description
		P	T	
DRAM interface				
190 to 197 199 to 201	MA0 to 7 MA8 to 10	4	O	DRAM multiplex address
202 ,204	NRAS00 ,01			RAS signal for DRAM bank 0
205 ,206	NRAS10 ,11			RAS signal for DRAM bank 1
207 ,209	NRAS20 ,21			RAS signal for DRAM bank 2
210 ,211	NRAS30 ,31			RAS signal for DRAM bank 3
212 to 215	NCAS0 to 3			CAS signal for DRAM
216	NWE			DRAM write enable signal
Power management interface				
112	NBCCS	1	O	Chip select signal for external devices using selectable port access
137	NPCCS			Write signal ("H" level pulse) to external register
138	GPOUT			General-purpose output port signal
221	OFF		OD	Signal indicating this device is in its OFF state
229	POWCPU		O	Power supply control signal for CPU ("L" level during normal operation)
231	NSTOPCPU			Signal indicating that CPU has stopped (is in DOZE mode)
232	NSUSPEND			Signal indicating that CPU is in suspended state
233	NPDDC			Signal for switching the power supply (DC-DC converter) to power-saving mode
234	PLLCNTO			Signal controlling “ON” or “OFF” of oscillation for external phase-locked loop "H" level: ON; "L" level: OFF
236	NEXSMI		IS	External system management interrupt (SMI) input for power management
240 to 245	PWI1 to 6			Power status signal input for power management
237	NSTOPGNT		I	Acknowledge signal responding to NSTOPRQ request
238	NSTOPRQ		O	Signal indicating request to suspend outward
ISA bus interface				
120	NOWS	1	I	Signal for ISA bus cycle to zero wait states
122	IRQ1		IS	Interrupt request signal from keyboard
123 to 127 129 to 130 132 to 133 134 to 135	IRQ3 to 7 IRQ9 to 10 IRQ11 to 12 IRQ14 to 15			Interrupt request signals from ISA bus
136	DRQIN			DMA channel-2 request signal (In the multiplex mode, this input represents multiplexed inputs from multiple channels.)

■ Pin Descriptions (continued)

The P column gives the corresponding power supply group number;
the T column, the I/O direction: I/O = bidirectional, I = input, O = output, Tri = tristate,
IS = Schmidt input, OD = open drain.

Pin No.	Symbol	Pin Type		Function Description
		P	T	
ISA bus interface (continued)				
141	NIOCHECK	3	I/O	ISA bus parity check signal input
142	NIOCS16			Signal input indicating 16-bit data width for ISA bus I/O access
143	NMEM16			Signal input indicating 16-bit data width for ISA bus memory access (output when DMA or ISA bus master)
144	CHRDY			ISA bus wait signal (Drive "L" when ISA bus master.)
145	SA0			ISA bus address 0 signal output (Input pin when ISA bus master.)
146	SBHE			ISA bus byte-high-enable signal output (Input pin when ISA bus master.)
147	SA1			ISA bus address-1 signal output (Input pin when ISA bus master.)
148	NIOR			I/O read command signal output (Input pin when ISA bus master.)
149	NIOW			I/O read command signal output (Input pin when ISA bus master.)
150	NMEMR			Memory read signal output (Input pin when ISA bus master.)
151	NMEMW			Memory write signal output (Input pin when ISA bus master.)
153	NSMEMR		Tri	Memory read signal (asserted for addresses in 0 to 1 megabyte)
154	NSMEMW			Memory write signal (asserted for addresses in 0 to 1 megabyte)
155	BALE			Address latch signal (The address is valid at the falling edge of this signal.)
157 to 164	SD00 to 07		I/O	ISA data bus signal
167 to 169 170 to 172	SD08 to 10 SD11 to 13			ISA data bus signal (During ROM access, these are the upper bits of the address.)
173	SD14			ISA data bus signal (During ROM access, this is the read signal output.)
174	SD15			ISA data bus signal (During ROM access, this is the write signal output.)
175	RSETDRV			ISA bus-reset signal output (asserted for PWRGOOD and NSYSRST signals, and when waking from the resume mode)
176	NREFRESH			ISA bus refresh signal (Input pin when ISA bus master.)
178	NDACKEN			DMA channel-2 request acknowledge signal (In the multiplex mode, this is the NDACKn decode control output.)

■ Pin Descriptions (continued)

The P column gives the corresponding power supply group number;
the T column, the I/O direction: I/O = bidirectional, I = input, O = output, Tri = tristate,
IS = Schmidt input, OD = open drain.

Pin No.	Symbol	Pin Type		Function Description
		P	T	
ISA bus interface (continued)				
179	TC	3	I/O	DMA transfer terminal count signal output ("H" level when the final count is reached)
180	AEN			Signal output indicating DMA cycle in progress ("H" level during DMA transfer)
182	ATCLK		O	ISA bus clock signal (8.3 MHz clock signal obtained by dividing frequency of CPUCLK2 signal by 6 or 8)
183	DAKMPXO		I/O	DMA request signal input supporting channel selection (DRQx) (In the multiplex mode, this is MPX code output "0.")
184	DAKMPX1		Tri	DMA request acknowledge signal (In the multiplex mode, this is MPX code output "1.")
185	DAKMPX2			Chip select signal for port 80H (In the multiplex mode, this is MPX code output "2.")
186	NMASTER		I/O	Bus request signal input from external bus master
ROM and keyboard controller interface				
113	NKBCPRST	1	IS	CPU reset (SRESET) signal from keyboard controller
117	KBA20M			CPU address-A20 mask-signal from keyboard controller
177	KBCLK	3	O	Keyboard controller clock (divided frequency of ATCLK by 2)
181	NKBCCS			Keyboard-access-port chip-select signal and ROM-access chip-select signal
Clock interface				
246	STBYCLK	1	IS	Operating clock (32.768 kHz) input at start-up and suspended operation
254	CLK14M			Timer-counter clock (14.31818 MHz) signal input
248	CPUCLK1		I	× 1 clock signal input (25/33 MHz: same as CPU clock input)
252	CPUCLK2			× 2 clock signal input (50/66 MHz)
250	SELCLK		O	Signal indicating relationship between CPUCLK2 and ATCLK
Other interfaces				
119	PWRGOOD	1	IS	Power supply reset input ("L" level triggers master reset.)
128	NIRQ8			Interrupt request signal for real-time clock
219	NSPKOUT		OD	Speaker output signal
224	NSYSRST		I	System reset signal (Asserting this signal asserts RESET and RESETDRV.)
249, 251	TEST0 to 1		I/O	Test signal inputs (Normally keep these at "L" level.)
253	TEST2		I	

■ Pin Descriptions (continued)

The P column gives the corresponding power supply group number;
the T column, the I/O direction: I/O = bidirectional, I = input, O = output, Tri = tristate,
IS = Schmidt input, OD = open drain.

Pin No.	Symbol	Pin Type		Function Description
		P	T	
Other interfaces (continued)				
107	SMS	1	IS	Test signal inputs (Normally keep these at "L" level.)
108	SCK			
109	SDI			
111	MS			
110	SD0		I/O	Test signal output
33	NBS8	2	I/O	Test signal output

Power supply pin specifications

Pin No.	Symbol	Function Description	Power Supply Voltage specifications
11 ,22 ,42 ,63 ,74 ,85 ,95 , 118 ,152 ,165 ,187 ,198 , 208 ,220 ,239 ,255	$V_{SS1\ to\ 16}$	GND	0V
106 ,121 ,131 ,139 ,218 , 235 ,247 ,256	$V_{DD11\ to\ 18}$	Power supply for core and input pin interfaces V_{DD1} group	3.3V
1 ,16 ,43 ,68 ,83 ,105	$V_{DD21\ to\ 26}$	Power supply for CPU interface V_{DD2} group	5.0V/3.3V
140 ,156 ,166 ,188	$V_{DD31\ to\ 34}$	Power supply for ISA bus interface V_{DD3} group	5.0V/3.3V
189 ,203 ,217	$V_{DD41\ to\ 43}$	Power supply for memory interface V_{DD4} group	5.0V/3.3V

■ Absolute Maximum Ratings

V_{SS}=0V

Parameter		Symbol	Ratings	Unit
Power supply voltage		V_{DD}	– 0.3 to 6.5	V
Input pin voltage	Normal cells with V_{DD} side input and without protective diode	V_I	– 0.3 to V_{DD} + 0.3 V_{SS} – 0.3 to +5.8	V
Output pin voltage		V_O	– 0.3 to V_{DD} + 0.3	V
Output current		I_{OL}	+12	mA
Output current		I_{OH}	–12	mA
Power dissipation		P_D	1350	mW
Operating ambient temperature		T_{opr}	0 to 70	˚C
Storage temperature		T_{stg}	–55 to 150	˚C

Notes

1: The above ratings represent the maximum values that may be applied without damaging the chip, not the limits for guaranteed operation.

2: Directly connect all V_{DD} pins to external power supplies and all V_{SS} pins to the ground.

3: V_{DD} pins are divided into four groups. (See timing charts.)

■ Recommended Operating Conditions

V_{SS}=0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply voltage (1)	V_{DD1}	Normal mode	3.0	3.3	3.6	V
Power supply voltage (2)	V_{DD2} to V_{DD4}	Normal mode	3.0	3.3	3.6	V
Ambient temperature	Ta		0		70	˚C
Rise time for input	t_r		0		150	ns
Full time for input	t_f		0		150	

Notes

V_{DD1}: Power supply for internal circuits and I/O buffer block

V_{DD2} to V_{DD4}: Power supplies restricted to specific I/O buffer blocks whose power supply is separated each other.

■ Input/Output Capacitance

Item	Symbol	Conditions	min	typ	max	Unit
Input pins	C_{IN}	V_{DD1} to V_{DD4}=V_I=0V f=1MHz, Ta=25˚C		7	15	pF
Output pins	C_{OUT}			7	15	pF
I/O pins	$C_{I/O}$			7	15	pF

■ Electrical Characteristics

$V_{DD1\ to\ 4}$=3.0 to 3.6V, V_{SS}=0.00V, f_{TEST}=40MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent supply current	I_{DDS}	$V_{DD1\ to\ 4}$=3.60V V_{SS}=0V Measured at pins $V_{DD1\ to\ 4}$			50	µA
Operating supply current	I_{DDO} f=40MHz	$V_I=V_{DD}$ *1 or V_{SS} $V_{DD1\ to\ 4}$=3.3V Outputs open V_{SS}=0V Measured at pins $V_{DD1\ to\ 4}$		40	100	mA
Low-voltage TTL level inputs with protective diodes on V_{DD} input side removed: V_{DD1} group pins TEST2						
"H" level input voltage	V_{IH1}	$V_{DD}=V_{DD1}$	2.0		V_{DD}	V
"L" level input voltage	V_{IL1}	$V_{DD}=V_{DD1}$	0		0.4	V
Input leakage current	I_{LI}	$V_I=V_{DD1}$ or V_{SS}			±5	µA
Low-voltage TTL level inputs with input penetration current protection on, protective diodes at V_{DD} input side removed: V_{DD1} group pins NOWS, PCD, HLDA, NFERR, NPCHK, CPUCLK1, CPUCLK2, NLBREQ, NLBSEL, NLRDYIN, NSMIACT, NSYSRST, NSTOPGNT						
"H" level input voltage	V_{IH1}	$V_{DD}=V_{DD1}$	2.0		V_{DD}	V
"L" level input voltage	V_{IL1}	$V_{DD}=V_{DD1}$	0		0.4	V
Input leakage current	I_{LI}	$V_I=V_{DD1}$ or V_{SS}			±5	µA
Low-voltage TTL level inputs: *2 V_{DD1} group pins NHITM, NCACHE						
"H" level input voltage	V_{IH1}	$V_{DD}=V_{DD1}$	2.0		V_{DD}	V
"L" level input voltage	V_{IL1}	$V_{DD}=V_{DD1}$	0		0.4	V
Pull-down resistance	R_{PD2}	V_I=3.3V	58	175	520	kΩ
Input leakage current	I_{LI}	$V_I=V_{DD1}$ or V_{SS}			±10	µA

Notes

*1: For all four power supply groups: $V_I = V_{DD1}$, $V_I = V_{DD2}$, $V_I = V_{DD3}$, and $V_I = V_{DD4}$.

*2: With penetration current protection on, protective diodes at V_{DD} input side removed, and pull-down resistance controller.

■ Electrical Characteristics (continued)

$V_{DD1\ to\ 4}$=3.0 to 3.6V, V_{SS}=0.00V, f_{TEST}=40MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
Low-voltage TTL level inputs with Schmidt circuit, penetration current protection on, protective diodes on V_{DD} input-side removed:						
V_{DD1} group pins CLK14M, KBA20M, PWI1 to PWI6, NIRQ8, NEXSMI, NKBCPRST						
Input threshold voltage	V_t	V_{DD}=V_{DD1}	0.7		2.2	V
Input leakage current	I_{LI}	V_I=V_{DD1} or V_{SS}			±5	µA
Low-voltage TTL level inputs with Schmidt circuit, penetration current protection on, pull-down resistance control on, and protective diodes on V_{DD} input-side removed:						
V_{DD1} group pins IRQ1, IRQ3 to IRQ7, IRQ9 to IRQ12, IRQ14 to IRQ15, TCK, TDI, TMS, DRQIN						
Input threshold voltage	V_t	V_{DD}=V_{DD1}	0.7		2.2	V
Pull-down resistance	R_{PD2}	V_I=V_{DD} V_{DD}=3.3V	58	175	520	kΩ
Input leakage current	I_{LI}	V_I=V_{DD1} or V_{SS}			±10	µA
Push-pull outputs for 5-volt interfaces (with level converters): V_{DD2} group pins NRDY, NLWBACK						
V_{DD4} group pins MA0 to MA10, NWE, NCAS0 to NCAS3, NRAS00 to NRAS01, NRAS10 to NRAS11, NRAS20 to NRAS21, NRAS30 to NRAS31						
"H" level output voltage	V_{OH}	V_{DD}=V_{DD2} or V_{DD4} I_O=–4.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD2} or V_{DD4} I_O=4.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–24		24	mA
Low-voltage TTL level inputs with Schmidt input and protective diodes on V_{DD} input side removed:						
V_{DD1} group pins PWRGOOD, STBYCLK						
Input threshold voltage	V_t	V_{DD}=V_{DD1}	0.7		2.2	V
Input leakage current	I_{LI}	V_I=V_{DD1} or V_{SS}			±5	µA
Low-voltage TTL level inputs with Schmidt input, pull-down resistance control on, and protective diodes on V_{DD} input side removed:						
V_{DD1} group pins MS						
Input threshold voltage	V_t	V_{DD}=V_{DD1}	0.7		2.2	V
Input leakage current	I_{LI}	V_I=V_{DD1} or V_{SS}			±10	µA

Note*1: For all four power supply groups: $V_I = V_{DD1}$, $V_I = V_{DD2}$, $V_I = V_{DD3}$, and $V_I = V_{DD4}$.

■ Electrical Characteristics (continued)

$V_{DD1\ to\ 4}$=3.0 to 3.6V, V_{SS}=0.00V, f_{TEST}=40MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
Push-pull outputs:						
V_{DD1} group pins GPOUT, NBCCS, NPCCS, NPDDC, PLLCNT0, POWCPU, SELCLK, NSTOPCPU, NSUSPEND						
"H" level output voltage	V_{OH}	V_{DD}=V_{DD1} I_O=–2.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD1} I_O=2.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–12		12	mA
Push-pull outputs for 5-volt interfaces (with level converters):						
V_{DD2} group pins NA20M, INV, NMI, HOLD, INTR, NSMI, AHOLD, NFLUSH, NIGNNE, NLBGNT, NSTPCLK, NWTHCPU, RESET, SRESET						
V_{DD3} group pins ATCLK, KBCLK, NKBCCS						
"H" level output voltage	V_{OH}	V_{DD}=V_{DD2} or V_{DD3} I_O=–2.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD2} or V_{DD3} I_O=2.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–12		12	mA
Tristate outputs for 5-volt interfaces (with level converters):						
V_{DD3} group pins DAKMPX1 to DAKMPX2						
"H" level output voltage	V_{OH}	V_{DD}=V_{DD3} I_O=–2.0mA V_I=V_{DD} or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD3} I_O=2.0mA V_I=V_{DD} or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_I=V_{DD3} or V_{SS}			±5	µA
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–12		12	mA

Note*1: For all four power supply groups: $V_I = V_{DD1}$, $V_I = V_{DD2}$, $V_I = V_{DD3}$, and $V_I = V_{DD4}$.

■ Electrical Characteristics (continued)

$V_{DD1\ to\ 4}$=3.0 to 3.6V, V_{SS}=0.00V, f_{TEST}=40MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
Tristate outputs: *2	V_{DD2} group pins NKEN V_{DD3} group pins BALE, NSMEMR, NSMEMW					
Pull-up resistance	R_{PU3}	V_I=0.0V V_{DD}=3.3V	58	175	520	kΩ
"H" level output voltage	V_{OH}	V_{DD}=V_{DD2} or V_{DD3} I_O=–6.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD2} or V_{DD3} I_O=6.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_I=V_{DD2} or V_{DD3} or V_{SS}			±10	µA
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–36		36	mA
N-channel open drain outputs with built-in pull-down resistors and protective diodes on V_{DD} input-side removed: V_{DD1} group pins OFF, NSPKOUT						
"L" level output voltage	V_{OL}	V_{DD}=V_{DD1} I_O=12.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_I=V_{DD1} or V_{SS}			±5	µA
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–72		72	mA
CMOS level I/O: V_{DD1} group pins NSTOPRQ						
"H" level input voltage	V_{IH2}	V_{DD}=V_{DD1}	V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}	V_{DD}=V_{DD1}	0		V_{DD} × 0.3	V
"H" level output voltage	V_{OH}	V_{DD}=V_{DD1} I_O=–2.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD1} I_O=2.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_I=V_{DD1} or V_{SS}			±5	µA
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–12		12	mA

Notes

*1: For all four power supply groups: V_I = V_{DD1}, V_I = V_{DD2}, V_I = V_{DD3}, and V_I = V_{DD4}.

*2: With slew rate and pull-up resistor controller, and support for 5 volt interfaces (with level converters)

■ Electrical Characteristics (continued)

$V_{DD1\ to\ 4}$=3.0 to 3.6V, V_{SS}=0.00V, f_{TEST}=40MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
CMOS level I/O (used only for input): V_{DD1} group pins TEST0 to TEST1						
"H" level input voltage	V_{IH2}	V_{DD}=V_{DD1}	V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}	V_{DD}=V_{DD1}	0		V_{DD} × 0.3	V
CMOS level I/O (used only for output): V_{DD1} group pins TDO						
"H" level output voltage	V_{OH}	V_{DD}=V_{DD1} I_O=–2.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD1} I_O=2.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Peak output voltage	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–12		12	mA
CMOS level I/O: *2 V_{DD2} group pins A02 to A26, A31, D00 to D31, DC, PD0 to PD3, WR, MIO, NBE0 to NBE3, NBS16, NADS, NBRDY, NEADS, NBLAST V_{DD3} group pins SA0 to SA1, SD00 to SD15, SBHE, NIOR, NIOW, NMEM16, CHRDY, NMEMR, NMEMW, NREFRESH						
"H" level input voltage	V_{IH2}	V_{DD}=V_{DD2} or V_{DD3}	V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}	V_{DD}=V_{DD2} or V_{DD3}	0		V_{DD} × 0.2	V
Pull-up resistance	R_{PU3}	V_I=0.0V V_{DD}=3.3V	58	175	520	kΩ
"H" level output voltage	V_{OH}	V_{DD}=V_{DD2} or V_{DD3} IO=–4.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD2} or V_{DD3} I_O=4.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_I=V_{DD2} or V_{DD3} or V_{SS}			±10	µA
Peak output voltage	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–24		24	mA
CMOS level I/O: *3 V_{DD3} group pins NIOCS16						
"H" level input voltage	V_{IH2}	V_{DD}=V_{DD2} or V_{DD3}	V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}	V_{DD}=V_{DD2} or V_{DD3}	0		V_{DD} × 0.2	V
Pull-up resistance	R_{PU3}	V_I=0.0V V_{DD}=3.3V	58	175	520	kΩ

Notes

*1: For all four power supply groups: $V_I = V_{DD1}$, $V_I = V_{DD2}$, $V_I = V_{DD3}$, and $V_I = V_{DD4}$.

*2: With penetration current protection on, slew rate and pull-up resistance controller, and support for 5-volt interfaces (with level converters)

*3: With input penetration current protector and pull-up resistance controller.

■ Electrical Characteristics (continued)

$V_{DD1\ to\ 4}$=3.0 to 3.6V, V_{SS}=0.00V, f_{TEST}=40MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
CMOS level I/O (used only for output): *2 V_{DD3} group pin RESETDRV						
Pull-up resistance	R_{PU3}	V_I=0.0V V_{DD}=3.3V	58	175	520	kΩ
"H" level output voltage	V_{OH}	V_{DD}=V_{DD2} or V_{DD3} I_O=–4.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD2} or V_{DD3} I_O=4.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_I=V_{DD2} or V_{DD3} or V_{SS}			±10	µA
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–24		24	mA
CMOS level I/O: *3 V_{DD2} group pin NBS8 V_{DD2} group pin DAKMPX0						
"H" level input voltage	V_{IH2}	V_{DD}=V_{DD2} or V_{DD3}	V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}	V_{DD}=V_{DD2} or V_{DD3}	0		V_{DD} × 0.2	V
"H" level output voltage	V_{OH}	V_{DD}=V_{DD2} or V_{DD3} I_O=–2.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD2} or V_{DD3} I_O=2.0mA V_I=V_{DD} *1 or V_{SS}			0.4	V
Output leakage current	I_{LO}	V_I=V_{DD2} or V_{DD3} or V_{SS}			±10	µA
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–12		12	mA
CMOS level I/O (used for input only): *4 V_{DD3} group pins NMASTER, NIOCHECK						
"H" level input voltage	V_{IH2}	V_{DD}=V_{DD2} or V_{DD3}	V_{DD} × 0.7		V_{DD}	V
"L" level input voltage	V_{IL2}	V_{DD}=V_{DD2} or V_{DD3}	0		V_{DD} × 0.2	V
Pull-up resistance	R_{PU3}	V_I=0.0V V_{DD}=3.3V	58	175	520	kΩ

Notes

*1: For all four power supply groups: $V_I = V_{DD1}$, $V_I = V_{DD2}$, $V_I = V_{DD3}$, and $V_I = V_{DD4}$.

*2: With slew rate and pull-up resistance controller, and support for 5-volt interfaces (with level converters)

*3: With input penetration current protector, slew rate controller, and support for 5-volt interfaces (with level converters)

*4: With input penetration current protection on, slew rate and pull-up resistance controller.

■ Electrical Characteristics (continued)

$V_{DD1\ to\ 4}$=3.0 to 3.6V, V_{SS}=0.00V, f_{TEST}=40MHz, Ta=0 to 70˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
CMOS level I/O (used for output only): *2 V_{DD3} group pins TC, AEN, XDACKEN						
Pull-up resistance	R_{PU3}	V_I=0.0V V_{DD}=3.3V	58	175	520	kΩ
"H" level output voltage	V_{OH}	V_{DD}=V_{DD2} or V_{DD3} I_O=–2.0mA V_I=V_{DD} *1 or V_{SS}	V_{DD}– 0.6			V
"L" level output voltage	V_{OL}	V_{DD}=V_{DD2} or V_{DD3} I_O=2.0mA V_I=V_{DD} *1 or V_{SS}	0		0.4	V
Output leakage current	I_{LO}	V_I=V_{DD2} or V_{DD3} or V_{SS}			±10	µA
Peak output current	I_O (Peak)	Absolute maximum rating (not guaranteed operating value)	–12		12	mA

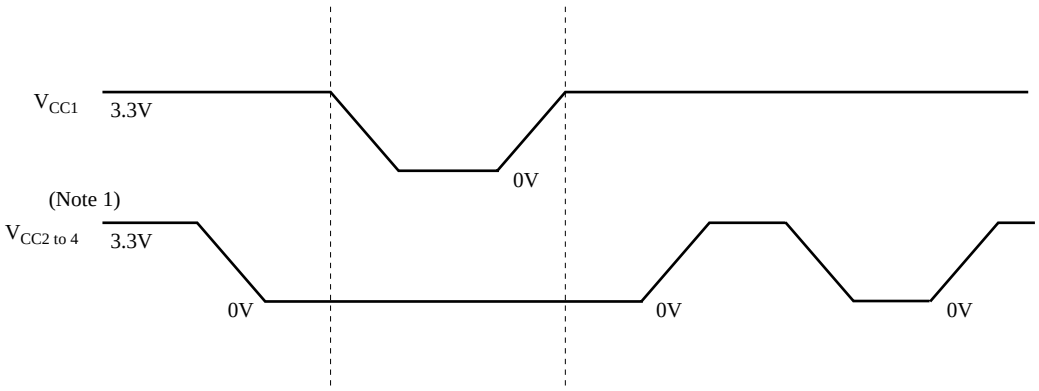
Notes

*1: For all four power supply groups: $V_I = V_{DD1}$, $V_I = V_{DD2}$, $V_I = V_{DD3}$, and $V_I = V_{DD4}$.

*2: With slew rate and pull-up resistance controller, and support for 5-volt interfaces (with level converters).

Note that output pins (including bidirectional pins configured for output) can sometimes under- or overshoot for light loads. If this arises, take measures with a damping resistor or anything.

■ Timing Chart

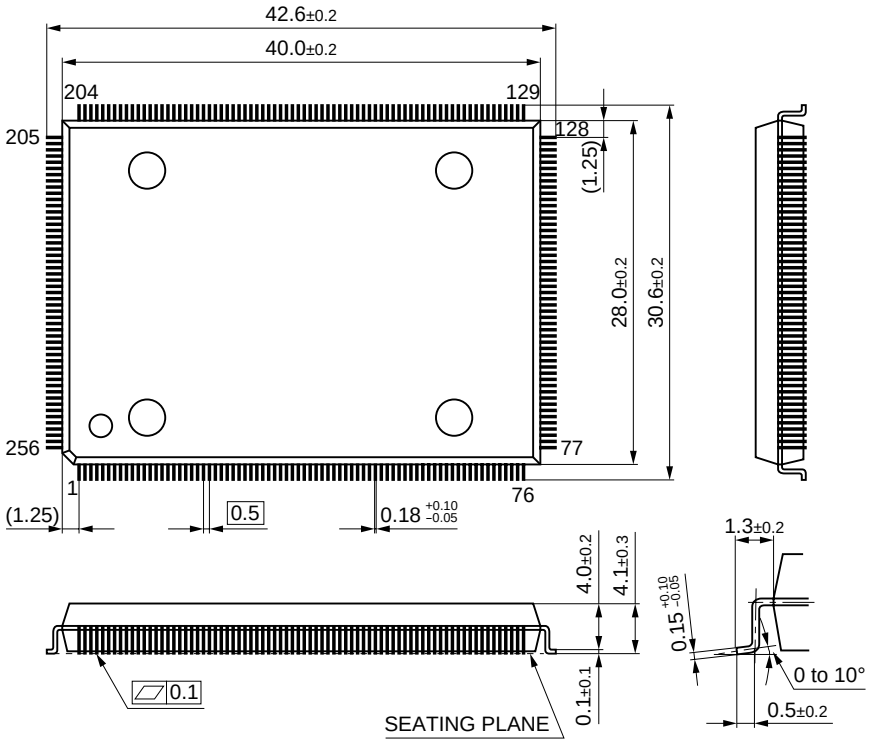


Note 1. Because V_{DD2} to V_{DD4} are separate power supplies, it is possible to have independent control over V_{CC2} to V_{CC4} when V_{CC1} is ON.

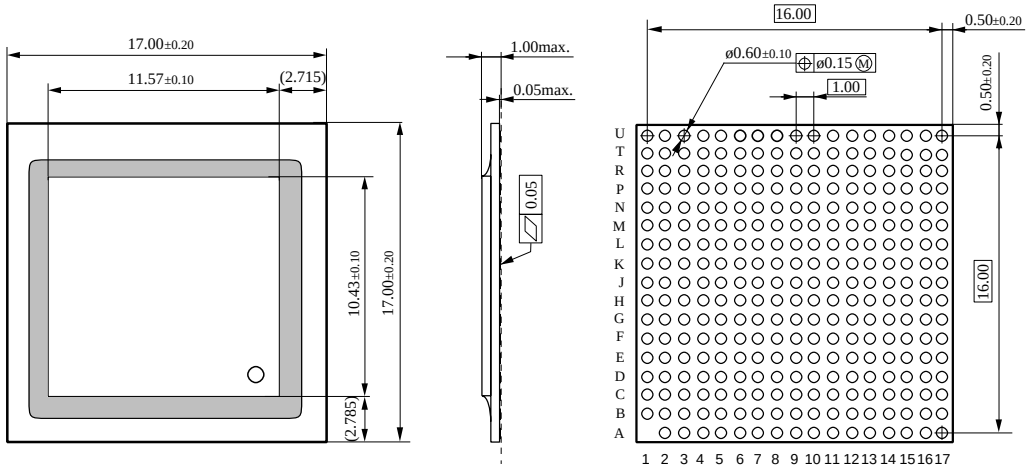
Never leave V_{DD} and V_{SS} pins open.

■ Package Dimensions (Unit: mm)

QFP256-P-2840



LGA288-C-1717 (MN5220A)



TOP VIEW

BOTTOM VIEW