MN3885S

NTSC-Compatible CCD Video Signal Delay Element

■ Overview

The MN3885S is a CCD signal delay element for video signal processing applications.

It contains such components as a shift register clock driver, charge I/O blocks, two CCD delay elements, a clamp bias circuit, resampling output amplifiers, and booster circuits.

The MN3885S samples the input using the supplied clock signal with a frequency 7.15909 MHz of twice the NTSC color signal subcarrier frequency, and after adding in the attached filter delay, produces independent delays of 1 H (the horizontal scan period) each for the two lines.

■ Features

- Single 5.0 V power supply
- Single chip combining luminance signal delay line and delay line for color signal converted to the low frequency.
- Low EMI levels from clock during driving

■ Applications

- VCRs, Video cameras

■ Structure and Operation

The MN3885S consists of the operational blocks shown in the block diagram. The shift register has the structure shown in the supplementary diagram.

- Shift register clock driver

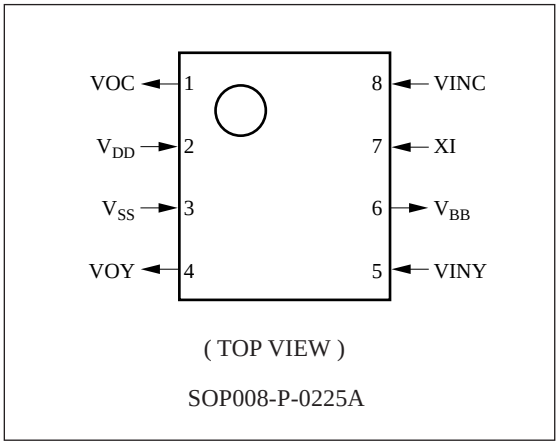
This block generates two transfer clock signals, ø1 and ø2, synchronized with the 7.15909 MHz input clock signal.

It also generates the sampling clock signals øS and øS', resampling clock signal øSH, and reset clock signal øR based on the timing control.

- Charge Input blocks

These blocks alter the analog input signals from the VINC and VINY pins on their way to the shift registers. One adds the bias voltage specified with the bias circuit to the analog signal from the VINC pin. The other applies an "L" level clamp voltage from the clamp circuit to the analog signal from the VINY pin.

■ Pin Assignment



(TOP VIEW)

SOP008-P-0225A

- Analog shift registers

These blocks sample the shift register input signals with the sampling clock, and convert the results to charges, and use transfer clocks ø1 and ø2 to transfer the results to the following block.

- Charge detection blocks

These convert the signal charges from the final stage of the analog shift registers into voltage signals.

- Resampling output amplifiers

In the output stage of this blocks, the voltage signal is executed Sample-and-Hold by resampling, and is outputted at signal output pin of VOC (1-pin) and VOY (4-pin).

- Bias circuit

This circuit applies a bias voltage to the analog signal from VINC (pin 8) to optimize it for the shift register.

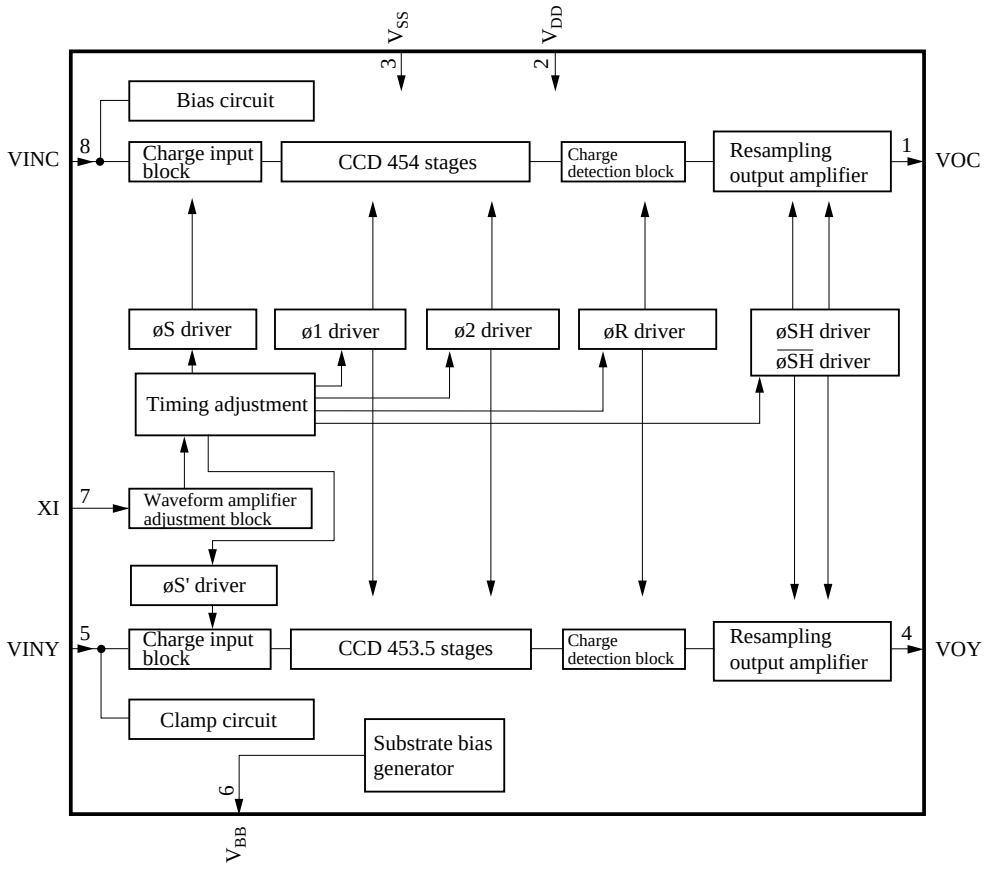
- Clamp circuit

This circuit applies an "L" level clamp to the analog signal from VINY (pin 5) to optimize it for the shift register.

- Booster circuits

These generate reset drain voltages.

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Pin Name	Remarks
1	VOC	Signal output (C)	
2	V_{DD}	Power supply	
3	V_{SS}	Ground	
4	VOY	Signal output (Y)	
5	VINY	Signal input (Y)	
6	V_{BB}	Substrate connection	Negative voltage pin
7	XI	Clock input	
8	VINC	Signal input (C)	

■ Operating Conditions

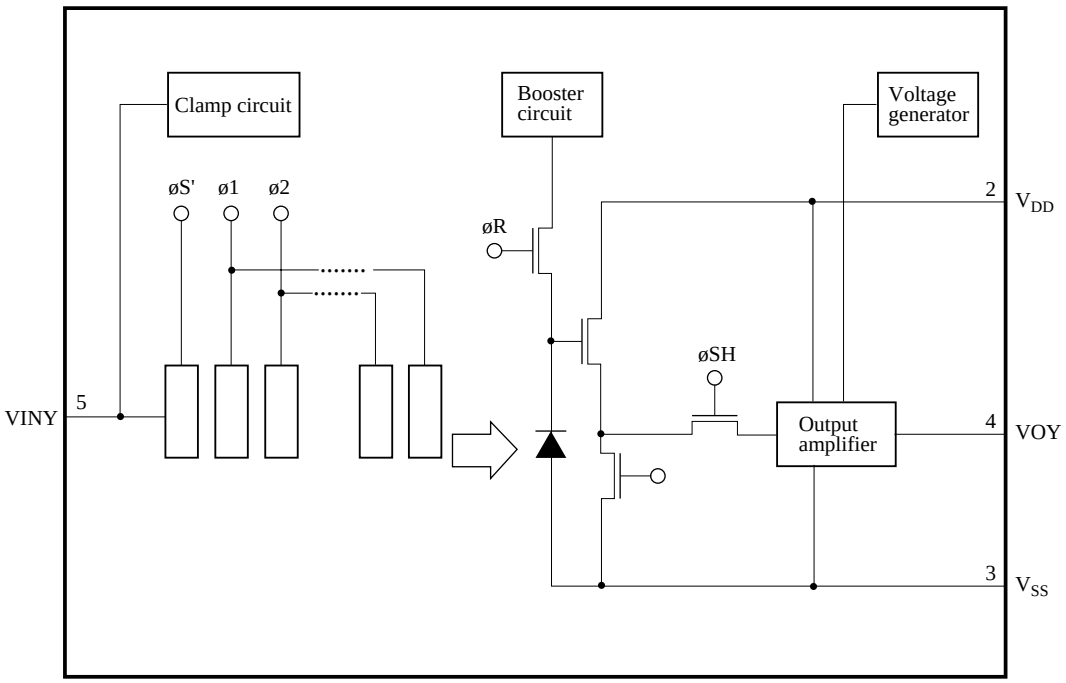
Parameter	Symbol	min	typ	max	Unit
Power supply	V_{DD}	4.75	5.00	5.25	V
Input clock frequency	f_{ck}		7.15909		MHz
Input clock amplitude (sine wave)	v_{ck}	0.2	0.3	1.5	V_{P-P}
Ambient temperature	Ta	–20		60	˚C

■ Electrical Characteristics

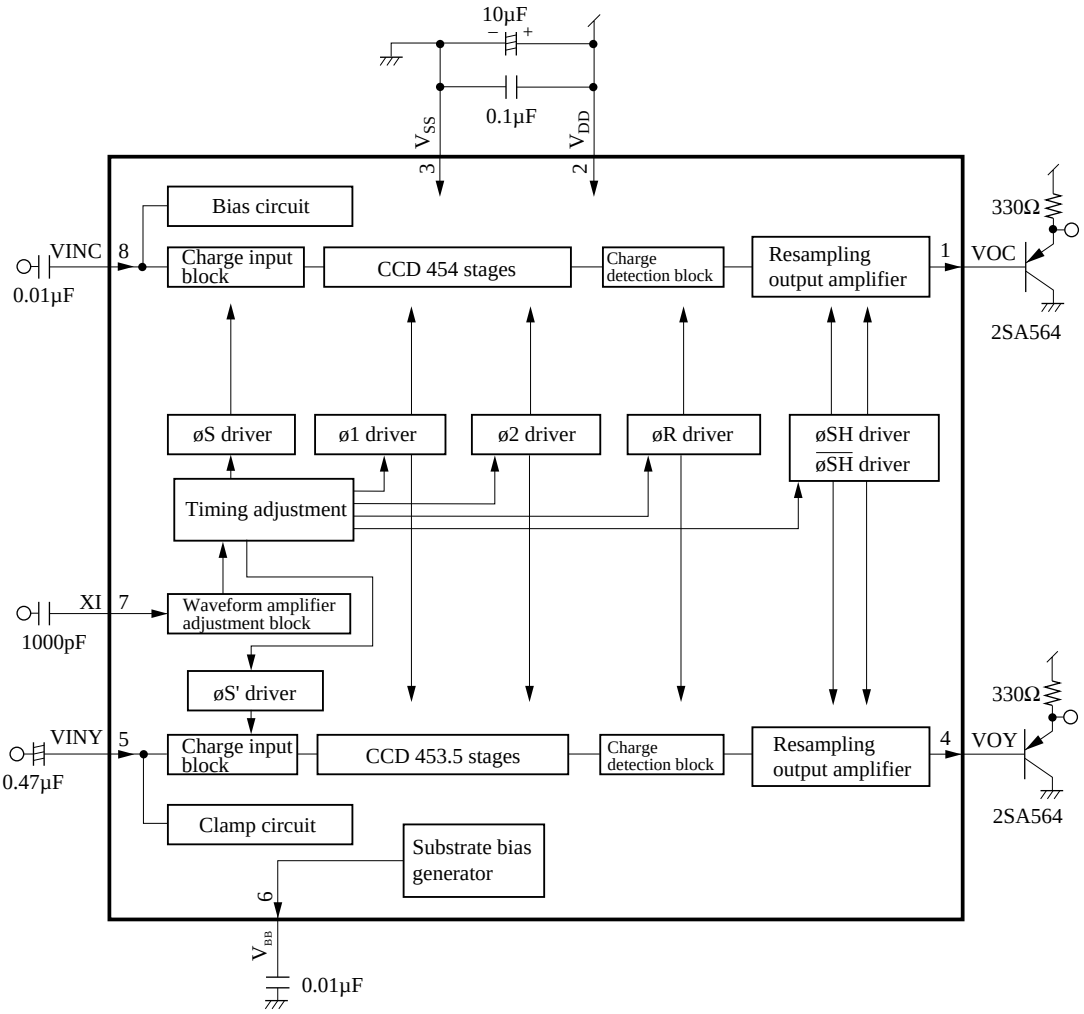
V_{DD}=5.0V, V_{ck}=0.3V_{P-P} (sine wave), V_{in}=0.5V_{P-P} (sine wave), f_{ck}=7.15909MHz, Ta=25˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply voltage	I_{DD}			18	36	mA
Signal bandwidth (Y signal)	BWY	–3 dB for 200 kHz value	1.8	2.8		MHz
Signal bandwidth (C signal)	BWC	–3 dB for 200 kHz value	1.8	2.8		
Insertion gain (Y signal)	IGY	f_{sig}=200kHz	0.0	3.0	6.0	dB
Insertion gain (C signal)	IGC	f_{sig}=200kHz	–1.0	2.0	5.0	
Total harmonic distortion	THD	f_{sig}=200kHz		1.0	4.5	%
Signal-to-noise ratio	S/N	Signal output (V_{p-p})/noise output (rms)	48	56		dB
Clock leak	NC	7.16 MHz components for both Y and C signals		–30	–10	dB
Crosstalk	CT	f_{sig}=200kHz		–50	–35	dB
Delay (Y signal)	τ_{DY}			63.38		µs
Delay (C signal)	τ_{DC}			63.46		
VO pin output impedance	Z_{OY}			0.5	0.9	kΩ
	Z_{OC}			0.5	0.9	
Input bias voltage	V_{BIN}	Applied to input from C signal input pin		2.86		V
Input clamp voltage	V_{CLIN}	Applied to input from Y signal input pin		2.70		V
Output bias voltage	V_{BO}	Applied to output from C signal output pin		2.70		V
Output clamp voltage	V_{CLO}	Applied to output from Y signal output pin		2.40		V
Substrate voltage	$–V_{BB}$			–2.80		V

■ VINY Shift Register Configuration



■ Application Circuit Example



Note: If the external capacitor attached to pin 6 is a electrolytic capacitor, connect the negative pole to pin 6.

■ Package Dimensions (Unit:mm)

SOP008-P-0225A