MN3775RE

8mm (1/2 inch) 1000V CCD Area Image Sensor

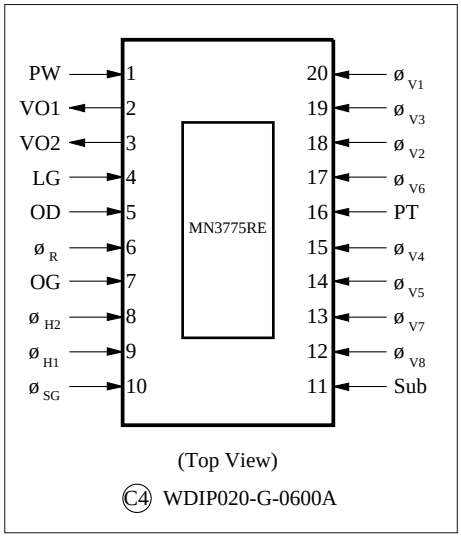
■ Overview

The MN3775RE is a 8mm (1/2 inch) Interline Transfer CCD (IT-CCD) solid state image sensor device.

This device has 1000 photodiodes in the vertical direction and a total of 900K photodiodes in the photoelectric conversion region, 4-phase drive vertical CCDs for signal read out, and a 2-channel horizontal CCD. It is possible to obtain faithful color reproduction due to the high resolution of 900K pixels and the use of the primary colors (R, G, B).

Type No.	Size	System	Color or B/W
MN3775RE	8mm (1/2 inch)		Color

■ Pin Assignments



(Top View)

C4 WDIP020-G-0600A

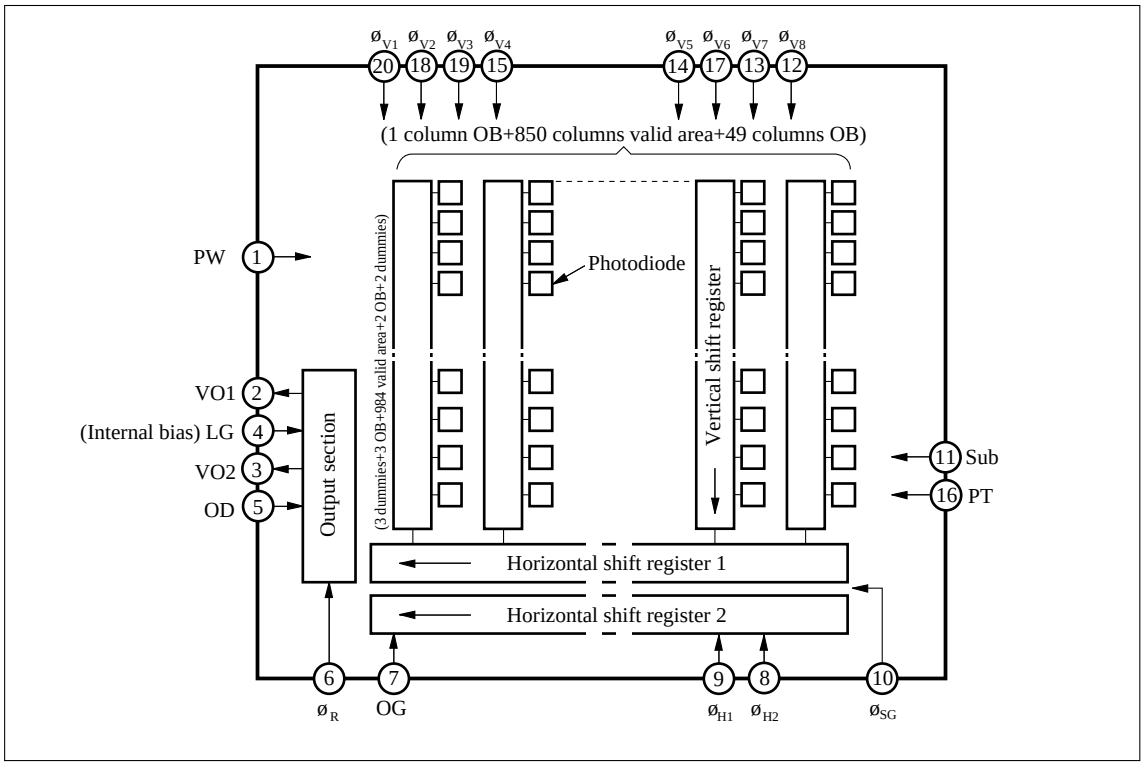
■ Features

- Total number of pixels: 900 (horizontal) × 989 (vertical)
- High resolution
- High color reproduction ability using the primary colors (R, G, B)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter function present
- No image distortion
- Small size enables design of compact equipment
- High reliability
- 20 Pin DIL ceramic package

■ Applications

- Cameras for surveillance, and measurement use
- Image capturing to personal computers
- Electronic still cameras
- Image input device in factory automation

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	PW	P-well	11	Sub	Substrate
2	VO1	Video output 1	12	$ø_{V8}$	Vertical shift register clock pulse (8)
3	VO2	Video output 2	13	$ø_{V7}$	Vertical shift register clock pulse (7)
4	LG	Output load transistor gate	14	$ø_{V5}$	Vertical shift register clock pulse (5)
5	OD	Output drain	15	$ø_{V4}$	Vertical shift register clock pulse (4)
6	$ø_R$	Reset pulse	16	PT	P-well for protection circuit
7	OG	Output gate	17	$ø_{V6}$	Vertical shift register clock pulse (6)
8	$ø_{H2}$	Horizontal register clock pulse (2)	18	$ø_{V2}$	Vertical shift register clock pulse (2)
9	$ø_{H1}$	Horizontal register clock pulse (1)	19	$ø_{V3}$	Vertical shift register clock pulse (3)
10	$ø_{SG}$	CCD shift gate	20	$ø_{V1}$	Vertical shift register clock pulse (1)

■ Absolute Maximum Ratings and Operating Conditions

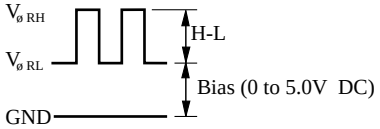
Parameter	Symbol	Rating Note 2)		Operating condition Note 1)			Unit
		min	max	min	typ	max	
Reset drain voltage	V_{RD}	– 0.2	18	14.5	15.0	15.5	V
Output drain voltage	V_{OD}	– 0.2	18	14.5	15.0	15.5	V
Output load transistor gate voltage Note 3)	V_{LG} *3	(Supplied internally)					V
Output gate voltage	V_{OG}	– 0.2	18	2.2	2.5	2.8	V
Protection P well voltage	V_{PT}	–10.0	0.2	$ø_{V(L)}$ –1.2	$ø_{V(L)}$ –1.0	$ø_{V(L)}$ – 0.7	V
P well voltage	V_{PW}	Reference voltage		—	0	—	V
Reset pulse voltage H-L	$V_{ø R (H-L)}$ *1	—	18	7.5	8.0	8.5	V
Reset pulse voltage Bias	$V_{ø R (Bias)}$ *1	– 0.2	—	3.0	3.5	4.0	V
Horizontal register clock pulse voltage 1	$V_{ø H1(H)}$	—	18	7.7	8.0	8.3	V
	$V_{ø H1 (L)}$	– 0.2	—	– 0.2	0	0.3	V
Horizontal register clock pulse voltage 2	$V_{ø H2 (H)}$	—	18	7.7	8.0	8.3	V
	$V_{ø H2 (L)}$	– 0.2	—	– 0.2	0	0.3	V
Vertical shift register clock pulse voltage 1, 5	$V_{ø V1,V5 (H)}$	—	18	14.5	15.0	15.5	V
	$V_{ø V1,V5 (M)}$	—	—	– 0.2	0	0.2	V
	$V_{ø V1,V5 (L)}$	–9	—	–7.3	–7.0	–6.7	V
Vertical shift register clock pulse voltage 2, 6	$V_{ø V2,V6 (M)}$	—	15	1.8	2.0	2.2	V
	$V_{ø V2,V6 (L)}$	–9	—	–7.3	–7.0	–6.7	V
Vertical shift register clock pulse voltage 3, 7	$V_{ø V3,V7 (H)}$	—	18	14.5	15.0	15.5	V
	$V_{ø V3,V7 (M)}$	—	—	– 0.2	0	0.2	V
	$V_{ø V3,V7 (L)}$	–9	—	–7.3	–7.0	–6.7	V
Vertical shift register clock pulse voltage 4, 8	$V_{ø V4,V8 (M)}$	—	15	1.8	2.0	2.2	V
	$V_{ø V4,V8 (L)}$	–9	—	–7.3	–7.0	–6.7	V
Substrate voltage	V_{Sub} * 2	0.2	45	3.0	Adjust	14.5	V
	$\triangle V_{Sub}$ * 2			24.2	25.0	25.8	V
CCD shift gate voltage	$V_{SG (H)}$	—	15	11.7	12.0	12.3	V
	$V_{SG (L)}$	–9	—	–7.3	–7.0	–6.7	V
Operating temperature	T_{opr}	–10	60	—	25	—	˚C
Storage temperature	T_{stg}	–30	70	—	—	—	˚C

Note 1) The initial setting of V_{Sub} shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming is caused at a light input of 100 times the standard value. The standard light input is the one when the exposure is done at an aperture of F/5.6 using a light source of 2856K and 1050nt, and placing a color temperature conversion filter LB-40 (Hoya) and an IR cutting filter CAW-500S (t=2.5mm) in the light path.
If any blooming is present at the minimum operating condition of V_{Sub}, it should be adjusted to 5.0V.
When any overflow charge is present, it should be adjusted to the minimum voltage at which the overflow charge is eliminated in the range under 13.5V.

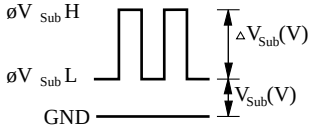
Note 2) Absolute maximum ratings: $-0.2 < V_{Sub} - V_{PT} < +55$ (V)
$-0.2 < V_{øV} - V_{PT} < +24.5$ (V)

Note 3) The LG pin should be grounded via a capacitor of 0.047µF or more.

* 1



* 2 V_{Sub} when using electronic shutter function



■ Optical Characteristics

Type No.	Color or B/W	Valid pixels		S/N typ. (dB)	Saturation output typ. (mV)	Sensitivity F8 typ. (mV)	Vertical smear Sm typ. (%)	Image lag typ. (%)	Horizontal resolution typ. (TV-lines)	Vertical resolution typ. (TV-lines)
		H	V							
MN3775RE	Color	850	984	58	600	120	0.02	0	600	480

■ Graphs of Characteristics

Color Filter Spectral Characteristics