# MN3723FE

## 4.5mm (1/4 inch) EIS CCD Area Image Sensor

### ■ Overview

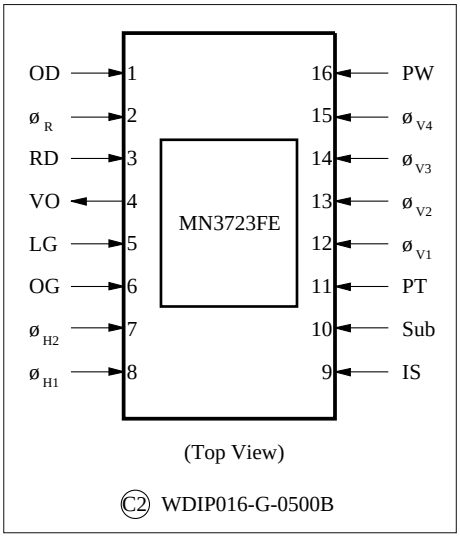
The MN3723FE is a 4.5mm (1/4 inch) Interline Transfer CCD (IT-CCD) solid state image sensor device.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made possible an exposure time of 1/10000 seconds. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

This device has a total of 670K pixels (908 horizontal × 728 vertical) and provides stable and clear images with a resolution of 430 horizontal TV-lines and 420 vertical TV-lines.

| Type No. | Size | System | Color or B/W |
|---|---|---|---|
| MN3723FE | 4.5mm (1/4 inch) | P A L | Color |

### ■ Pin Assignments




(Top View)

C2 WDIP016-G-0500B

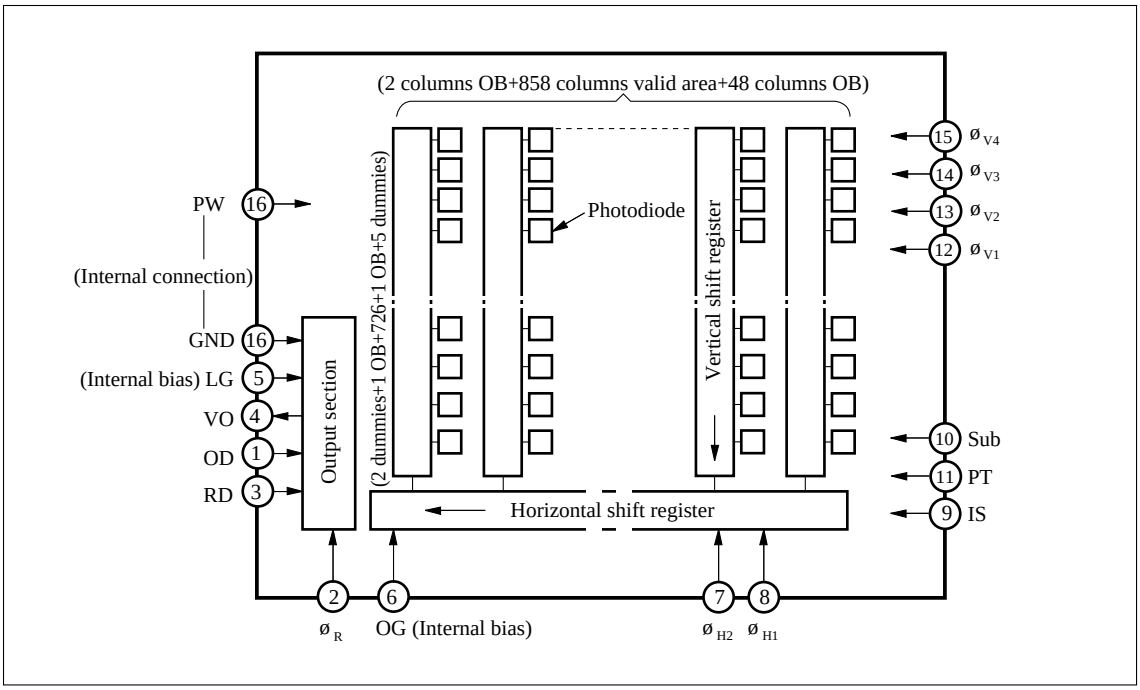
### ■ Features

- Total number of pixels: 908 (horizontal) × 728 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter function present
- No image distortion
- Small size enables design of compact equipment
- High reliability
- 16 Pin DIL ceramic package (cerdip)

### ■ Applications

- Compact lightweight camcoders
- Cameras for surveillance, measurement, and medical use

■ Block Diagram




■ Pin Descriptions

| Pin No. | Symbol | Descriptions | Pin No. | Symbol | Descriptions |
|---|---|---|---|---|---|
| 1 | OD | Output drain | 9 | IS | Horizontal CCD input source |
| 2 | ø R | Reset pulse | 10 | Sub | Substrate |
| 3 | RD | Reset drain | 11 | PT | P-well for protection circuit |
| 4 | VO | Video output | 12 | ø V1 | Vertical shift register clock pulse (1) |
| 5 | LG | Output load transistor gate | 13 | ø V2 | Vertical shift register clock pulse (2) |
| 6 | OG | Output gate | 14 | ø V3 | Vertical shift register clock pulse (3) |
| 7 | ø H2 | Horizontal register clock pulse (2) | 15 | ø V4 | Vertical shift register clock pulse (4) |
| 8 | ø H1 | Horizontal register clock pulse (1) | 16 | PW | P-well |

## ■ Absolute Maximum Ratings and Operating Conditions

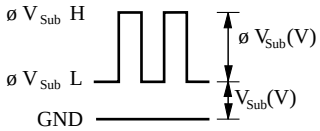
| Parameter | Symbol | Rating Note 2) | | Operating condition Note 1) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | min | max | min | typ | max | |
| Reset drain voltage | $V_{RD}$ | – 0.2 | 18 | 15.6 | 16.2 | 16.8 | V |
| Output drain voltage | $V_{OD}$ | – 0.2 | 18 | 15.6 | 16.2 | 16.8 | V |
| Output load transistor gate voltage Note 3) | $V_{LG}$ | (Supplied internally) | | | | | V |
| Output gate voltage Note 3) | $V_{OG}$ | (Supplied internally) | | | | | V |
| Horizontal CCD input source voltage | $V_{IS}$ | –0.2 | 18 | 15.6 | 16.2 | 16.8 | V |
| Protection P well voltage | $V_{PT}$ | –10.0 | 0.2 | $ø_{V(L)}$ –1.2 | $ø_{V(L)}$ –1.0 | $ø_{V(L)}$ – 0.7 | V |
| P well voltage | $V_{PW}$ | Reference voltage | | — | 0 | — | V |
| Reset pulse voltage H-L | $V_{ø R (H-L)}$ | — | 18 | 10.0 | 11.5 | 13.0 | V |
| Reset pulse voltage Bias | $V_{ø R (Bias)}$ | – 0.2 | — | 2.0 | 2.5 | 3.0 | V |
| Horizontal register clock pulse voltage 1 Note 2) | $V_{ø H1 (H)}$ | — | 18 | 4.4 | 5.0 | 5.6 | V |
| | $V_{ø H1 (L)}$ | – 0.3 | — | – 0.2 | 0 | 0.2 | V |
| Horizontal register clock pulse voltage 2 Note 2) | $V_{ø H2 (H)}$ | — | 18 | 4.4 | 5.0 | 5.6 | V |
| | $V_{ø H2 (L)}$ | – 0.3 | — | – 0.2 | 0 | 0.2 | V |
| Vertical shift register clock pulse voltage 1 | $V_{ø V1 (H)}$ | — | 18 | 15.6 | 16.2 | 16.8 | V |
| | $V_{ø V1 (M)}$ | — | — | – 0.2 | 0 | 0.2 | V |
| | $V_{ø V1 (L)}$ | –9 | — | –7.3 | –7.0 | –6.7 | V |
| Vertical shift register clock pulse voltage 2 | $V_{ø V2 (M)}$ | — | 15 | 0.8 | 1.0 | 1.2 | V |
| | $V_{ø V2 (L)}$ | –9 | — | –7.3 | –7.0 | –6.7 | V |
| Vertical shift register clock pulse voltage 3 | $V_{ø V3 (H)}$ | — | 18 | 15.6 | 16.2 | 16.8 | V |
| | $V_{ø V3 (M)}$ | — | — | – 0.2 | 0 | 0.2 | V |
| | $V_{ø V3 (L)}$ | –9 | — | –7.3 | –7.0 | –6.7 | V |
| Vertical shift register clock pulse voltage 4 | $V_{ø V4 (M)}$ | — | 15 | 0.8 | 1.0 | 1.2 | V |
| | $V_{ø V4 (L)}$ | –9 | — | –7.3 | –7.0 | –6.7 | V |
| Substrate voltage | $V_{Sub}$ * | – 0.2 | 41 | 3.0 | Adjust | 14.5 | V |
| | ø $V_{Sub}$ * | | | 24.2 | 25.0 | 25.8 | V |
| Operating temperature | $T_{opr}$ | –10 | 70 | — | 25.0 | — | ˚C |
| Storage temperature | $T_{stg}$ | –30 | 80 | — | — | — | ˚C |

Note 1) The initial setting of $V_{Sub}$ shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming is caused at a light input of 100 times the standard value. The standard light input is a light source of 2856K, F1.4 and 27.5nt.
If any FPN picture is present at the minimum operating condition of $V_{Sub}$, it should be adjusted to the minimum voltage at which there is no FPN picture.
When any overflow charge is present, it should be adjusted to the minimum voltage at which the overflow charge is eliminated in the range under 13.5V.

Note 2) Absolute maximum ratings: $-0.2 < V_{Sub} - V_{PT} < +55$ (V)
$-0.2 < V_{øV} - V_{PT} < +24.5$ (V)

Note 3) The LG and OG pins should each be grounded via a capacitor of 0.047µF or more.

* $V_{Sub}$ when using electronic shutter function

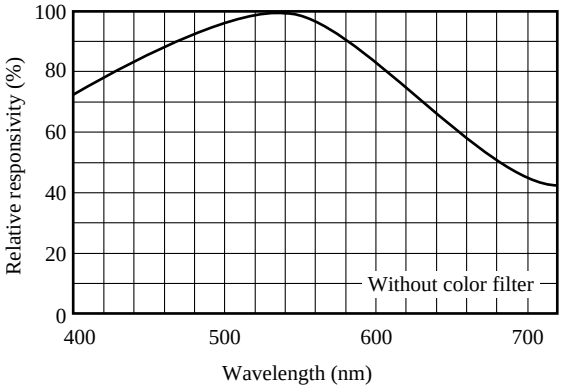



## ■ Optical Characteristics

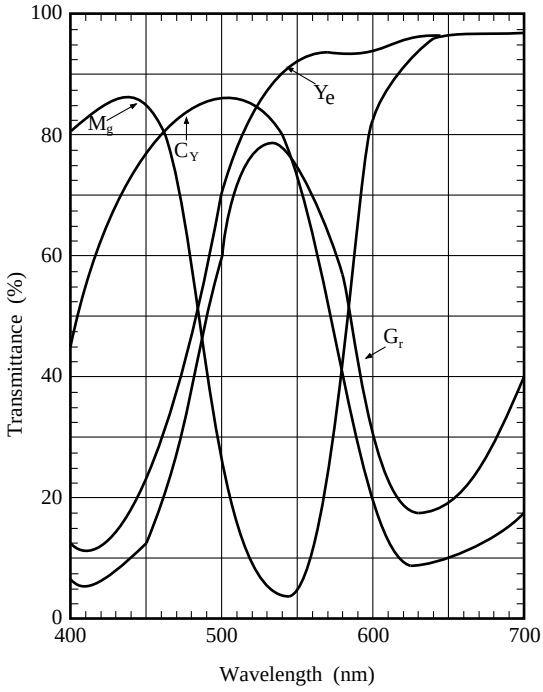
| Type No. | Color or B/W | Valid pixels H | Valid pixels V | S/N typ. (dB) | Saturation output typ. (mV) | Sensitivity F8 typ. (mV) | Vertical smear Sm typ. (%) | Image lag typ. (%) | Horizontal resolution typ. (TV-lines) | Vertical resolution typ. (TV-lines) |
|---|---|---|---|---|---|---|---|---|---|---|
| MN3723FE | Color | 858 | 726 | 60 | 550 | 180 | 0.02 | 0 | 430 | 420 |

■ Graphs of Characteristics

CCD Spectral Characteristics



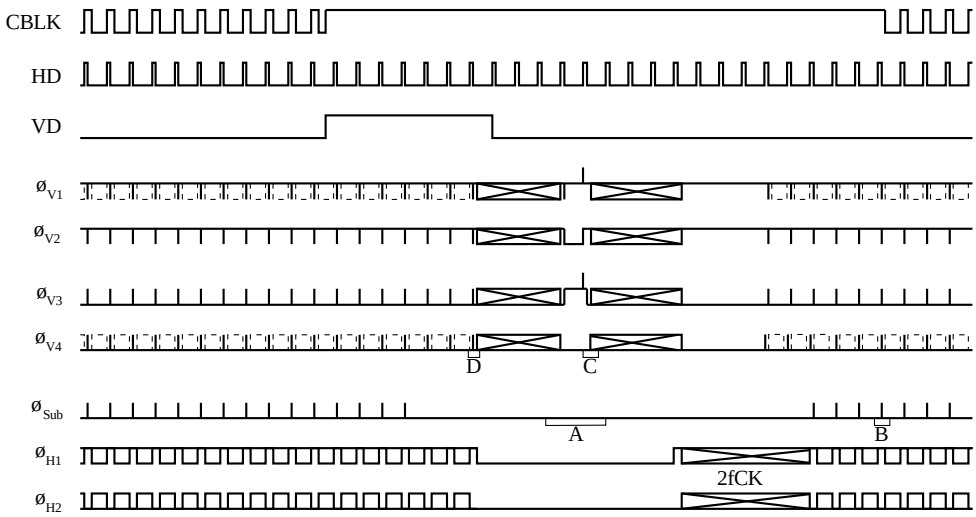

Color Filter Spectral Characteristics



■ Example of Recommended Driving Pulses

• V Rate timing

< Field A >

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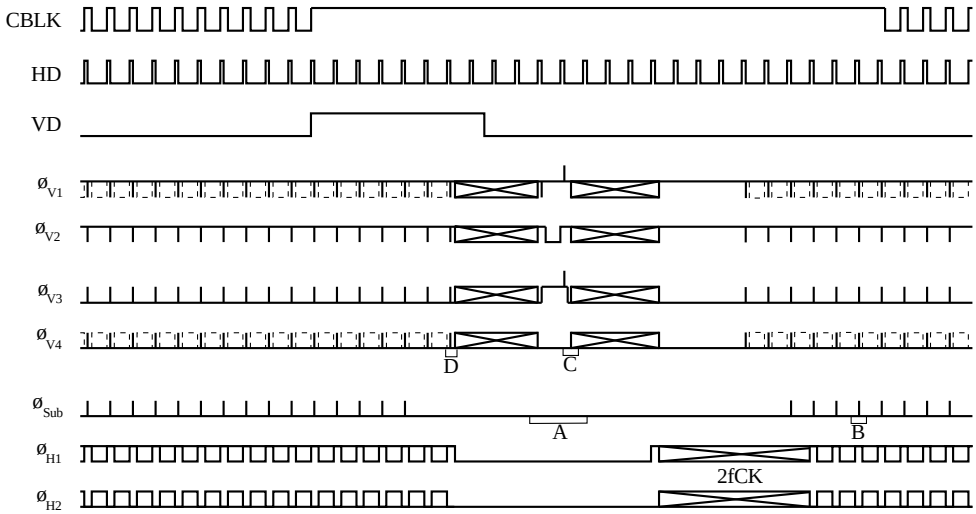
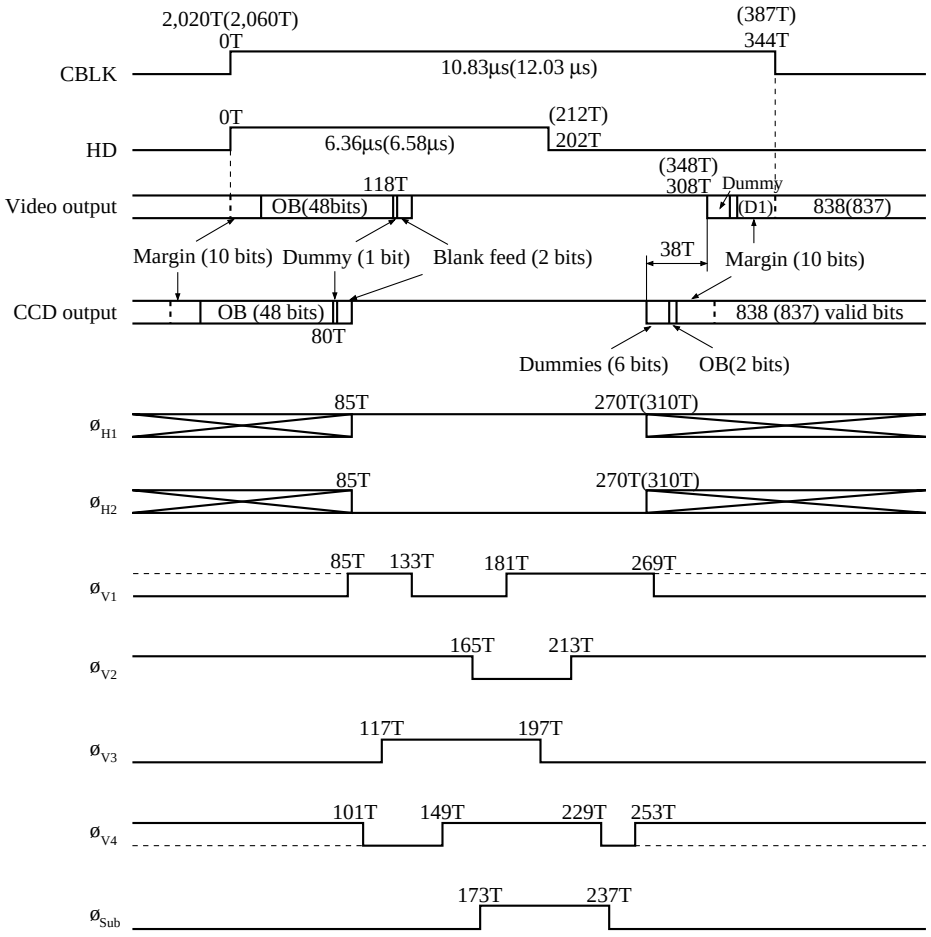


• H Rate timing




• High speed pulse timing