

MN3713FE

4.5mm (1/4 inch) EIS CCD Area Image Sensor

■ Overview

The MN3713FE is a 4.5mm (1/4 inch) Interline Transfer CCD (IT-CCD) solid state image sensor device.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made possible an exposure time of 1/10000 seconds. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

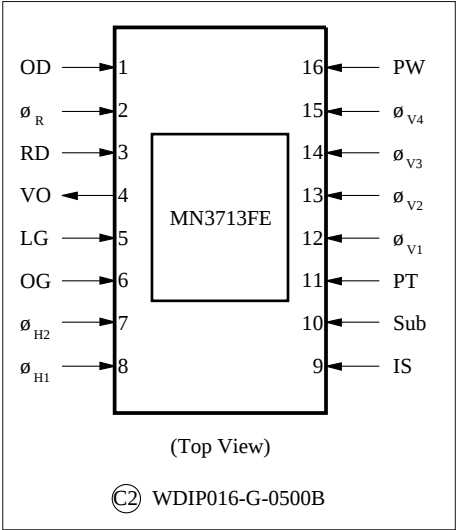
This device has a total of 560K pixels (908 horizontal × 616 vertical) and provides stable and clear images with a resolution of 430 horizontal TV-lines and 350 vertical TV-lines.

Type No.	Size	System	Color or B/W
MN3713FE	4.5mm (1/4 inch)	NTSC	Color

■ Features

- Total number of pixels: 908 (horizontal) × 616 (vertical)
- High sensitivity
- Low noise
- Broad dynamic range
- Low smear
- Low image lag
- Electronic shutter function present
- No image distortion
- Small size enables design of compact equipment
- High reliability
- 16 Pin DIL ceramic package (surdip)

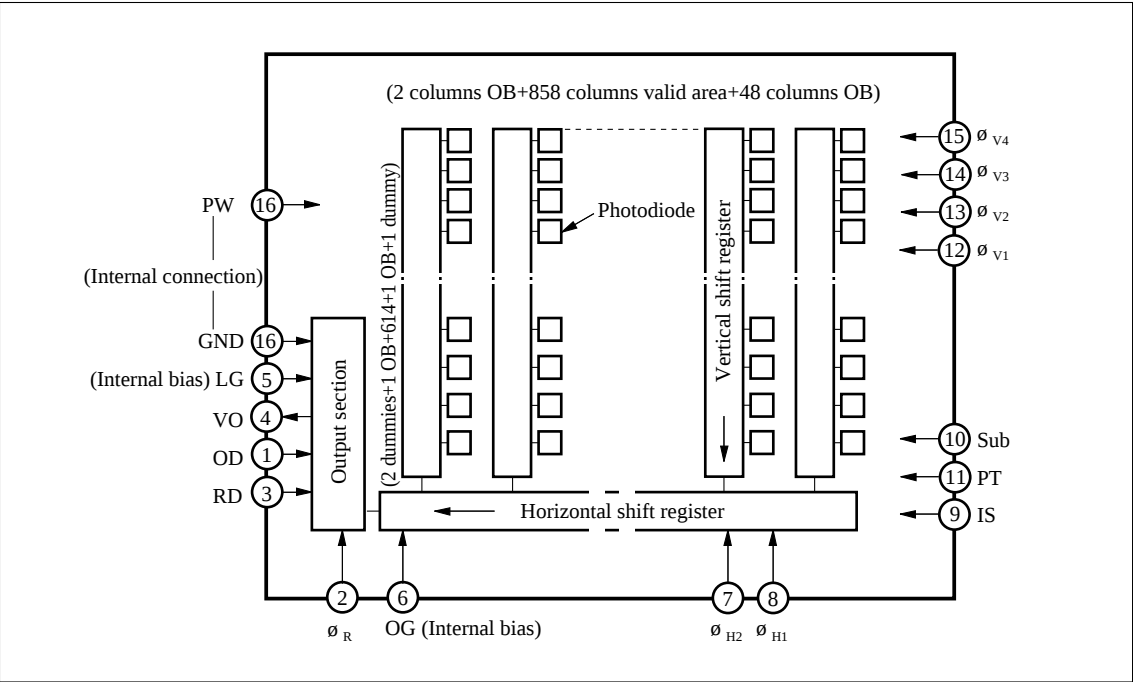
■ Pin Assignments



■ Applications

- Compact lightweight camcoders, including wide screens
- Cameras for surveillance, measurement, and medical use

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	9	IS	Horizontal CCD input source
2	ϕ_R	Reset pulse	10	Sub	Substrate
3	RD	Reset drain	11	PT	P-well for protection circuit
4	VO	Video output	12	ϕ_{V1}	Vertical shift register clock pulse (1)
5	LG	Output load transistor gate	13	ϕ_{V2}	Vertical shift register clock pulse (2)
6	OG	Output gate	14	ϕ_{V3}	Vertical shift register clock pulse (3)
7	ϕ_{H2}	Horizontal register clock pulse (2)	15	ϕ_{V4}	Vertical shift register clock pulse (4)
8	ϕ_{H1}	Horizontal register clock pulse (1)	16	PW	P-well

■ Absolute Maximum Ratings and Operating Conditions

Parameter	Symbol	Rating ^{Note 2)}		Operating condition ^{Note 1)}			Unit
		min	max	min	typ	max	
Reset drain voltage	V_{RD}	-0.2	18	15.6	16.2	16.8	V
Output drain voltage	V_{OD}	-0.2	18	15.6	16.2	16.8	V
Output load transistor gate voltage ^{Note 3)}	V_{LG}	(Supplied internally)					V
Output gate voltage ^{Note 3)}	V_{OG}	(Supplied internally)					V
Vertical CCD input source voltage	V_{IS}	-0.2	18	15.6	16.2	16.8	V
Protection P well voltage	V_{PT}	-10.0	0.2	$\phi_{V(L)}$ -1.2	$\phi_{V(L)}$ -1.0	$\phi_{V(L)}$ -0.7	V
P well voltage	V_{PW}	Reference voltage		—	0	—	V
Reset pulse voltage	H-L $V_{\phi R(H-L)}$ * 1	—	18	4.7	5.0	5.3	V
	Bias $V_{\phi R(Bias)}$ * 1	-0.2	—	0	Adjust	5.0	V
Horizontal register clock pulse voltage 1	$V_{\phi H1(H)}$	—	18	4.7	5.0	5.3	V
	$V_{\phi H1(L)}$	-0.2	—	0	0	0	V
Horizontal register clock pulse voltage 2	$V_{\phi H2(H)}$	—	18	4.7	5.0	5.3	V
	$V_{\phi H2(L)}$	-0.2	—	0	0	0	V
Vertical shift register clock pulse voltage 1	$V_{\phi V1(H)}$	—	18	15.6	16.2	16.8	V
	$V_{\phi V1(M)}$	—	—	-0.2	0	0.2	V
	$V_{\phi V1(L)}$	-9	—	-7.3	-7.0	-6.7	V
Vertical shift register clock pulse voltage 2	$V_{\phi V2(M)}$	—	15	0.8	1.0	1.2	V
	$V_{\phi V2(L)}$	-9	—	-7.3	-7.0	-6.7	V
Vertical shift register clock pulse voltage 3	$V_{\phi V3(H)}$	—	18	15.6	16.2	16.8	V
	$V_{\phi V3(M)}$	—	—	-0.2	0	0.2	V
	$V_{\phi V3(L)}$	-9	—	-7.3	-7.0	-6.7	V
Vertical shift register clock pulse voltage 4	$V_{\phi V4(M)}$	—	15	0.8	1.0	1.2	V
	$V_{\phi V4(L)}$	-9	—	-7.3	-7.0	-6.7	V
Substrate voltage	V_{Sub} * 2	-0.2	45	3.0	Adjust	14.5	V
	ϕV_{Sub} * 2			24.2	25.0	25.8	V
Operating temperature	T_{opr}	-10	70	—	25.0	—	°C
Storage temperature	T_{stg}	-30	80	—	—	—	°C

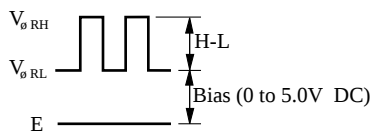
Note 1) The initial setting of V_{Sub} shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming is caused at a light input of 100 times the standard value. The standard light input is the one when the exposure is done at an aperture of F/4 using a light source of 2856K and 1050nt, and placing a color temperature conversion filter LB-40 (Hoya) and an IR cutting filter CAW-500 ($\tau=2.5\text{mm}$) in the light path.

Note 2) Absolute maximum ratings: $-0.2 < V_{Sub} - V_{PT} < +55 \text{ (V)}$

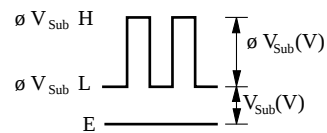
$-0.2 < V_{\phi V} - V_{PT} < -25.5 \text{ (V)}$

Note 3) The LG and OG pins should each be grounded via a capacitor of 0.047 μF or more.

*1



*2 V_{Sub} when using electronic shutter function

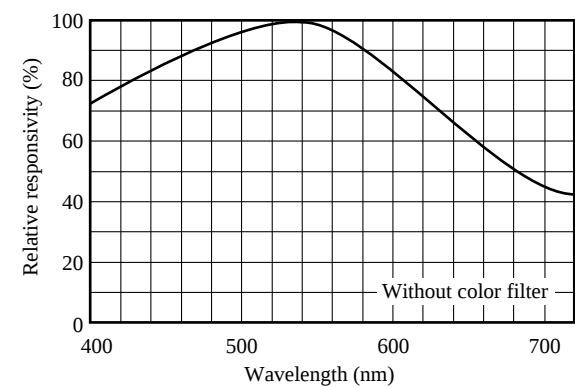


■ Optical Characteristics

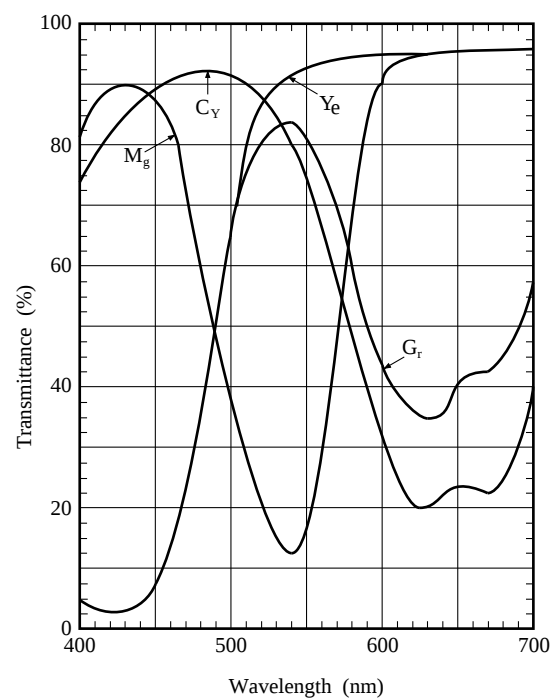
Type No.	Color or B/W	Valid pixels		S/N typ. (dB)	Saturation output typ. (mV)	Sensitivity F8 typ. (mV)	Vertical smear Sm typ. (%)	Image lag typ. (%)	Horizontal resolution typ. (TV-lines)	Vertical resolution typ. (TV-lines)
		H	V							
MN3713FE	Color	858	614	60	600	200	0.02	0	430	350

■ Graphs of Characteristics

CCD Spectral Characteristics

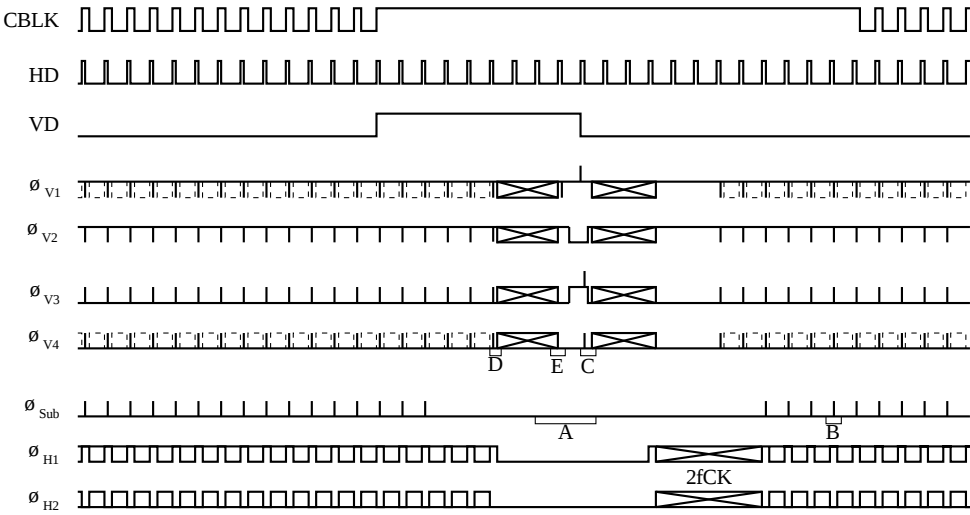


Color Filter Spectral Characteristics

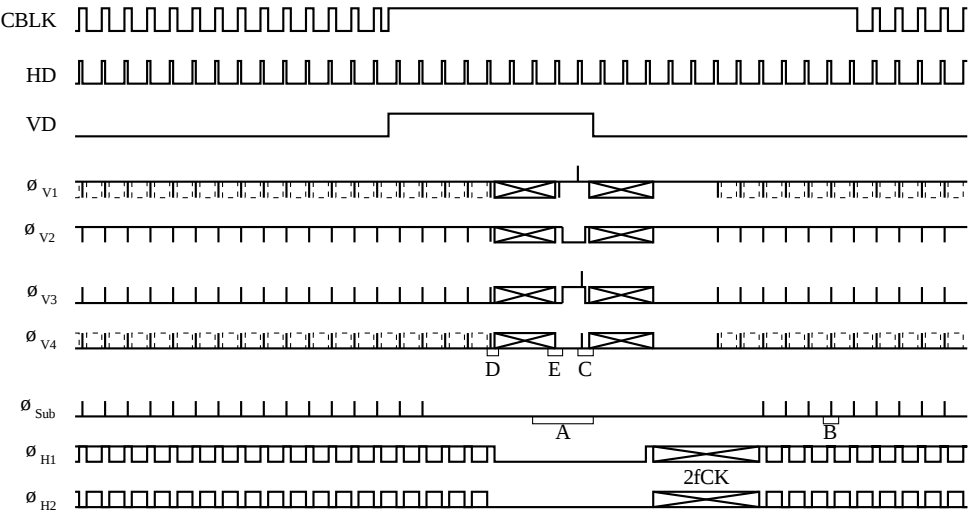


■ Example of Recommended Driving Pulses
• V Rate timing

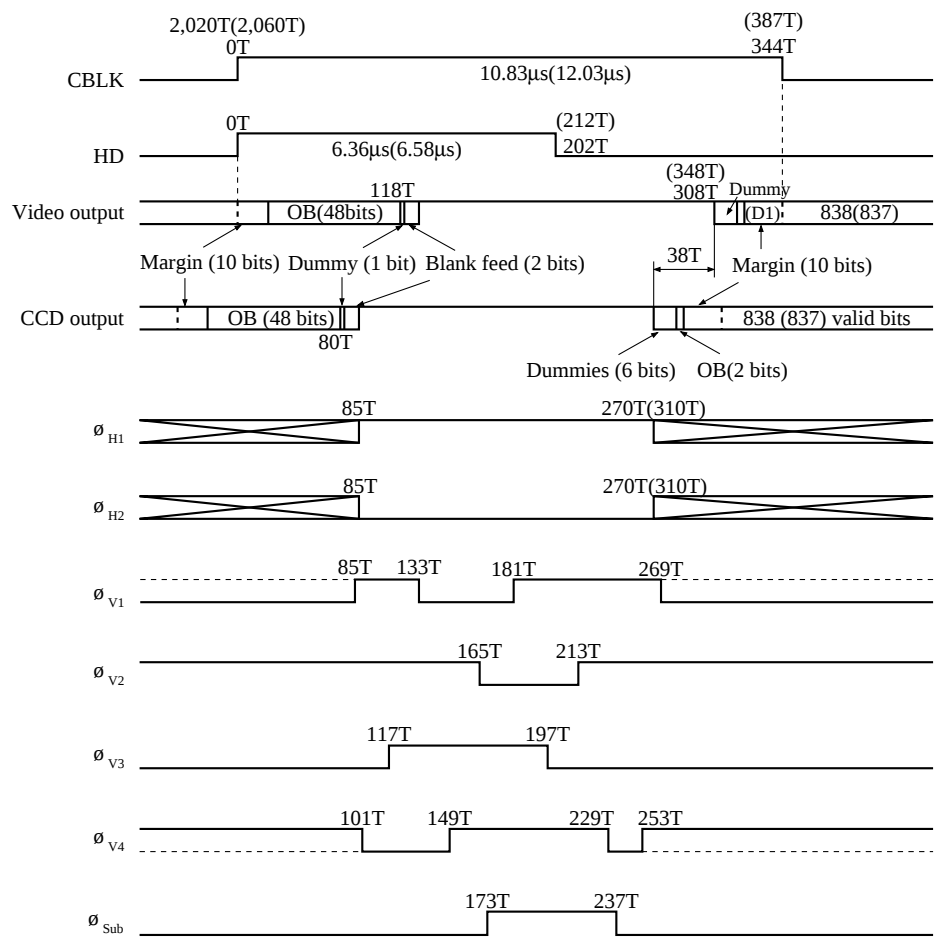
< Field A >



< Field B >



• H Rate timing



• High speed pulse timing

