MN3673RE

Color CCD Linear Image Sensor with 2592 Bits each for R, G, and B Colors

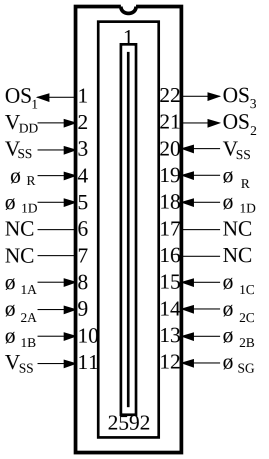
■ Overview

The MN3673RE is a 2592-pixel high sensitivity CCD linear image sensor combining photo-sites using low dark output floating photodiodes and CCD analog shift registers for read out. It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

■ Features

- 7776 (2592 × R, G, B) floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Since the spacing between the photodiode lines of different colors is small, it is possible to greatly reduce the memory for compensation between lines. (1 line between R-B, 10 lines between B-G)
- The configuration of the signal processing circuits such as the preamplifier, sample and hold circuit, etc., becomes simpler since the separate signal output pins are provided for the pixels of each of the colors R, G, an B.
- RGB primary colors type on-chip color filters are used for color separation.
- The dark signal output voltage has been suppressed to a very low level due to the use of photodiodes with a new structure. (0.2mV (typ.) at an accumulation time of 10ms.)
- Operation with a single +12V positive power supply.

■ Pin Assignments



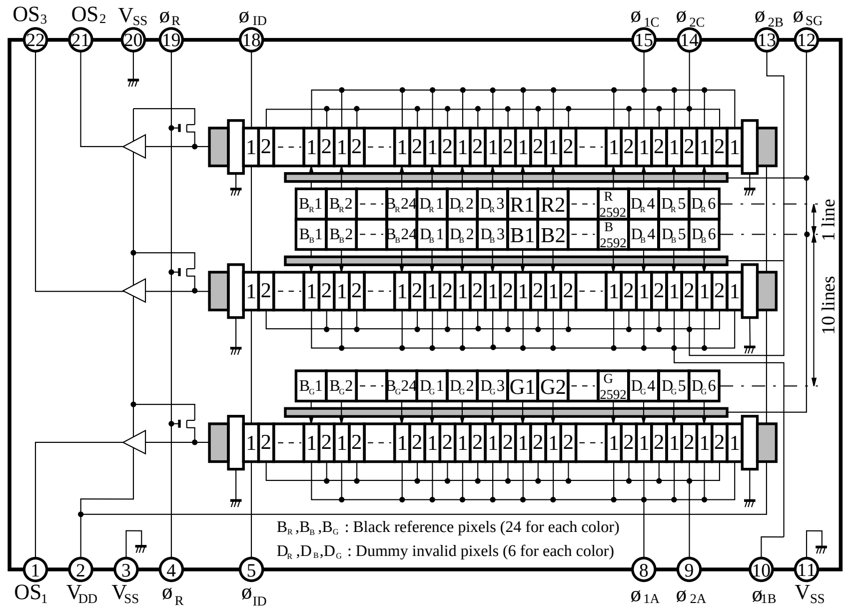
(Top View)

Ⓒ25 WDIP022-C-0440B

■ Application

- Color graphic read out in color copying machines, color scanners, and color fax machines.

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25˚C, V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +17	V
Input pin voltage	V_I	– 0.3 to +17	V
Output pin voltage	V_O	– 0.3 to +17	V
Operating temperature range	T_{opr}	0 to + 60	˚C
Storage temperature range	T_{stg}	–25 to + 85	˚C

■ Operating Conditions

• Voltage conditions (Ta=–20 to + 60˚C, V_{SS}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.4	12.0	13.0	V
CCD shift register clock High level	$V_{øH}$	(ø$_{1A}$ ~ ø$_{1D}$, ø$_{2A}$~ ø$_{2C}$)	V_{DD}-1	V_{DD}	V_{DD}	V
CCD shift register clock Low level	$V_{øL}$	(ø$_{1A}$ ~ ø$_{1D}$, ø$_{2A}$~ ø$_{2C}$)	0	0.5	0.8	V
Shift gate clock High level	V_{SH}	(ø$_{SG}$)	V_{DD}-1	V_{DD}	V_{DD}	V
Shift gate clock Low level	V_{SL}	(ø$_{SG}$)	0	0.5	0.8	V
Reset gate clock High level	V_{RH}	(ø$_R$)	V_{DD}-1	V_{DD}	V_{DD}	V
Reset gate clock Low level	V_{RL}	(ø$_R$)	0	0.5	0.8	V

• Timing conditions (Ta=–20 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	f_C=f_R=1/2T	0.1	—	5	MHz
Reset clock frequency	f_R		0.1	—	5	MHz
Shift register clock rise time	t_{Cr}	See timing diagram	0	20	50	ns
Shift register clock fall time	t_{Cf}		0	20	50	ns
Shift clock rise time	t_{Sr}	See timing diagram	0	15	50	ns
Shift clock fall time	t_{Sf}		0	15	50	ns
Shift clock set up time	t_{Ss}		250	400	1000	ns
Shift clock pulse width	t_{Sw}		1.0	1.8	10	µs
Shift clock hold time	t_{Sh}		0	—	1	µs
Reset clock rise time	t_{Rr}	See timing diagram	0	10	20	ns
Reset clock fall time	t_{Rf}		0	10	20	ns
Reset clock set up time	t_{Rs}		0.7T	—	—	ns
Reset clock pulse width	t_{Rw}		20	30	—	ns
Reset clock hold time	t_{Rh}		5	10	—	ns

■ Electrical Characteristics

• Clock input capacitance (Ta=0 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	C_{1A}, C_{1B} C_{1C}, C_{2A} C_{2B}, C_{2C}	V_{IN} =12V, f=1MHz	—	300	—	pF
Shift register final stage clock input capacitance	C_{1D}		—	10	—	pF
Reset clock input capacitance	C_{RS}		—	10	—	pF
Shift clock input capacitance	C_{SG}		—	250	—	pF

• DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{DD} = +12V	—	10	—	mA

■ Electrical Characteristics (continued)

- AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output delay time	t_{OS}		—	50	—	ns

■ Optical Characteristics

<Inspection conditions>

- Ta=25˚C, V_{DD}=12V, $V_{øH}$=V_{SH}=V_{RH}=12V (pulse), f_C=f_R=1MHz, T_{int} (accumulation time)=10ms
- Light source: Daylight type fluorescent lamp with IR/UV cutting filter
- Optical system: A slit with an aperture dimensions of 20mm × 20mm is used with a slit to sensor spacing of 200mm (equivalent to F=10).
- Load resistance = 100k Ohms
- These specifications apply to the 2592 valid pixels for each color excluding the dummy pixels D1 to D6.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R_R		0.7	1.0	1.3	V/lx·s
	R_G		1.4	2.0	2.6	
	R_B		1.0	1.4	1.8	
Photo response non-uniformity	PRNU	Note 1	—	7	15	%
Saturation output voltage	V_{SAT}	Note 2	0.9	1.2	—	V
Saturation exposure	SE_R	Note 2	0.69	1.20	—	lx·s
	SE_G	Note 2	0.35	0.60	—	
	SE_B	Note 2	0.50	0.86	—	
Dark signal output voltage	V_{DRK}	Dark condition, see Note 3	—	0.2	2.0	mV
Dark signal output non-uniformity	DSNU	Dark condition, see Note 3	—	0.1	1.0	mV
Shift register total transfer efficiency	STTE		92	—	—	%
Output impedance	Z_O		—	—	1	kΩ
Dynamic range	DR	Note 4	—	6000	—	
Signal output pin DC level	V_{OS}	Absolute DC level of OS_1, OS_2, OS_3, see Note 5	2.5	4.0	5.5	V
Signal output pin DC level difference	$\triangle V_{OS}$	Relative DC difference between OS_1, OS_2, OS_3, see Note 5	—	50	200	mV

Note 1) The photo response non-uniformity (PRNU) is defined by the following equation, where X_{ave} is the average output voltage of the 2592 valid pixels and Δx is the absolute value of the difference between X_{ave} and the voltage of the maximum (or minimum) output pixel, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

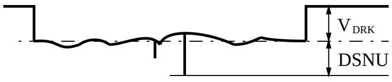
$$\mathrm{PRNU}=\frac{\triangle x}{X_{ave}}\times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation.

Note 2) The Saturation output voltage (V_{SAT}) is defined as the output voltage at the point when the linearity of the photoelectric characteristics cannot be maintained as the incident light intensity is increased. (The light intensity of exposure at this point is called the saturation exposure.)

Note 3) The dark signal output voltage (V_{DRK}) is defined as the average output voltage of the 2592 pixels in the dark condition at Ta=25˚C and T_{int}=10ms. Normally, the dark output voltage doubles for every 8 to 10˚C rise in Ta, and is proportional to T_{int}.

The dark signal output non-uniformity (DSNU) is defined as the difference between the maximum output voltage among all the valid pixels and V_{DRK} in the dark condition at Ta=25˚C and T_{int}=10ms.

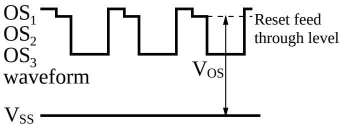


Note 4) The dynamic range is defined by the following equation.

$$\mathrm{DR}=\frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

Note 5) The signal output pin DC level (V_{OS}) and the compensation output pin DC level (V_{DS}) are the voltage values shown in the following figure.



■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS_1	Signal output 1 (Green)	
2	V_{DD}	Power supply	
3	V_{SS}	Ground	
4	$ø_{R}$	Reset clock	Internally connected to pin 19.
5	$ø_{1D}$	CCD final stage clock (Phase 1)	Internally connected to pin 18.
6	NC	Non connection	
7	NC	Non connection	
8	$ø_{1A}$	CCD clock (Phase 1)	
9	$ø_{2A}$	CCD clock (Phase 2)	
10	$ø_{1B}$	CCD clock (Phase 1)	
11	V_{SS}	Ground	
12	$ø_{SG}$	Shift clock gate	
13	$ø_{2B}$	CCD clock (Phase 2)	
14	$ø_{2C}$	CCD clock (Phase 2)	
15	$ø_{1C}$	CCD clock (Phase 1)	
16	NC	Non connection	
17	NC	Non connection	
18	$ø_{1D}$	CCD final stage clock (Phase 1)	
19	$ø_{R}$	Reset clock	
20	V_{SS}	Ground	
21	OS_2	Signal output 2 (Red)	
22	OS_3	Signal output 3 (Blue)	

Note) Connect all NC pins externally to V_{SS} (GND).

■ Construction of the Image Sensor

The MN3673RE can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11µm floating photodiode and a 3µm channel stopper (isolation region) per pixel, and such 2592 pixels per color are arranged in a linear row with a pitch of 14µm along the main scanning direction with the pixel rows of different colors being placed parallel to each other.
- There is a spacing of one line between R-B in the sideways scanning direction (center to center spacing of 14µm) and a 10 line spacing between B-G in the sideways scanning direction (center to center spacing of 140µm).
- The photo detector's windows are 14µm × 14µm squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 24 optically shielded pixels (black reference pixels) which serve as the black reference.

b) CCD Transfer region (shift register)

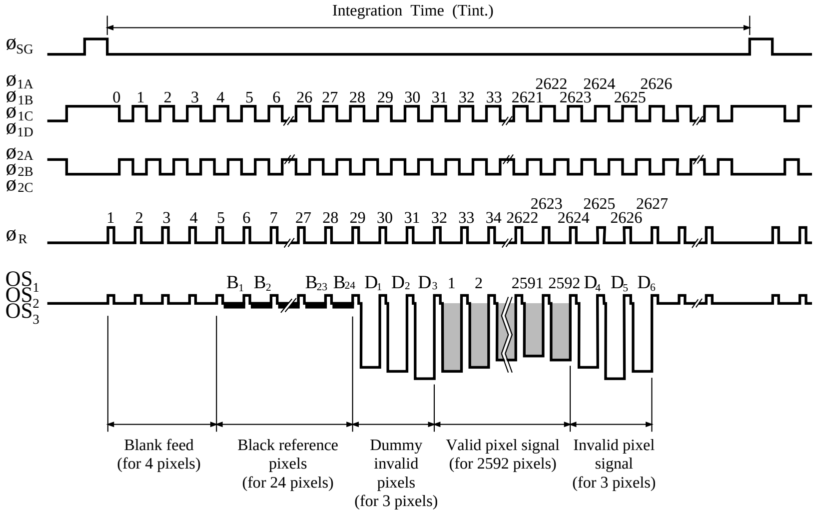
- The light output that has been photoelectrically converted is transferred to the CCD transfer for each odd and even pixel at the timing of the shift clock ($ø_{SG}$). The optical signal charge transferred to this analog shift register is successively transferred out and guided to the output.
- A buried type CCD that can be driven by a two phase clock ($ø_1$, $ø_2$) is used for the analog shift register.
- The last gate of the CCD transfer region is connected to an independent pin ($ø_{1D}$). By driving this pin independent of the other pins by a clock driver, it is possible to speed up the flow of signal charge into the charge to voltage conversion region thereby making the output waveform rise sharply. This makes it easy to obtain margin of the signal processing time during high speed drive operation.

c) Output region

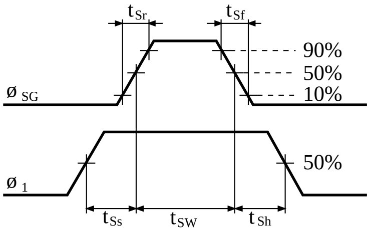
- The signal charge transferred to the output region is first sent to the charge to voltage conversion region where it is converted into a voltage level corresponding to the amount of the signal charge, and then output after impedance conversion in a two stage source follower amplifier.

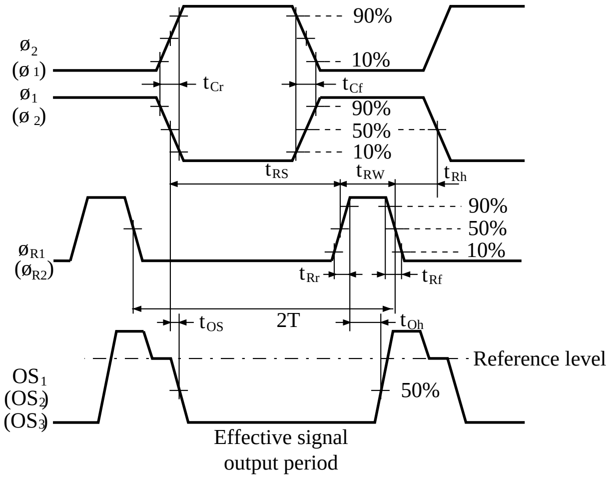
■ Timing Diagram

(1) I/O timing



(2) Drive timing





■ Graphs and Characteristics

Spectral Response Characteristics