MN3672RE (Preliminary)

Color CCD Linear Image Sensor with 5000 Bits each for R, G, and B Colors

■ Overview

The MN3672RE is a high speed high responsivity CCD color linear image sensor with 5000 pixels for each of the colors R, G, and B. This device consists of a photodetector region having low dark output floating photodiodes and a CCD analog shift register in the read out region.

It is possible to read out an A3 size color document with a high quality and a high resolution of 400dpi.

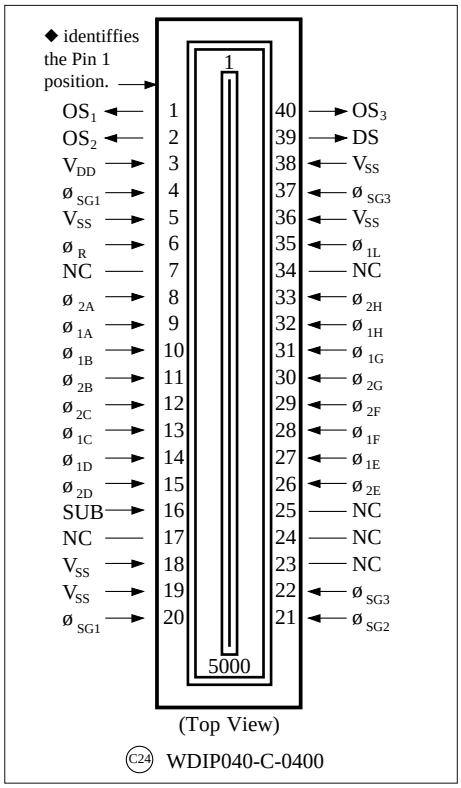
■ Features

- 5000 floating photodiodes for each color R, G, and B, and an n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Since the photodiode lines for each color are neighboring (with a line spacing of 14µm), it is possible to greatly reduce the memory for compensation between lines.
- The configuration of the signal processing circuits such as the preamplifier, sample and hold circuit, etc., becomes simpler since the separate signal output pins are provided for the pixels of each of the colors R, G, and B.
- RGB primary colors type on chip color filters are used for color separation.
- The dark signal output voltage has been suppressed to a very low level due to the use of photodiodes with a new structure. (0.2mV (typ.) at accumulation time of 10ms.)
- Large signal output of typically 1.0V at saturation can be obtained.
- Operation with a single +12V positive power supply.

■ Application

- Color graphic read out in color copying machines, color scanners, and color fax machines.

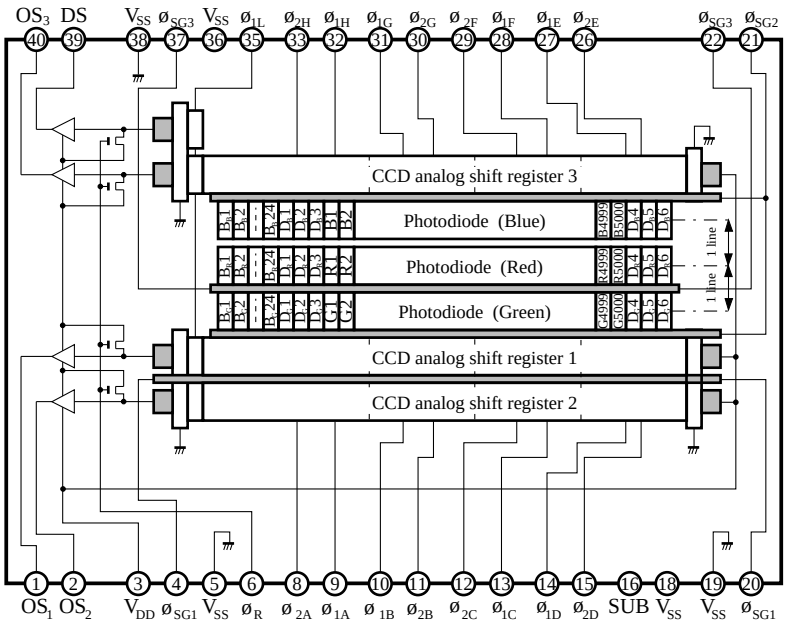
■ Pin Assignments



(Top View)

C24 WDIP040-C-0400

■ Block Diagram



B_R,B_B,B_G:
Black reference pixels
(24 pixels each)

D_R,D_B,D_G:
Dummy invalid pixels
(6 pixels each)

■ Absolute Maximum Ratings (Ta=25˚C, V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	– 0.3 to +17	V
Input pin voltage	V_I	– 0.3 to +17	V
Output pin voltage	V_O	– 0.3 to +17	V
Operating temperature range	T_{opr}	0 to + 60	˚C
Storage temperature range	T_{stg}	–25 to + 85	˚C

■ Operating Conditions

• Voltage conditions (Ta=0 to + 60˚C, V_{SS}=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V_{DD}		11.0	12.0	13.0	V
CCD shift register clock High level	$V_{øH}$	($ø_{1A}$ ~ $ø_{1L}$, $ø_{2A}$~ $ø_{2H}$)	—	10.0	11.0	V
CCD shift register clock Low level	$V_{øL}$	($ø_{1A}$ ~ $ø_{1L}$, $ø_{2A}$~ $ø_{2H}$)	0	0.5	0.8	V
Shift gate clock High level	V_{S1H}	($ø_{SG1}$)	—	$V_{øH}$ +2	—	V
	V_{S2H}	($ø_{SG2}$)	9.0	10.0	11.0	V
	V_{S3H}	($ø_{SG3}$)	—	4.0	—	V
Shift gate clock Low level	V_{SL}	($ø_{SG1}$~ $ø_{SG3}$)	0	0.5	0.8	V
Reset gate clock High level	V_{RH}	($ø_R$)	V_{DD} –1	V_{DD}	V_{DD}	V
Reset gate clock Low level	V_{RL}	($ø_R$)	0	0.5	0.8	V

• Timing conditions (Ta=0 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f_C	See drive timing diagram (2) f_C=1/2T	0.1	1.0	5.0	MHz
Reset clock frequency (=data rate)	f_R	See drive timing diagram (2) f_R=1/2T	0.1	1.0	5.0	MHz
Shift register clock rise time	t_{Cr}	See drive timing diagram (2) f_R=1/2T	0	10	20	ns
Shift register clock fall time	t_{Cf}		0	10	20	ns
Shift clock 1 rise time	t_{SG1r}		0	20	50	ns
Shift clock 1 fall time	t_{SG1f}		0	20	50	ns
Shift clock 1 set up time	t_{SG1s}		See drive timing diagram (1)			µs
Shift clock 1 pulse width	t_{SG1w}					µs
Shift clock 2 rise time	t_{SG2r}		0	15	50	ns
Shift clock 2 fall time	t_{SG2f}		0	15	50	ns
Shift clock 2 pulse width	t_{SG2w}		See drive timing diagram (1)			µs
Shift clock 3 rise time	t_{SG3r}		0	20	50	ns
Shift clock 3 fall time	t_{SG3f}		0	20	50	ns
Shift clock 3 set up time	t_{SG3s}		See drive timing diagram (1)			µs
Shift clock 3 pulse width	t_{SG3w}					µs
Shift clock 3 hold time	t_{SG3h}					µs
Reset clock rise time	t_{Rr}		0	5	10	ns
Reset clock fall time	t_{Rf}		0	5	10	ns
Reset clock set up time	t_{Rs}	See drive timing diagram (2)	0.7T			ns
Reset clock pulse width	t_{Rw}		10			ns
Reset clock hold time	t_{Rh}		10			ns

■ Electrical Characteristics

• Clock input capacitance (Ta=0 to + 60˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clocks A to D input capacitance	C_{1A}, C_{1B} C_{1C}, C_{1D} C_{2A}, C_{2B} C_{2C}, C_{2D}	V_{IN} =12V, f=1MHz	—	160	—	pF
Shift register clocks E to H input capacitance	C_{1E}, C_{1F} C_{1G}, C_{1H} C_{2E}, C_{2F} C_{2G}, C_{2H}		—	120	—	pF
Shift register final stage clock input capacitance	C_{1L}		—	10	—	pF
Reset clock input capacitance	C_{RS}		—	10	—	pF
Shift clocks 1, 3 input capacitance	C_{SG1}, C_{SG3}		—	150	—	pF
Shift clock 2 input capacitance	C_{SG2}		—	250	—	pF

• DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	I_{DD}	V_{DD}=+12V	—	15	—	mA

• AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output delay time	t_{OS}		—	50	—	ns

■ Optical Characteristics

<Inspection conditions>

- Ta=25˚C, V_{DD}=12V,
  Pulse: $V_{øH}$=10V, V_{RH}=12V, V_{S1H}=12V, V_{S2H}=10V, V_{S3H}=4V, f_C=f_R=1MHz, T_{int} (accumulation time)=10ms
- Light source: A light source with IR cutting filter (CM-500S)
- Optical system: A slit with an aperture dimensions of 20mm × 20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- Load resistance = 100k Ohms
- These specifications apply to the 5000 valid pixels for each color excluding the dummy pixels D1 to D6.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R_R	Note 1		1.2		V/lx·s
	R_G	Note 1		1.5		
	R_B	Note 1		1.3		
Photo response non-uniformity	PRNU	Note 2		10		%
Saturation output voltage	V_{SAT}	Note 3		1.0		V
Saturation exposure	SE_R	Note 4		0.83		lx·s
	SE_G	Note 4		0.67		
	SE_B	Note 4		0.77		
Dark signal output voltage	V_{DRK}	Dark condition, see Note 5		0.2	2.0	mV
Dark signal output non-uniformity	DSNU	Dark condition, see Note 6		0.1	2.0	mV
Shift register total transfer efficiency	STTE		92			%
Output impedance	Z_O				1	kΩ
Dynamic range	DR	Note 7		5000		
Signal output pin DC level	V_{OS}	(OS1, OS2, OS3) see Note 8		4.5		V
Compensation output pin DC level	V_{DS}	Note 8		4.5		V
Signal and compensation output pin DC level difference	$\lvert V_{OS} - V_{DS} \rvert$	Note 8			300	mV

Connect all NC pins externally to V_{SS} (GND).

Note 1) Responsivity (R)
This is the value obtained by dividing the average output voltage (V) of all valid pixels of each of the colors R, G, and B by the exposure (lx·s). The exposure is the product of the incident light intensity (lx) and the accumulation time (s).
Since the responsivity changes with the spectral distribution of the light source used, care should be taken when using a light source other than the daylight type fluorescent lamp specified in the inspection conditions.

Note 2) Photo response non-uniformity (PRNU)
This is defined by the following equation where X_{ave} is the average output voltage of the active pixels of each of the colors R, G, and B, and Δx is the difference between the output voltage of the maximum (or minimum) output pixel and X_{ave}, when the photodetector region is illuminated with light of a uniform illumination intensity distribution.

$$PRNU = \frac{\triangle x}{X_{ave}} \times 100\ (\%)$$

The incident light intensity shall be 50% of the standard saturation llight intensity.

Note 3) Saturation output voltage (V_{SAT})
This is the output voltage at the point beyond which it is not possible to maintain the linearity of the photoelectric conversion characteristics as the exposure is increased. (The exposure at this point is called the saturation exposure.)

Note 4) Saturation Exposure (SE)
This is the exposure beyond which it is not possible to maintain the linearity of the output voltage as the exposure is increased. When designing the equipment using these devices, make sure that the incident light exposure is set with sufficient margin so that the CCD never gets saturated.

Note 5) Dark signal output voltage (V_{DRK})
This is defined as the average of the output from all the valid pixels in the dark condition at Ta=25˚C, T_{int}=10ms. Normally, the dark signal output voltage gets doubled for every 8 to 10˚C increase in Ta and is proportional to T_{int}.

Note 6) Dark signal non-uniformity (DSNU)
This is defined as the difference between the maximum value among the output voltages of the all valid pixels at Ta=25˚C and T_{int}=10ms and V_{DRK}.

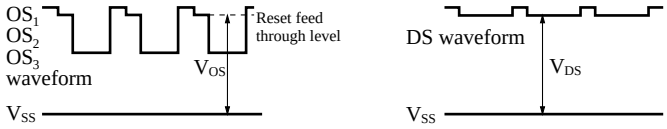
■ Optical Characteristics (continued)

Note 7) Dynamic range (DR)
This is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal output voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter.

Note 8) The signal output pin DC level (V_{OS}) and the compensation output pin DC level (V_{DS}) are the voltage values given in the following figure.



■ Construction of the Image Sensor

The MN3672 can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

a) Photo detector region

- The photoelectric conversion device consists of an 11µm floating photodiode and a 3µm channel stopper (isolation region) per pixel, and 5000 pixels' lines of each of the colors R, G, and B are arranged neighboring.
- There is a spacing of one line between B-R in the sideways scanning direction (center to center spacing of 14µm) and a similar one line spacing between R-G in the sideways scanning direction (center to center spacing of 14µm).
- The photodetector window is a rectangle of dimensions 8µm (Horizontal) × 11µm (Vertical), and the areas other than the photodetector window are optically shielded.
- The photodetector region has 24 optically shielded (black reference) pixels for each color that can be used as the black level reference.

b) CCD Transfer region (analog shift register)

- The signal charges obtained by photoelectric conversion are transferred to the CCD transfer regions of the respective colors during the period when the shift gate ($ø_{SG}$) is at the High level. The signal charges transferred to this analog shift register are successively transferred to the output region.
- A buried type CCD that can be driven by a two phase clock ($ø_1$, $ø_2$) is used for the analog shift register.
- In the CCD transfer region, since each CCD shift register is divided into four segments each of which are provided with separate $ø_1$, $ø_2$ clock pins, it is possible to reduce the heat generation in the chip and the load on the clock driver circuit by providing separate clock driver circuit for each pin during high speed operation.
- The last gate of the CCD transfer region is connected to an independent pin ($ø_{1L}$). By driving this pin independent of the other pins by a clock driver, it is possible to speed up the flow of signal charge into the charge to voltage conversion region thereby making the output waveform rise sharply. This makes it easy to obtain margin of the signal processing time during high speed drive operation.

c) Output region

- The signal charge transferred to the output region is first sent to the charge to voltage conversion region where it is converted into a voltage level corresponding to the amount of the signal charge, and then output after impedance conversion in a two stage source follower amplifier.
- The DC level component not containing the optical signal and the clock noise component are output at the DS pin.
- It is possible to obtain a signal with a high S/N ratio with reduced clock noise, etc., by carrying out differential amplification of the OS and DS outputs externally.

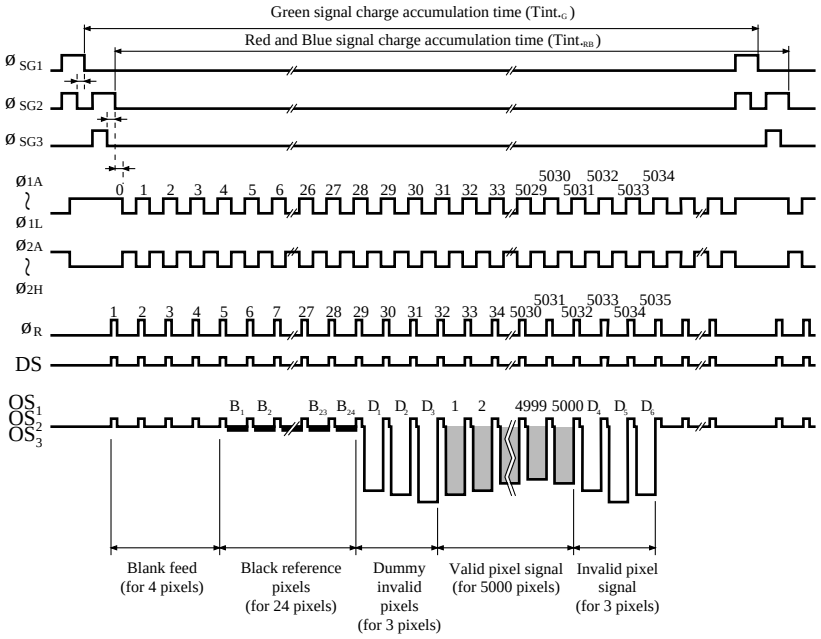
■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS_1	Signal output 1 (Red)	
2	OS_2	Signal output 2 (Green)	
3	V_{DD}	Power supply	
4	$ø_{SG1}$	Shift clock gate 1	Internally connected to pin 20.
5	V_{SS}	Ground	
6	$ø_R$	Reset clock	
7	NC	Non connection	
8	$ø_{2A}$	CCD clock (Phase 2)	All pins are independent. (Separate drivers can be used)
9	$ø_{1A}$	CCD clock (Phase 1)	
10	$ø_{1B}$	CCD clock (Phase 1)	
11	$ø_{2B}$	CCD clock (Phase 2)	
12	$ø_{2C}$	CCD clock (Phase 2)	
13	$ø_{1C}$	CCD clock (Phase 1)	
14	$ø_{1D}$	CCD clock (Phase 1)	
15	$ø_{2D}$	CCD clock (Phase 2)	
16	SUB	Substrate	Should be left open.
17	NC	Non connection	
18	V_{SS}	Ground	Connected to the aluminum layer for optical shielding.
19	V_{SS}	Ground	
20	$ø_{SG1}$	Shift clock gate 1	Internally connected to pin 4.
21	$ø_{SG2}$	Shift clock gate 2	
22	$ø_{SG3}$	Shift clock gate 3	Internally connected to pin 37.
23	NC	Non connection	
24	NC	Non connection	
25	NC	Non connection	
26	$ø_{2E}$	CCD clock (Phase 2)	All pins are independent. (Separate drivers can be used)
27	$ø_{1E}$	CCD clock (Phase 1)	
28	$ø_{1F}$	CCD clock (Phase 1)	
29	$ø_{2F}$	CCD clock (Phase 2)	
30	$ø_{2G}$	CCD clock (Phase 2)	
31	$ø_{1G}$	CCD clock (Phase 1)	
32	$ø_{1H}$	CCD clock (Phase 1)	
33	$ø_{2H}$	CCD clock (Phase 2)	
34	NC	Non connection	
35	$ø_{1L}$	CCD final stage clock (Phase 1)	
36	V_{SS}	Ground	Connected to the aluminum layer for optical shielding.
37	$ø_{SG3}$	Shift clock gate 3	Internally connected to pin 22.
38	V_{SS}	Ground	
39	DS	Compensation output	
40	OS_3	Signal output 3 (Blue)	

Note) Connect all NC pins externally to V_{SS} (GND).

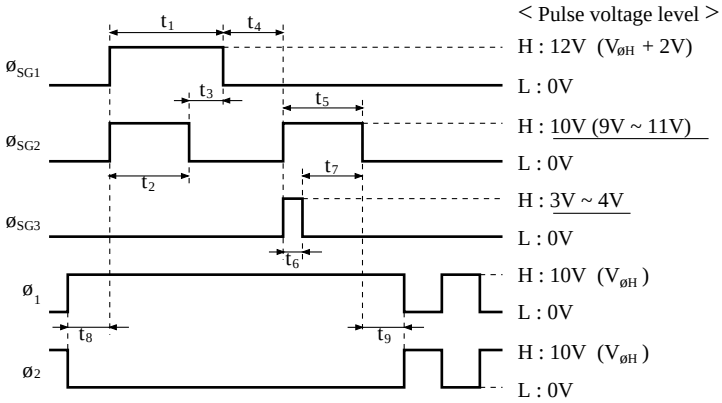
■ Timing Diagram

(1) I/O timing



(2) Drive timing 1

(during shifting signal charge to CCD)



< Pulse timing >

$t_1 \geq 5.5\mu s$ ($t_1 > t_2$)

$t_2 \geq 5\mu s$ ($t_2 = t_5$)

$t_3 \geq 0.5\mu s$

$t_4 \geq 0.5\mu s$

$t_5 \geq 5\mu s$ ($t_2 = t_5$)

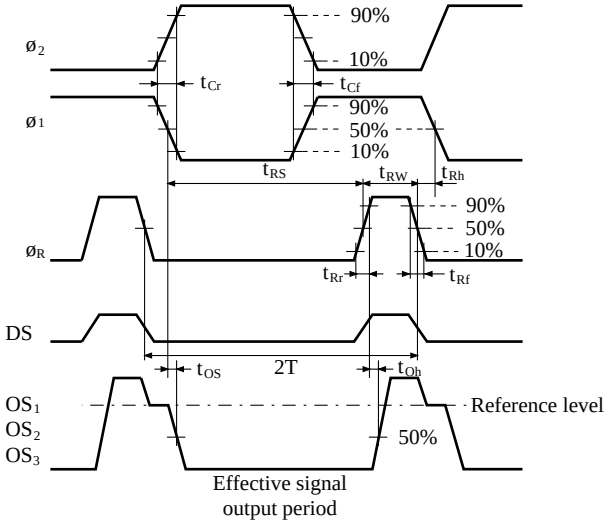
$t_6 \geq 1\mu s$

$t_7 \geq 4\mu s$

$t_8 \geq 0.5\mu s$

$t_9 \geq 0.5\mu s$

(2) Drive timing 2
(during repeated pattern)



■ Graphs and Characteristics

Spectral Response Characteristics