

# MN3666A

## 7500-Bit High-Speed High-Resolution CCD Linear Image Sensor

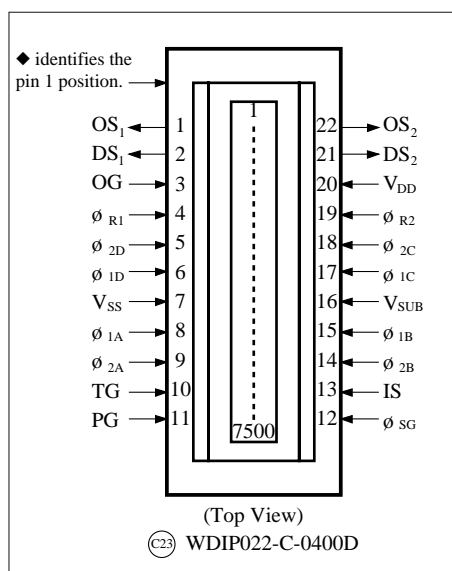
### Overview

The MN3666A is a high-speed high-resolution CCD linear image sensor having low dark output floating photodiodes in the photodetector region and CCD analog shift registers for read out. It provides large output at a high S/N ratio for visible light inputs over a wide range of wavelength.

### Features

- 7500 floating photodiodes and n-channel buried type CCD shift registers for read out are integrated in a single chip.
- Use of photodiodes with a new structure has made the dark output voltage very low.
- An A3 size document can be read with a high resolution of 600dpi.
- Permits high speed scanning of a data rate of 10MHz.
- High blue responsivity of a maximum responsivity ratio of 60% (typ.) at 400nm, and smooth spectral response over the entire visible region.
- A large signal output of 1400mV (typ.) can be obtained at saturation, and the hold type waveform output makes signal processing easy.
- Operation with a single +12V positive power supply.

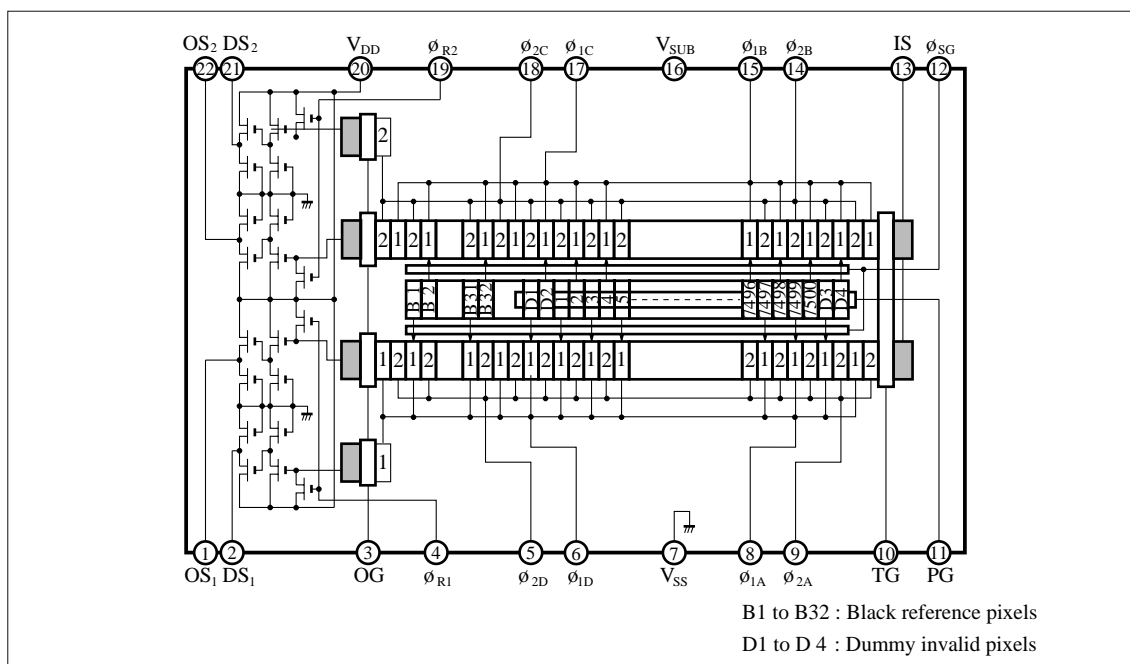
### Pin Assignments



### Application

- Graphic, character, and numeral read out in fax machines, image scanners, etc.

### Block Diagram



### ■ Absolute Maximum Ratings (Ta=25°C, Vss=0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V <sub>DD</sub>	− 0.3 to +17	V
	V <sub>SUB</sub>	− 0.3 to +17	V
	V <sub>IS</sub>	− 0.3 to +17	V
	V <sub>OG</sub>	− 0.3 to +17	V
	V <sub>PG</sub>	− 0.3 to +17	V
Input pin voltage	V <sub>I</sub>	− 0.3 to +17	V
Output pin voltage	V <sub>O</sub>	− 0.3 to +17	V
Operating temperature range	T <sub>opr</sub>	−20 to + 60	°C
Storage temperature range	T <sub>stg</sub>	−40 to +100	°C

### ■ Operating Conditions

#### • Voltage conditions (Ta=−20 to + 60°C, Vss=0V)

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply voltage	V <sub>DD</sub>		11.5	12.0	12.5	V
IS test pin voltage	V <sub>IS</sub>	V <sub>IS</sub> = V <sub>DD</sub>	11.5	12.0	12.5	V
Substrate voltage	V <sub>SUB</sub>	V <sub>SUB</sub> = V <sub>DD</sub>	11.5	12.0	12.5	V
Output gate voltage	V <sub>OG</sub>		4.2	4.5	4.8	V
Photo storage gate voltage	V <sub>PG</sub>	V <sub>PG</sub> = V <sub>OG</sub>	4.2	4.5	4.8	V
TG test pin voltage	V <sub>TG</sub>	V <sub>TG</sub> = V <sub>SS</sub>	0	0	0.3	V
CCD shift register clock High level	V <sub>oH</sub>	Note 1	8.0	10.0	V <sub>DD</sub>	V
CCD shift register clock Low level	V <sub>oL</sub>		0	0.5	0.8	V
Shift gate clock High level	V <sub>SH</sub>		9.0	V <sub>DD</sub>	V <sub>DD</sub>	V
Shift gate clock Low level	V <sub>SL</sub>		0	0.5	0.8	V
Reset gate clock High level	V <sub>RH</sub>		9.0	V <sub>DD</sub>	V <sub>DD</sub>	V
Reset gate clock Low level	V <sub>RL</sub>		0	0.5	0.8	V

Note 1) There is no problem in operation even when the CCD shift register clock High level is a voltage equal to about V<sub>DD</sub>, it is preferable to set this at a value close to the standard value considering the load on the clock driver particularly at high speed drives and the increase in the dark signal output voltage due to the heat generation in the chip.

#### • Timing conditions (Ta=−20 to + 60°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock frequency	f <sub>C</sub>	f <sub>C</sub> = f <sub>R</sub> = 1/2T	0.1	1.0	5.0	MHz
Reset clock frequency	f <sub>R</sub>		0.1	1.0	5.0	MHz
Shift register clock rise time	t <sub>Cr</sub>	Note 1	0	20	50	ns
Shift register clock fall time	t <sub>Cf</sub>		0	20	50	ns
Shift clock rise time	t <sub>Sr</sub>		0	15	50	ns
Shift clock fall time	t <sub>Sf</sub>		0	15	50	ns
Shift clock set up time	t <sub>Ss</sub>		250	400	1000	ns
Shift clock pulse width	t <sub>Sw</sub>		1.0	1.8	20	μs
Shift clock hold time	t <sub>Sh</sub>		0	0.5	1	μs
Reset clock rise time	t <sub>Rr</sub>		0	10	20	ns
Reset clock fall time	t <sub>Rf</sub>		0	10	20	ns
Reset clock set up time	t <sub>Rs</sub>		0.7T	—	—	ns
Reset clock pulse width	t <sub>Rw</sub>		20	30	—	ns
Reset clock hold time	t <sub>Rh</sub>		5	10	—	ns

Note 1) The lag characteristic becomes better if the shift clock pulse width is made long if there is no problem in the timing generation.

Note 2) The standard values of the timing conditions given above are merely for guidance and need not be taken as valued strictly required for operation. Determine the optimum values by experimentation depending on the actually used driving frequency and signal processing method.

## ■ Electrical Characteristics

- Clock input capacitance (Ta=−20 to + 60°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Shift register clock input capacitance	$C_{1A}, C_{2A}$ $C_{1B}, C_{2B}$	$V_{IN}=12V$ $f=1MHz$	—	600	750	pF
Reset clock input capacitance	$C_R$		—	15	30	pF
Shift clock input capacitance	$C_S$		—	100	150	pF

\* $\phi_{1A}$ ,  $\phi_{2A}$ ,  $\phi_{1B}$ , and  $\phi_{2B}$  are respectively connected to  $\phi_{1D}$ ,  $\phi_{2D}$ ,  $\phi_{1C}$ , and  $\phi_{2C}$  internally.

## • DC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Power supply current	$I_{DD}$	$V_{DD}=+12V$	—	20	50	mA
IS test pin leak current	$I_{IS}$		—	—	1	mA
Photo storage gate leak current	$I_{PG}$	$V_{DD}=+5V$	—	—	50	$\mu A$
Output gate pin leak current	$I_{OG}$		—	—	50	$\mu A$

## • AC characteristics

Parameter	Symbol	Condition	min	typ	max	Unit
Signal output set up time *	$t_{OS}$		—	30	—	ns
Signal output hold time	$t_{OW}$		—	30	—	ns

\* OS output level: =500mV

## ■ Optical Characteristics

<Inspection conditions>

- Ta=25°C
- $V_{DD}=V_{IS}=V_{SUB}=12V$  (DC),  $V_{OG}=V_{PG}=4.5V$  (DC),  $V_{\phi H}=10V$  (pulse),  $V_{SH}=V_{RH}=12V$  (pulse)
- $f_C=f_R=1MHz$ ,  $T_{int}$  (accumulation time)=10ms
- Light source: Daylight type fluorescent lamp
- Optical system: A slit with an aperture dimensions of 20mm × 20mm is used at a distance of 200mm from the sensor (equivalent to F=10).
- This parameters are inspected by signal multiplex with channels 1 and 2 which correspond to the output of both OS<sub>1</sub> and DS<sub>1</sub> (channel 1) and the output of both OS<sub>2</sub> and DS<sub>2</sub> (channel 2) respectively. Before multiplex the channels 1 and 2, the OS and DS signals should be respectively through unity gain differential amplifiers with input impedances of 100k Ohms or more, carrying out zero level DC clamping of each channel.
- These specifications apply to the 7500 valid pixels excluding the dummy pixels D1 to D4.

Parameter	Symbol	Condition	min	typ	max	Unit
Responsivity	R	Note 1	1.6	1.9	2.2	V/lx · s
Photo response non-uniformity	PRNU	Note 2	—	—	15	%
Bit non-uniformity	BNU	Note 3	—	—	±8	%
Saturation output voltage	$V_{SAT}$	Note 4	1.00	1.40	—	V
Saturation exposure	SE	Note 5	0.45	0.74	—	lx · s
Dark signal output voltage	$V_{DRK}$	Dark condition, see Note 6	—	0.5	3.0	mV
Dark signal output non-uniformity	DSNU	Dark condition, see Note 7	—	0.2	2.0	mV
Shift register total transfer efficiency	STTE	Note 8	92	—	—	%
Dynamic range	DR	Note 9	—	2800	—	
Modulation transfer function	$MTF_R$	Note 10	—	65	—	%

\* The definitions of the parameters are given in Note 1) to Note 10) on the following page.

## ■ Optical Characteristics (continued)

### Note 1) Responsivity (R)

This is the value obtained by dividing the average output voltage (V) of the 7500 valid pixels by the exposure (lx·s).

The exposure (lx·s) is the product of the illumination intensity (lx) and the accumulation time (s).

Since the responsivity changes with the spectral distribution of the light source used, care should be taken when using a light source other than the daylight type fluorescent lamp specified in the inspection conditions.

### Note 2) Photo response non-uniformity (PRNU)

The photo response non-uniformity (PRNU) is defined by the following equation, where  $X_{ave}$  is the average output voltage of the valid 7500 pixels and  $\Delta x$  is the absolute value of the difference between the maximum and minimum voltage, when the surface of the photo-sites is illuminated with light having a uniform distribution over the entire surface.

$$PRNU = \frac{\Delta x}{X_{ave}} \times 100 (\%)$$

The incident light intensity shall be 50% of the standard saturation light intensity.

### Note 3) Bit non-uniformity (BNU)

This is defined by the following equation where the output voltage of each pixel among the 7500 pixels is denoted by  $X_i$  ( $i = 1$  to 7500) when the photodetector region is illuminated by a light of uniform illumination intensity distribution, and the average output voltage of the pixels near the  $i$ th pixel is denoted by  $X_{local-ave}$ . (a total of 20 pixels with 10 pixels before and 10 pixels after that pixel). Here, the max. operation consists of comparing with the absolute value and assigning the sign of the numerator.

$$BNU = \max. \left( \frac{X_i - X_{local-ave}}{X_{local-ave}} \right) \times 100 (\%)$$

The incident light intensity shall be 50% of the standard saturation light intensity.

### Note 4) Saturation output voltage ( $V_{SAT}$ )

This is the output voltage at the point beyond which it is not possible to maintain the linearity of the photoelectric conversion characteristics as the exposure is increased. (The exposure at this point is called the saturation exposure.)

### Note 5) Saturation Exposure (SE)

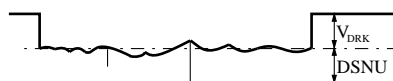
This is the exposure beyond which it is not possible to maintain the linearity of the output voltage as the exposure is increased. When designing the equipment using these devices, make sure that the incident light exposure is set with sufficient margin so that the CCD never gets saturated.

### Note 6) Dark signal output voltage ( $V_{DRK}$ )

This is defined as the average of the output from the 7500 active pixels in the dark condition at  $T_a=25^\circ\text{C}$ ,  $T_{int}=10\text{ms}$ . Since normally the dark signal output voltage gets doubled for every 8 to  $10^\circ\text{C}$  increase in  $T_a$  and is proportional to  $T_{int}$ , it is necessary to convert the value if  $T_a$  and  $T_{int}$  are different from the inspection conditions given above. (See the figure below.)

### Note 7) Dark signal non-uniformity (DSNU)

This is defined as the difference between the maximum value among the output voltages from the 7500 valid pixels at  $T_a=25^\circ\text{C}$  and  $T_{int}=10\text{ms}$  and  $V_{DRK}$ . (See the figure below.)



### Note 8) Shift register total transfer efficiency (STTE)

This is given by the following equation where the average output voltage of all the 7500 pixels is denoted by  $X_{ave}$ , and the larger of the output voltages of the 2 dummy pixels following the dummy pixel D4 is denoted by  $X_r$  when the photodetector region is illuminated by a light of uniform illumination intensity distribution.

$$STTE = \frac{X_{ave} - X_r}{X_{ave}} \times 100 (\%)$$

### Note 9) Dynamic range (DR)

This is defined by the following equation.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

Since the dark signal output voltage is proportional to the accumulation time, the dynamic range becomes wider when the accumulation time is shorter. This value is not a guaranteed value, but is merely a reference value.

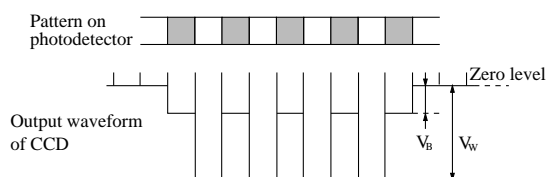
### Note 10) Modulation transfer function ( $MTF_R$ )

This is defined by the following equation where the average output voltages of the pixels with the white pattern and the pixels with the black pattern are respectively denoted by  $V_W$  and  $V_B$  when a black and white stripe pattern (in which the black and white patterns alternate at every pixel) is projected on the photodetector region in phase (equivalent to the Nyquist spatial frequency).

$$MTF_R = \frac{V_W - V_B}{V_W + V_B} \times 100 (\%)$$

This value is a measure of resolution of the sensor.

This parameter is not a guaranteed value but is merely a reference value.



### ■ Pin Descriptions

Pin No.	Symbol	Pin name	Condition
1	OS <sub>1</sub>	Signal output 1	
2	DS <sub>1</sub>	Compensation output 1	
3	OG	Output gate	
4	$\phi_{R1}$	Reset clock	
5	$\phi_{2D}$	CCD shift register clock	
6	$\phi_{1D}$	CCD shift register clock	
7	V <sub>SS</sub>	Ground	
8	$\phi_{1A}$	CCD shift register clock	Internally connected to $\phi_{1D}$ .
9	$\phi_{2A}$	CCD shift register clock	Internally connected to $\phi_{2D}$ .
10	TG	Test pin	Connect externally to V <sub>SS</sub> .
11	PG	Photo storage gate	
12	$\phi_{SG}$	Shift clock gate	
13	IS	Test pin	Connect externally to V <sub>DD</sub> .
14	$\phi_{2B}$	CCD shift register clock	Internally connected to $\phi_{2C}$ .
15	$\phi_{1B}$	CCD shift register clock	Internally connected to $\phi_{1C}$ .
16	V <sub>SUB</sub>	Substrate	Connect externally to V <sub>DD</sub> .
17	$\phi_{1C}$	CCD shift register clock	
18	$\phi_{2C}$	CCD shift register clock	
19	$\phi_{R2}$	Reset clock	
20	V <sub>DD</sub>	Power supply	
21	DS <sub>2</sub>	Compensation output 2	
22	OS <sub>2</sub>	Signal output 2	

### ■ Construction of the Image Sensor

The MN3666A can be made up of the three sections of—a) photo detector region, b) CCD transfer region (shift register), and c) output region.

#### a) Photo detector region

- The photoelectric conversion device consists of a 6 $\mu$ m floating photodiode and a 3 $\mu$ m channel stopper for each pixel, and 7500 of these devices are linearly arranged side by side at a pitch of 9 $\mu$ m.
- The photo detector's windows are 9 $\mu$ m  $\times$  9 $\mu$ m squares and light incident on areas other than these windows is optically shut out.
- The photo detector is provided with 32 optically shielded pixels (black dummy pixels) which serve as the black reference.

#### b) CCD Transfer region (shift register)

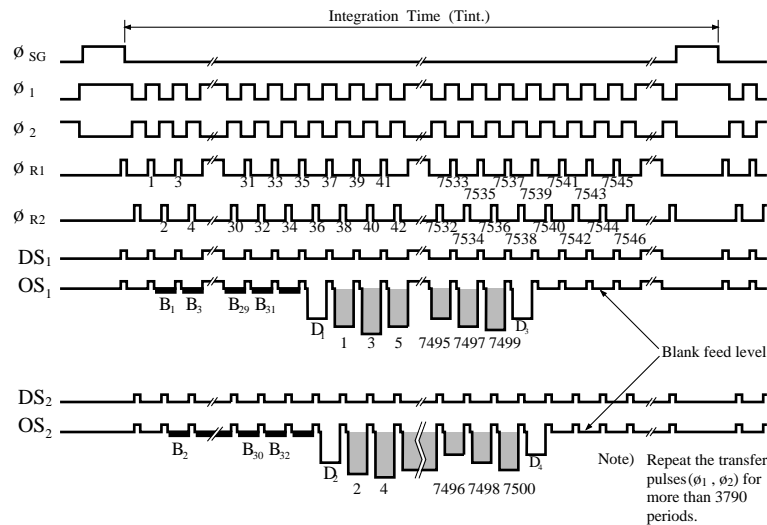
- The light output that has been photoelectrically converted is transferred to the CCD transfer for each odd and even pixel at the timing of the shift clock ( $\phi_{SG}$ ). The optical signal electric charge transferred to this analog shift register is successively transferred out and guided to the output region.
- A buried type CCD that can be driven by a two phase clock ( $\phi_1$ ,  $\phi_2$ ) is used for the analog shift register.

#### c) Output region

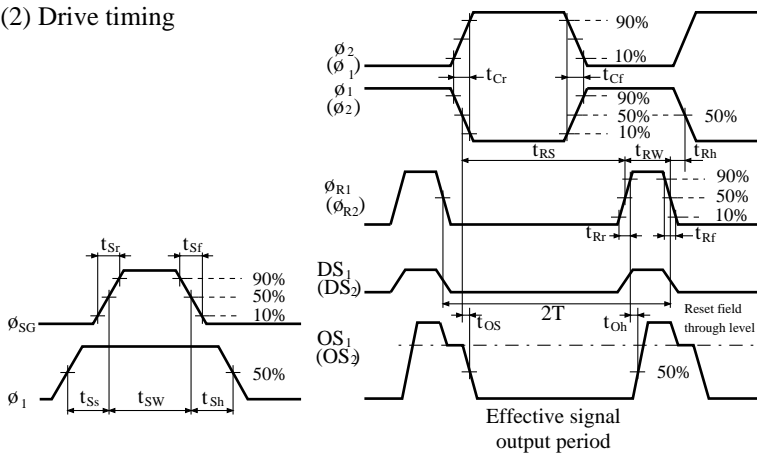
- The signal charge that is transferred to the output region is sent to the detector where impedance transformation is done using two source follower stages.

■ Timing Diagram

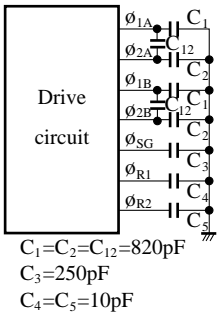
(1) I/O timing



(2) Drive timing

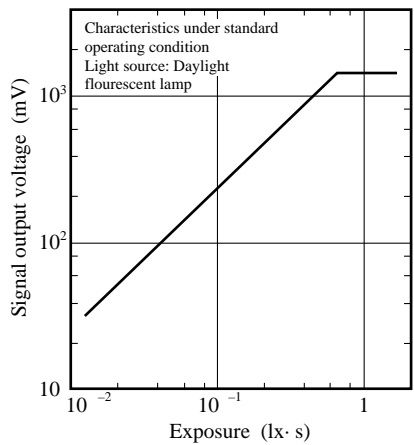


(3) Timing condition measuring circuit

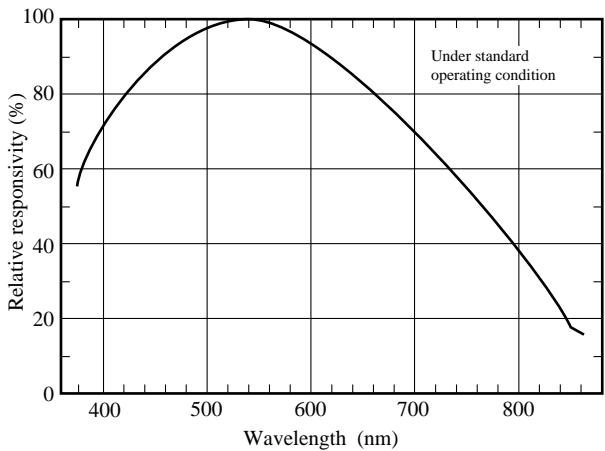


■ Graphs and Characteristics

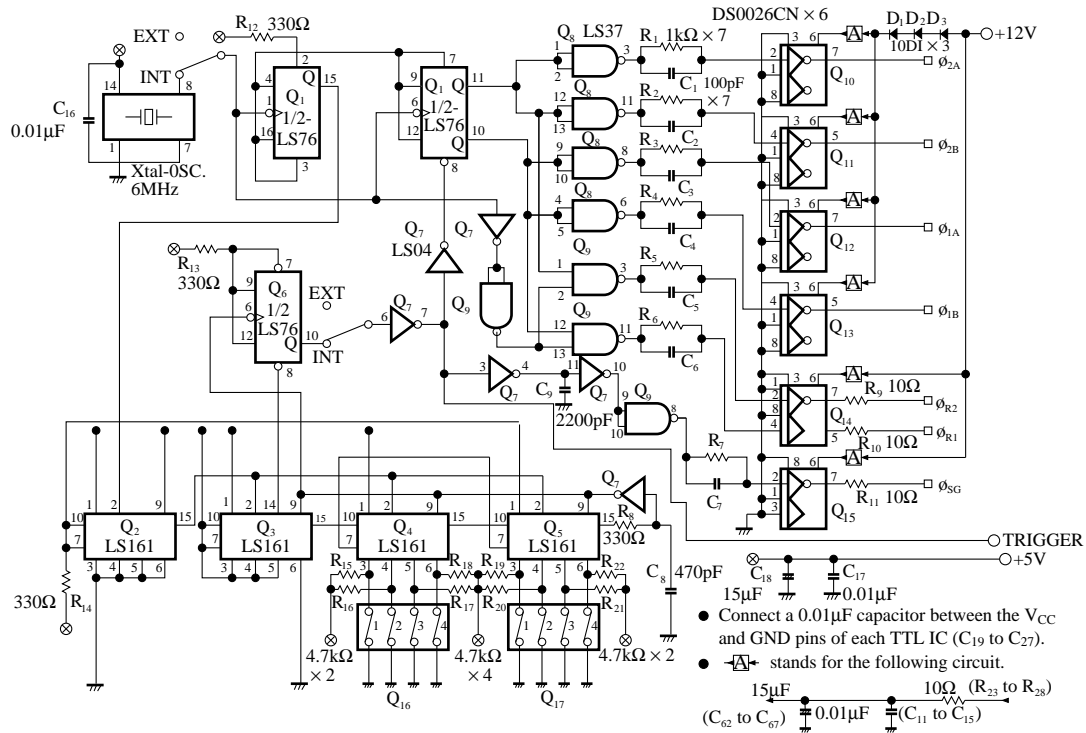
Photoelectric Conversion Characteristics



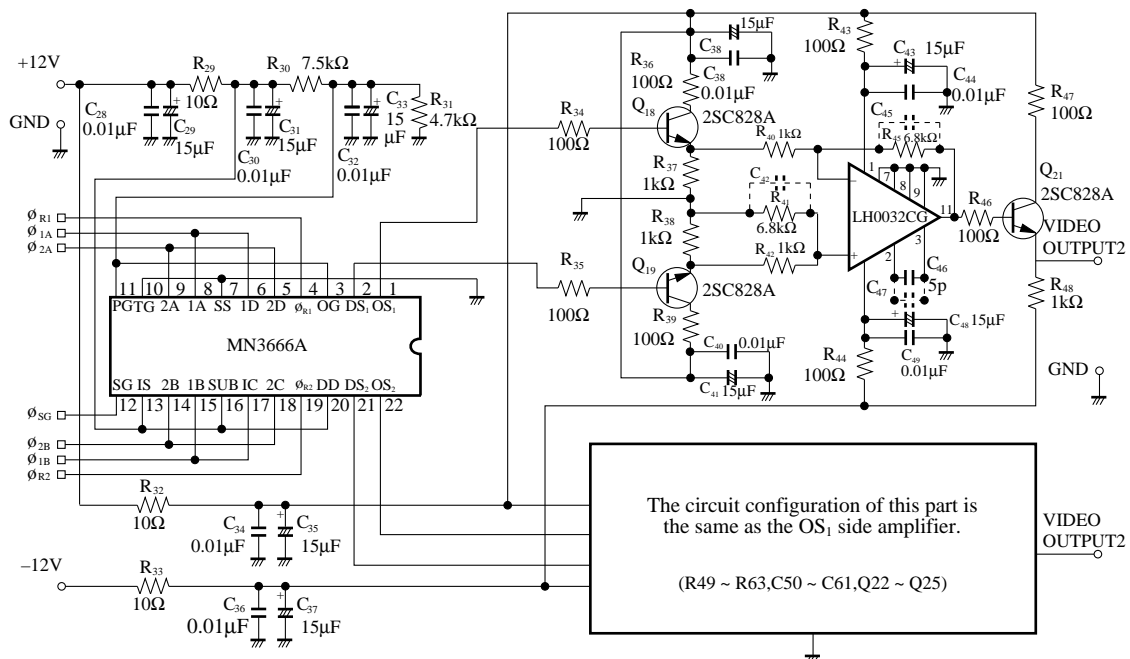
Spectral Response Characteristics



## ■ Drive Circuit Diagram (Digital Section)



## ■ Drive Circuit Diagram (Analog Section)



- The drive circuit shown here is sample drive circuit when evaluating the first stage of the MN3666A and any other drive circuit can be used as long as the operating conditions are satisfied.